
SAM G53 Series Family Silicon Errata and Data Sheet Clarification

The SAM G53 Series family of devices that you have received conform functionally to the current Device Data Sheet (Atmel-11240F-ATARM-SAM-G53G-SAM-G53N-Datasheet_24-Jul-15), except for the anomalies described in this document.

New Silicon Errata Issues

<p>Note: This document provides information on new errata issues for the SAM G53 Series of devices. Please refer to the current device data sheet for all pre-existing silicon errata issues.</p>
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There are no new silicon errata to report at this time.

SAM G53 SERIES

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (Atmel-11240F-ATARM-SAM-G53G-SAM-G53N-Datasheet_24-Jul-15).

Corrections in tables and paragraphs are shown in **bold**. Where possible, the original bold text formatting has been removed for the clarity.

1. Module: Bootloader

Chapter 8 “Bootloader” has a new verbiage for the NRST line. The newly added text is shown in bold.

The SAM G53 devices ship with a factory-programmed Bootloader in Flash. The Flash loader downloads code either through the SPI or through the TWI0.

The Bootloader mode is entered automatically on power-up if no valid firmware is detected in the Flash. A valid firmware is detected by performing a CRC on the content of the Flash. If the CRC is correct, the application is started. Otherwise, the Bootloader mode is entered.

Alternatively, the Bootloader mode can be forced by applying 10 low pulses of 1 ms on the NRST line (with a period of 10 ms max). When the Bootloader detects this sequence, it asserts the pin PA01 (NCHG) low as an acknowledge.

The Bootloader mode initializes the TWI0 in Slave Mode with the I²C address 0x26 and the SPI in Slave Mode, 8-bit data length, SPI Mode 1.

2. Module: CKGR_PLLAR Register

In the current data sheet section 25.17.9, the MULA bit field for the CKGR_PLLAR register extends from bit 16 to bit 27. The corrected bit field extends from bit 16 to bit 28.

3. Module: PMC_PMMR Register

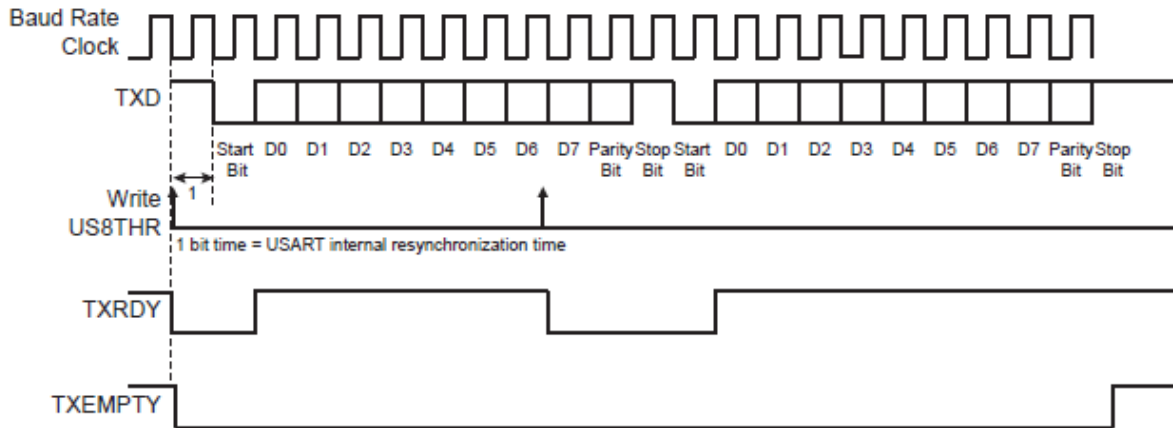
In the current data sheet section 25.17.26 the PLLA_MMAX bit field for the PMC_PMMR register extends from bit 0 to bit 10. The corrected bit field extends from bit 0 to bit 12.

4. Module: I2SC_MR Register

The table for the FORMAT bit is incorrect and lists Left Justified format. This format is not supported for this device.

5. Module: Transmitter Operations

Figure 33-6 is incorrect, and the corrected figure is as follows:



6. Module: Multi-drop Mode

In the Section 33.6.3.6, the bit name SENTA is incorrect. The corrected name is SENDA.

7. Module: ISO7816 Mode Overview

The last paragraph of the Section 33.6.4.1 has erroneous text. The corrected version is shown in bold.

When operating in ISO7816, either in T = 0 or T = 1 modes, the character format is fixed. The configuration is 8 data bits and 1 or 2 stop bits, regardless of the values programmed in the Mode register fields CHRL, MODE9 and CHMODE. MSBF can be used to transmit LSB or MSB first. Parity Bit (PAR) can be used to transmit in normal or inverse mode. Refer to Section 31.7.3 "USART Mode Register" and "PAR: Parity Type".

8. Module: US_RTOR Register

In the section 33.7.16, the TO bit information is incomplete, hence the following information has been added.

16 bits for USART which supports all modes.

8 bits for USART which does not support ISO7816.

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APPENDIX A: REVISION HISTORY

Revision A Document (07/2019)

This is the initial released version of this document.

Note the following details of the code protection feature on Microchip devices:

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