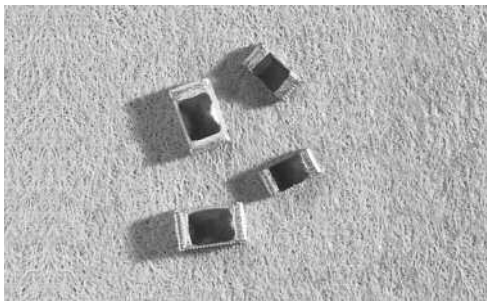
ESD Suppression selection guide for polymer ESD suppressors



Overview

Eaton's Voltage Variable Material (VVM) ESD suppressors have unique properties that are highly preferred in ESD suppression applications. The polymer matrix responds to an overvoltage condition by rapidly changing from a high impedance state to a low impedance state.

Eaton utilizes this polymeric matrix for fast response, ultra-low capacitance, and very low current leakage. The device is activated by overvoltage threats and clamps to a low value to protect sensitive circuit components.

How it works

Eaton's VVM ESD suppressor families are board level circuit protection devices designed exclusively for the fast, transient overvoltages associated with ESD. When a sufficient overvoltage occurs it exhibits a dramatic increase in the ability to conduct electrons. The nature of the material creates a bi-directional part, which means that only one device is required to provide complete ESD protection regardless of the surge polarity.

In a typical application, the device is placed across a signal line leading to an integrated circuit and ground. The device exhibits minimal capacitance and is "invisible" to the circuit during the normal operation. Under normal operating voltages (typically 3 to 15 V) the high impedance of the device insulates each signal line from ground. When an ESD event occurs, the voltage variable material switches to a conductive state within nanoseconds. The voltage across signal line collapses to the clamping level, and current is shunted through the device to the ground.

When the overvoltage event ends, the circuit returns to its normal operating state as the device switches back to its $>10^{12}$Ohm, high resistance state and "invisibility."

VVM ESD suppressor selection guide:

Part Number	Package Size	Lines	Operating Voltage (Vdc)	Capacitance (pF @ 1 kHz ~ 1.8 GHz)	Current Leakage (nA @ 12 Vdc)	Clamp Voltage V	Specification
0402ESDA-MLP1	0402	1	0 ~ 30	< 0.15	< 0.1	35	IEC61000-4-2, Level 4
0603ESDA-MLP7	0603	1	0 ~ 30	< 0.15	< 0.1	35	IEC61000-4-2, Level 4
PS04LTVA1	0402	1	0 ~ 12	< 0.15	< 0.1	25	IEC61000-4-2, Level 4
0603ESDA2-TR2	0603	1	0 ~ 30	< 0.15	< 0.1	35	IEC61000-4-2, Level 4

Device marking

VVM ESD Suppressors are marked on the tape and reel packages, not individually. Since the product is bi-directional and symmetrical, no orientation marking is required.

Test methodology

Full product characterization requires use of multiple test methods. Each test method reveals unique information about the device response. The results of all of the tests must be analyzed to fully understand the VVM ESD Suppressor response to an overvoltage event.

Electrostatic Discharge (ESD) pulse

The ESD pulse is the defining test for an ESD protective device. The ESD pulse is an extremely fast rising transient event. The pulse, as characterized in IEC 61000-4-2, has a rise time of less than 1 ns, peak currents up to 45 A, and voltage levels to 15 kV (Figure 1). Characteristics determined by this test are those such as voltage overshoot, peak voltage, clamping voltage, peak current, and device resistance.

Due to the extremely fast rate of rise of the ESD pulse, the test setup can have a definite impact on the above factors. Variables such as wiring inductance and probe capacitance can produce inaccurate readings on an otherwise capable oscilloscope.

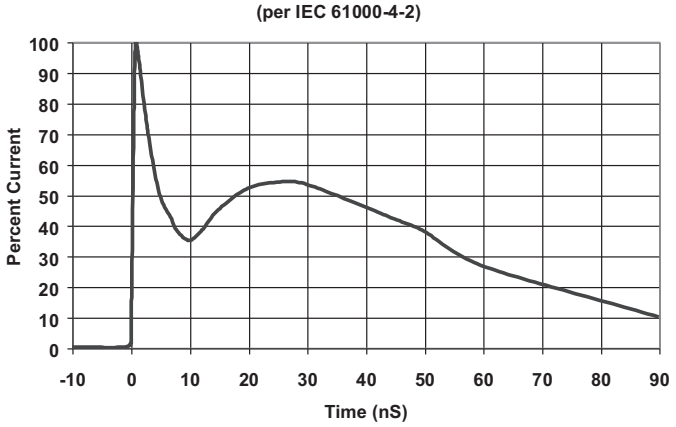


Figure 1. IEC 6100-4-2 ESD pulse

Transmission Line Pulse (TLP)

The Transmission Line Pulse tester implements a controlled impedance cable to deliver a square wave current pulse. The advantage of this technique is that the constant current of the square wave allows the behavior of the protection structure to be more accurately studied.

The actual implementation of this technique produces a waveform that has a slightly slower rise time that the ESD pulse but can be correlated to the deliver approximately the same surge current and energy (Figure 2). This controlled impedance pulse provides a more accurate depiction of the trigger voltage of the device because of the reduced voltage overshoot caused by a fast rising transient and the reactive components of the test fixture.

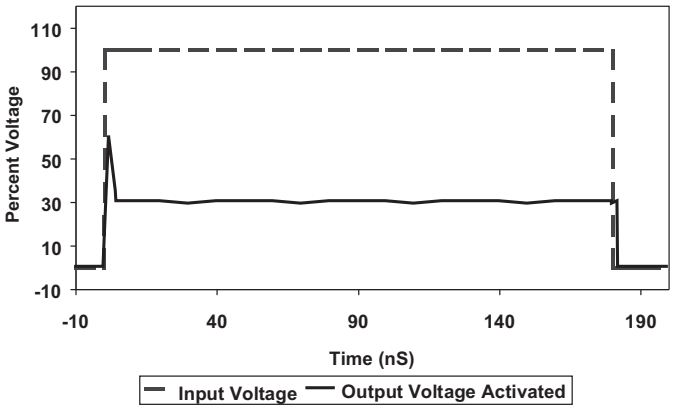


Figure 2. Transmission Line Pulse

Definition of terms

Clamp Voltage – The voltage at which the VVM device stabilizes during the transition from high to low impedance. This is the voltage experienced by the circuit, after stabilizing, for the duration of the ESD transient.

Trigger Voltage – The voltage at which the VVM device begins to function. When the ESD threat voltage reaches this level, the VVM device begins the transition from high impedance to low impedance, shunting the ESD energy to ground.

Threat Voltage – The voltage that the test equipment is set to operate (i.e. the voltage across the discharge capacitor).

Peak Current – The maximum instantaneous current level that a device will receive. IEC-61000-4-2 states that the peak current should be 30 A at 8 kV ESD and 45 A at 15 kV ESD.

ESD Transient pulse energy controlled by the VVM ESD suppressor

Figure 3 shows typical VVM ESD suppressor response to an 8 kV contact ESD pulse. Triggered polymer in the device conducts excess energy to ground and prevents system damage by ESD transient threat. As the polymer resistance drops current flows to ground. The top scope trace indicates current, and the bottom scope trace indicates voltage.

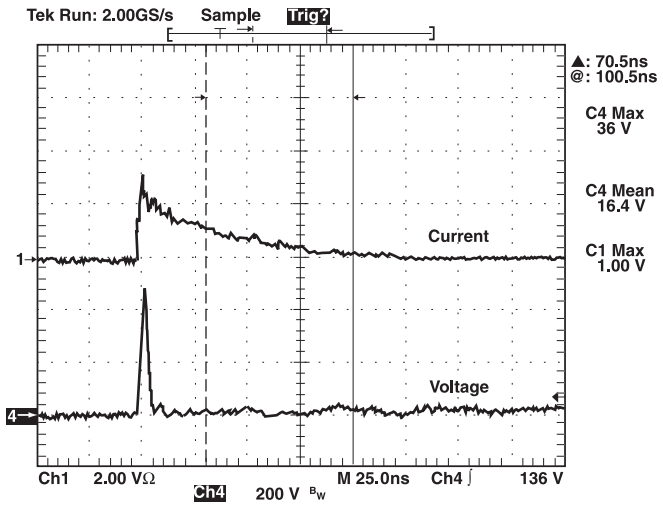


Figure 3. Typical device response to an 8 kV ESD

VVM ESD suppressor protects against ESD voltage transient without affecting signal quality

VVM ESD Suppressors have an ultra low capaci-tance of <0.15 pF and when typically installed from the signal line to ground have a negligible effect on the signal.

Figure 4 illustrates the test conducted with a precision network analyzer on a 50 Ω circuit at up to 6 GHz. Only a 0.2 dB deviation from the original signal was recorded.

The setup was similar to the addition of the VVM ESD suppressor to a circuit with very fast digital signal or a mobile phone antenna.

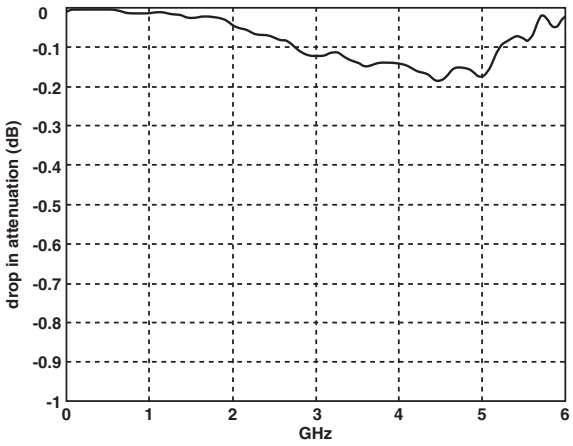


Figure 4. VVM device induced interference with signal quality

Signal frequency does not affect the capacitance of the device

The device capacitance is very low and constant over a wide frequency range. The typical capacitance is less than 0.15 pF over the tested range of 0.1 MHz to 1.8 GHz. Figure 5 demonstrates the capacitance will remain same over the life cycle of the device (i.e. the number of the ESD pulse does not change the device capacitance).

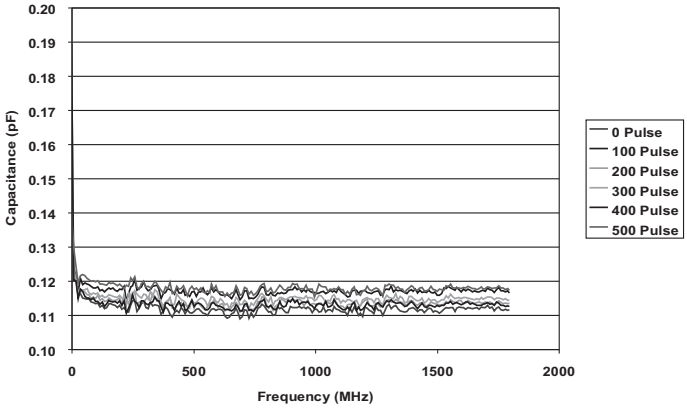


Figure 5. Capacitance vs. frequency curve

Clamp voltage remains consistent despite repeated ESD pulses

As depicted in Figure 6, the VVM ESD suppressors are highly reliable and stable over hundreds of pulses. The VVM ESD suppressors have been tested with fast rate ESD pulses at 8 kV contact discharge. Clamping voltage measured at every pulse shows minimal changes throughout the test.

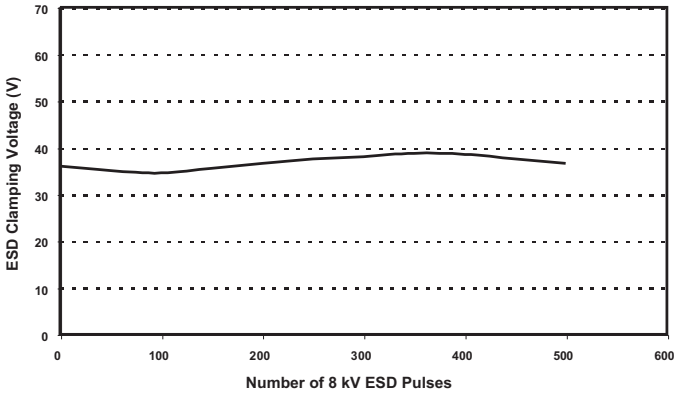


Figure 6. ESD Clamping voltage vs. number of 8 kV ESD Pulses

Typical non-triggered (off state) current leakage of VVM is very low at normal operating voltages and temperatures

The current leakage of the VVM ESD Suppressor is typically very low, well under 1 nA, even over 12 Vdc operating voltage (Figure 7). Some increase in the current leakage may be expected at much higher operating voltage and elevated temperature.

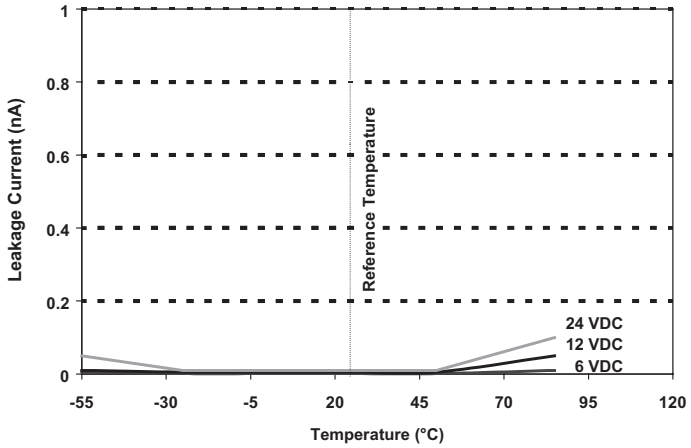


Figure 7. Average off state current leakage vs. temperature

Eaton
1000 Eaton Boulevard
Cleveland, OH 44122
United States
www.eaton.com/electronics

Printed in USA
Publication No.
December 2017

Powering Business Worldwide