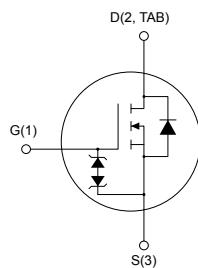


## N-channel 650 V, 1.4 $\Omega$ typ., 3.5 A MDmesh M6 Power MOSFET in a DPAK package


**DPAK**


AM01475V1

### Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|------------|----------|-------------------|-------|
| STD3N65M6  | 650 V    | 1.5 $\Omega$      | 3.5 A |

- Reduced switching losses
- Lower  $R_{DS(on)}$  per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent  $R_{DS(on)}$  per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



#### Product status link

[STD3N65M6](#)

#### Product summary

|                   |           |
|-------------------|-----------|
| <b>Order code</b> | STD3N65M6 |
| <b>Marking</b>    | 3N65M6    |
| <b>Package</b>    | DPAK      |
| <b>Packing</b>    | Tube      |

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol         | Parameter                                                       | Value      | Unit             |
|----------------|-----------------------------------------------------------------|------------|------------------|
| $V_{GS}$       | Gate-source voltage                                             | $\pm 25$   | V                |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 3.5        | A                |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 2.2        | A                |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                          | 14         | A                |
| $P_{TOT}$      | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$     | 45         | W                |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                               | 5          | V/ns             |
| $dv/dt^{(3)}$  | MOSFET $dv/dt$ ruggedness                                       | 100        |                  |
| $T_J$          | Operating junction temperature range                            | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature range                                       |            |                  |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 3.5\text{ A}$ ,  $di/dt=400\text{ A}/\mu\text{s}$ ;  $V_{DS}(\text{peak}) < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .
3.  $V_{DS} \leq 520\text{ V}$ .

**Table 2. Thermal data**

| Symbol              | Parameter                        | Value | Unit                      |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$      | Thermal resistance junction-case | 2.78  | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb  | 50    |                           |

1. When mounted on FR-4 board of  $\text{inch}^2$ , 2 oz Cu.

**Table 3. Avalanche characteristics**

| Symbol   | Parameter                                                                                                            | Value | Unit |
|----------|----------------------------------------------------------------------------------------------------------------------|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_J$ max)                                   | 1     | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 78    | mJ   |

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified

**Table 4. On/off-state**

| Symbol        | Parameter                         | Test conditions                                                                        | Min. | Typ. | Max.    | Unit          |
|---------------|-----------------------------------|----------------------------------------------------------------------------------------|------|------|---------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$                                            | 650  |      |         | V             |
| $I_{DSS}$     | Zero gate voltage drain current   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$                                        |      |      | 1       | $\mu\text{A}$ |
|               |                                   | $V_{GS} = 0\text{ V}$ , $V_{DS} = 650\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup> |      |      | 100     | $\mu\text{A}$ |
| $I_{GSS}$     | Gate body leakage current         | $V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$                                     |      |      | $\pm 5$ | $\mu\text{A}$ |
| $V_{GS(th)}$  | Gate threshold voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                     | 2.25 | 3    | 3.75    | V             |
| $R_{DS(on)}$  | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$ , $I_D = 1.75\text{ A}$                                         |      | 1.4  | 1.5     | $\Omega$      |

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

| Symbol                              | Parameter                     | Test conditions                                                                                                                               | Min. | Typ. | Max. | Unit     |
|-------------------------------------|-------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|----------|
| $C_{iss}$                           | Input capacitance             | $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$                                                                          | -    | 150  | -    | pF       |
| $C_{oss}$                           | Output capacitance            |                                                                                                                                               | -    | 13   | -    | pF       |
| $C_{rss}$                           | Reverse transfer capacitance  |                                                                                                                                               | -    | 0.7  | -    | pF       |
| $C_{oss\text{ eq.}}$ <sup>(1)</sup> | Equivalent output capacitance | $V_{DS} = 0\text{ to }520\text{ V}$ , $V_{GS} = 0\text{ V}$                                                                                   | -    | 31   | -    | pF       |
| $R_G$                               | Intrinsic gate resistance     | $f = 1\text{ MHz}$ , $I_D = 0\text{ A}$                                                                                                       | -    | 5.2  | -    | $\Omega$ |
| $Q_g$                               | Total gate charge             | $V_{DD} = 520\text{ V}$ , $I_D = 3.5\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$<br>(see Figure 14. Test circuit for gate charge behavior) | -    | 6    | -    | nC       |
| $Q_{gs}$                            | Gate-source charge            |                                                                                                                                               | -    | 1    | -    | nC       |
| $Q_{gd}$                            | Gate-drain charge             |                                                                                                                                               | -    | 3.2  | -    | nC       |

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

| Symbol       | Parameter           | Test conditions                                                                                         | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---------------------------------------------------------------------------------------------------------|------|------|------|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 325\text{ V}$ , $I_D = 1.75\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ | -    | 5.2  | -    | ns   |
| $t_r$        | Rise time           |                                                                                                         | -    | 5.4  | -    | ns   |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | -    | 14.1 | -    | ns   |
| $t_f$        | Fall time           |                                                                                                         | -    | 17.1 | -    | ns   |

**Table 7. Source-drain diode**

| Symbol          | Parameter                     | Test conditions                                                                                                                  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |                                                                                                                                  | -    |      | 3.5  | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |                                                                                                                                  | -    |      | 14   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 3.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$                                                                                | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 3.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$                                         | -    | 159  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       | (see Figure 15. Test circuit for inductive load switching and diode recovery times)                                              | -    | 0.7  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |                                                                                                                                  | -    | 8.9  |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 3.5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 60 \text{ V}$ ,<br>$T_J = 150 \text{ }^\circ\text{C}$ | -    | 190  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |                                                                                                                                  | -    | 0.8  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      | (see Figure 15. Test circuit for inductive load switching and diode recovery times)                                              | -    | 8.5  |      | A             |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

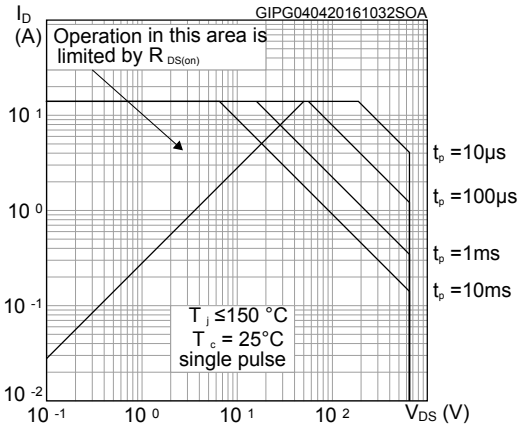


Figure 2. Thermal impedance

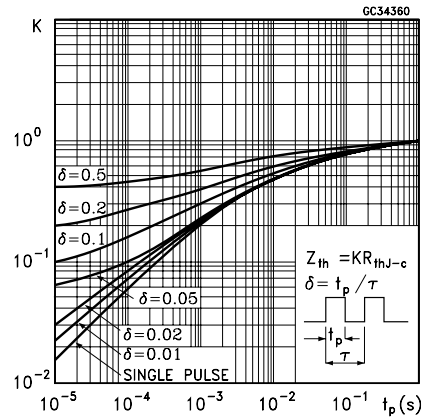


Figure 3. Output characteristics

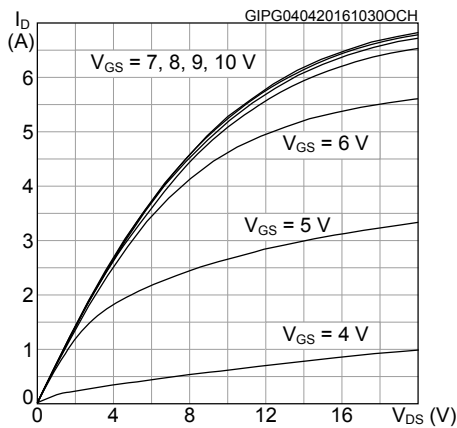


Figure 4. Transfer characteristics

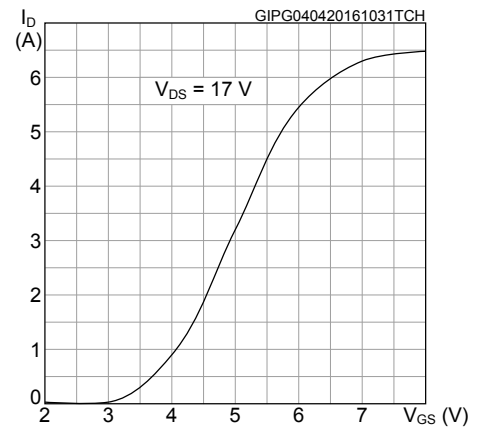


Figure 5. Gate charge vs gate-source voltage

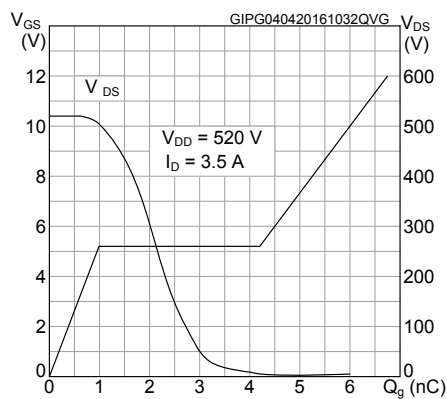
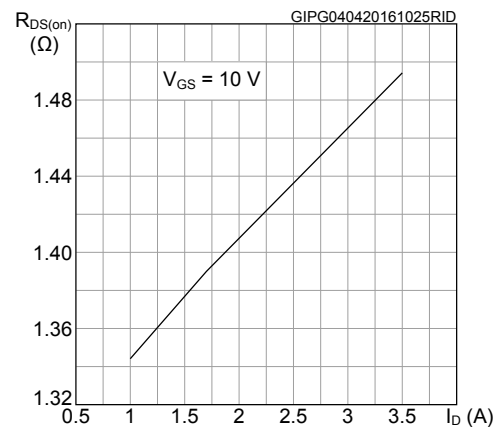
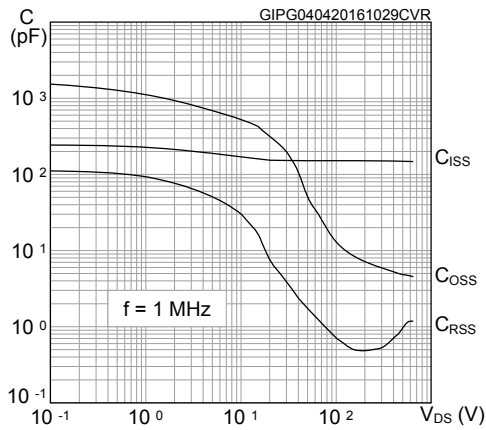


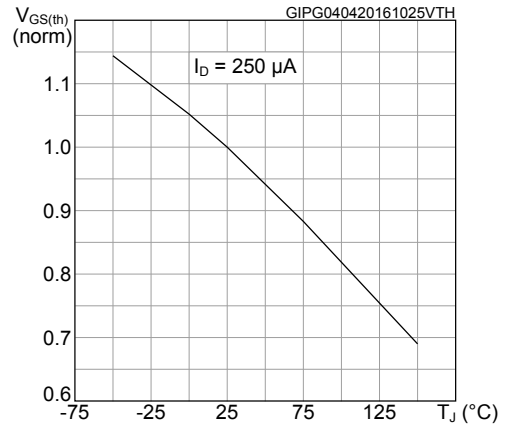
Figure 6. Static drain-source on-resistance



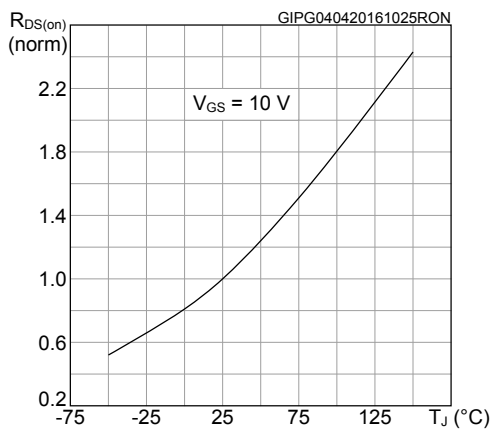
**Figure 7. Capacitance variations**



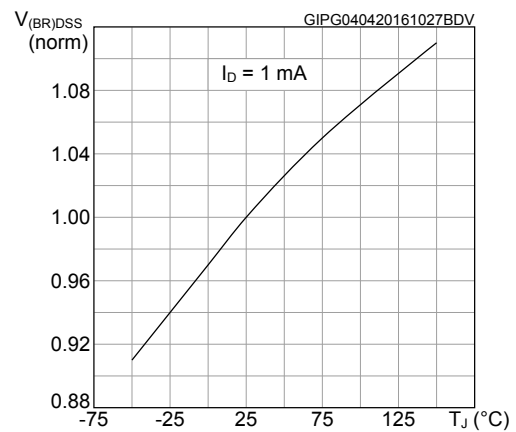
**Figure 8. Normalized gate threshold voltage vs temperature**



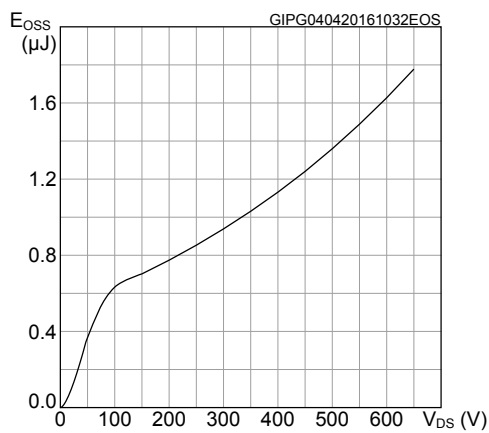
**Figure 9. Normalized on-resistance vs temperature**



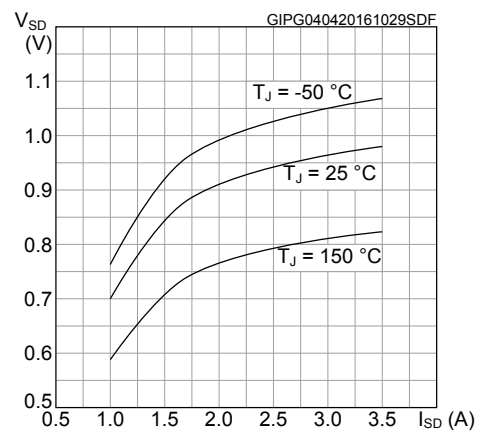
**Figure 10. Normalized V(BR)DSS vs temperature**



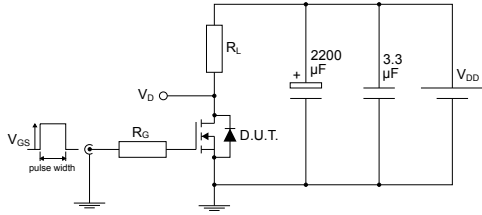
**Figure 11. Output capacitance stored energy**



**Figure 12. Source-drain diode forward characteristics**



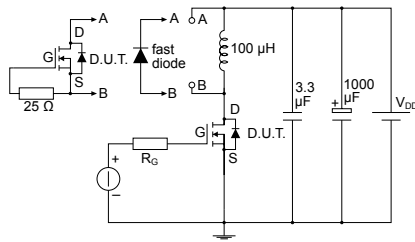
### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


AM01468v1

**Figure 14. Test circuit for gate charge behavior**


AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**


AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

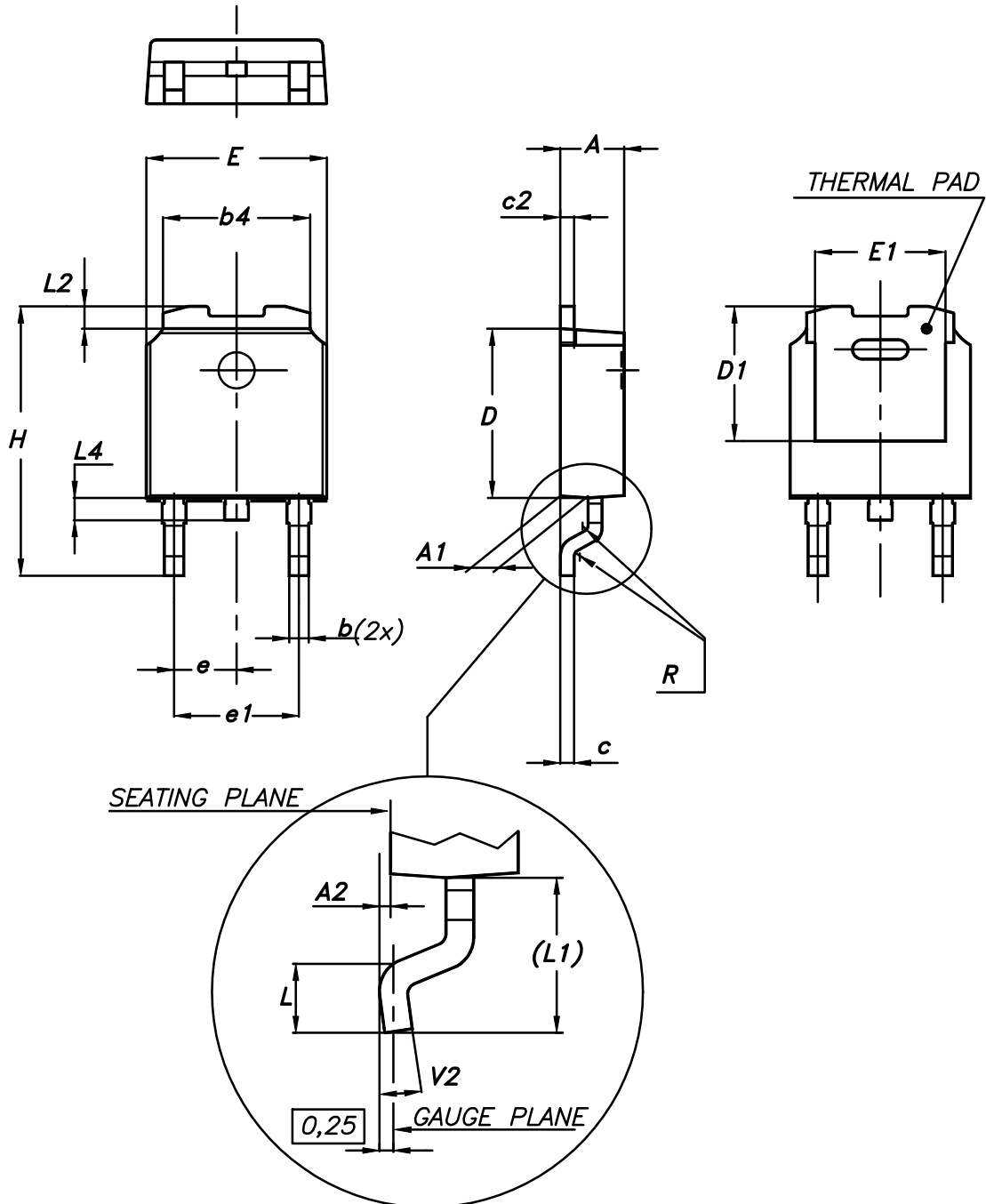
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



### 4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



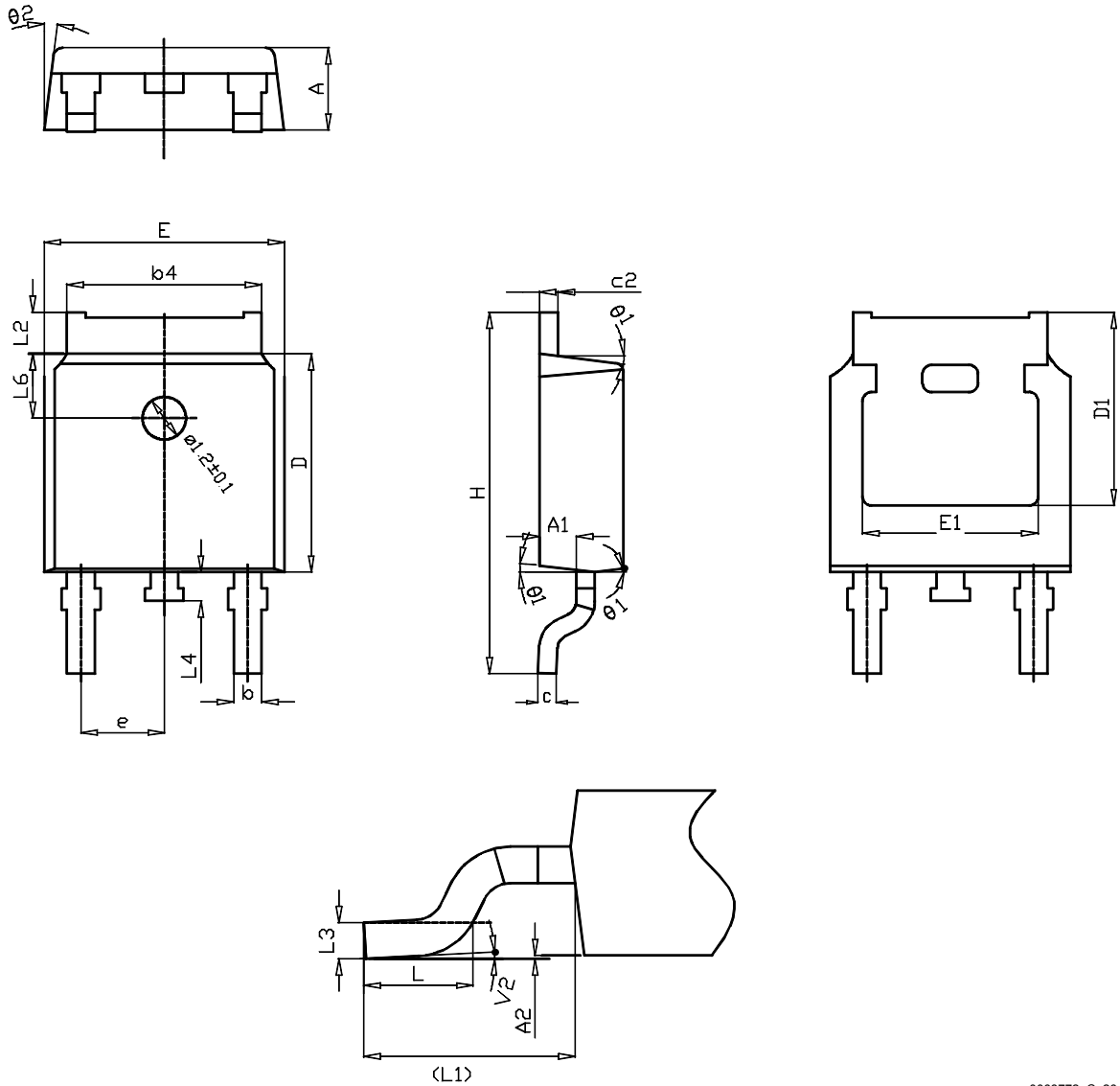
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**Table 8. DPAK (TO-252) type A mechanical data**

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    | 2.20  |       | 2.40  |
| A1   | 0.90  |       | 1.10  |
| A2   | 0.03  |       | 0.23  |
| b    | 0.64  |       | 0.90  |
| b4   | 5.20  |       | 5.40  |
| c    | 0.45  |       | 0.60  |
| c2   | 0.48  |       | 0.60  |
| D    | 6.00  |       | 6.20  |
| D1   | 4.95  | 5.10  | 5.25  |
| E    | 6.40  |       | 6.60  |
| E1   | 4.60  | 4.70  | 4.80  |
| e    | 2.159 | 2.286 | 2.413 |
| e1   | 4.445 | 4.572 | 4.699 |
| H    | 9.35  |       | 10.10 |
| L    | 1.00  |       | 1.50  |
| (L1) | 2.60  | 2.80  | 3.00  |
| L2   | 0.65  | 0.80  | 0.95  |
| L4   | 0.60  |       | 1.00  |
| R    |       | 0.20  |       |
| V2   | 0°    |       | 8°    |

## 4.2 DPAK (TO-252) type C package information

Figure 20. DPAK (TO-252) type C package outline

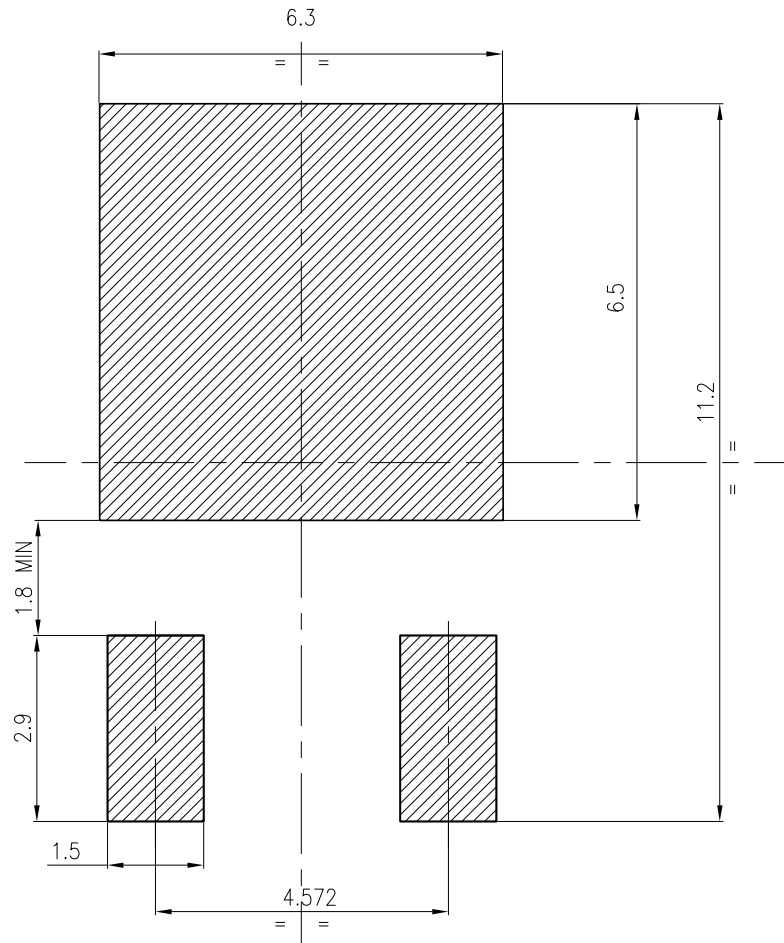


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**Table 9. DPAK (TO-252) type C mechanical data**

| Dim. | mm       |       |       |
|------|----------|-------|-------|
|      | Min.     | Typ.  | Max.  |
| A    | 2.20     | 2.30  | 2.38  |
| A1   | 0.90     | 1.01  | 1.10  |
| A2   | 0.00     |       | 0.10  |
| b    | 0.72     |       | 0.85  |
| b4   | 5.13     | 5.33  | 5.46  |
| c    | 0.47     |       | 0.60  |
| c2   | 0.47     |       | 0.60  |
| D    | 6.00     | 6.10  | 6.20  |
| D1   | 5.25     |       |       |
| E    | 6.50     | 6.60  | 6.70  |
| E1   | 4.70     |       |       |
| e    | 2.186    | 2.286 | 2.386 |
| H    | 9.80     | 10.10 | 10.40 |
| L    | 1.40     | 1.50  | 1.70  |
| L1   | 2.90 REF |       |       |
| L2   | 0.90     |       | 1.25  |
| L3   | 0.51 BSC |       |       |
| L4   | 0.60     | 0.80  | 1.00  |
| L6   | 1.80 BSC |       |       |
| θ1   | 5°       | 7°    | 9°    |
| θ2   | 5°       | 7°    | 9°    |
| V2   | 0°       |       | 8°    |

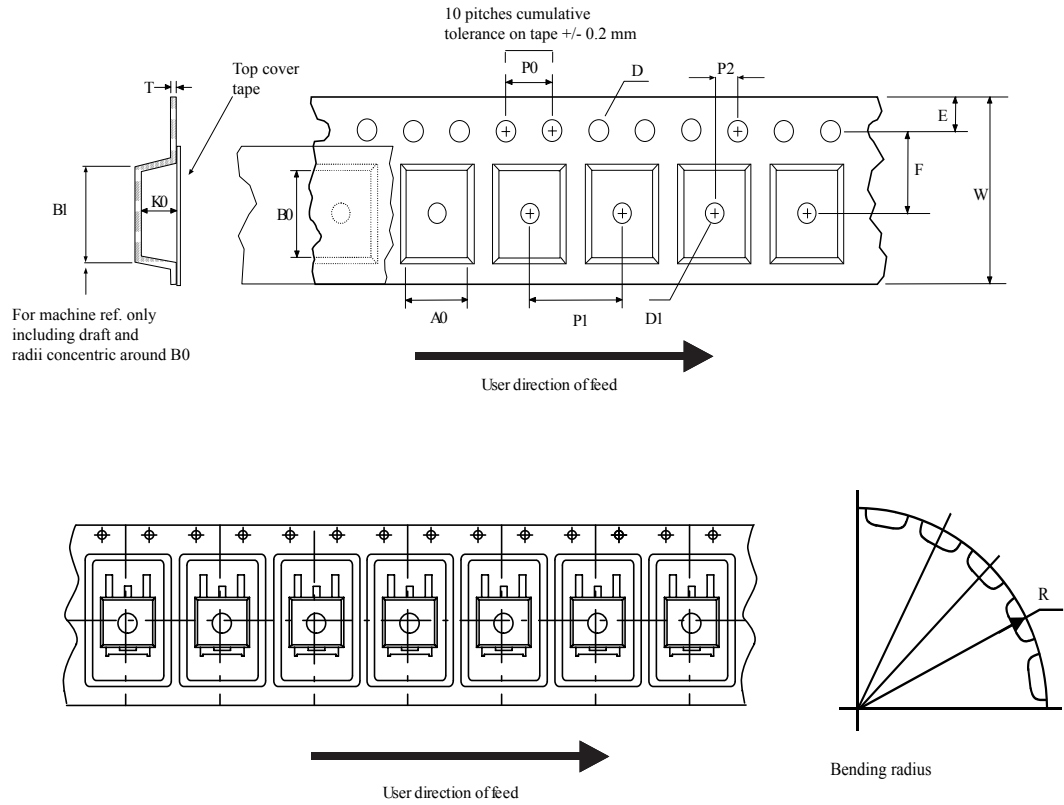
Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)



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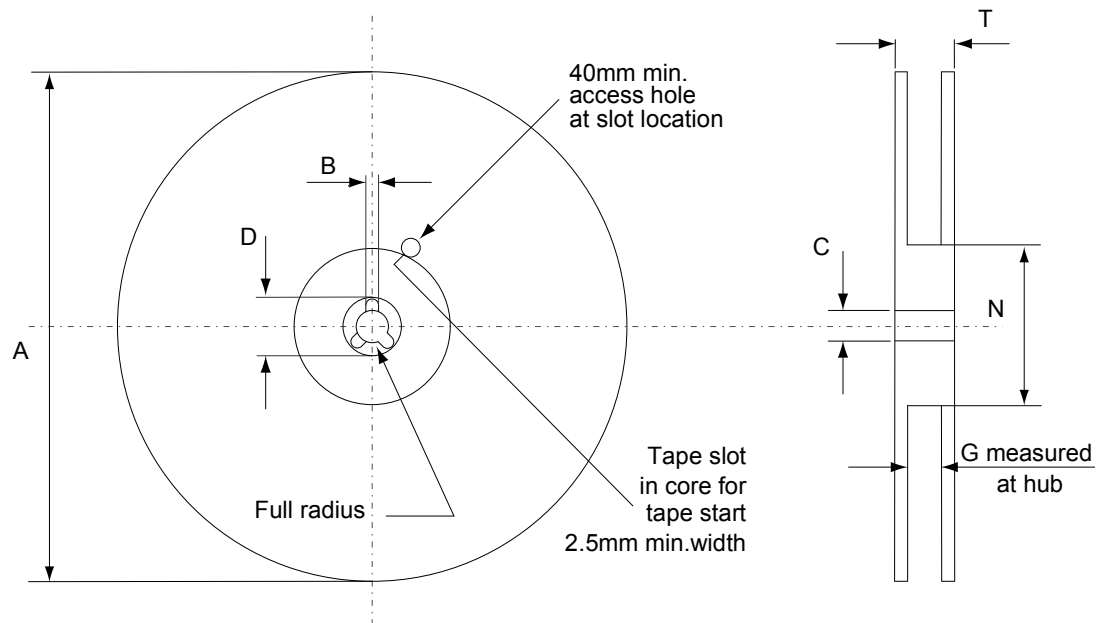
### 4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



AM08852v1

**Figure 23. DPAK (TO-252) reel outline**



AM06038v1

**Table 10. DPAK (TO-252) tape and reel mechanical data**

| Dim. | Tape |      | Dim. | Reel      |      |
|------|------|------|------|-----------|------|
|      | mm   |      |      | mm        |      |
|      | Min. | Max. |      | Min.      | Max. |
| A0   | 6.8  | 7    | A    |           | 330  |
| B0   | 10.4 | 10.6 | B    | 1.5       |      |
| B1   |      | 12.1 | C    | 12.8      | 13.2 |
| D    | 1.5  | 1.6  | D    | 20.2      |      |
| D1   | 1.5  |      | G    | 16.4      | 18.4 |
| E    | 1.65 | 1.85 | N    | 50        |      |
| F    | 7.4  | 7.6  | T    |           | 22.4 |
| K0   | 2.55 | 2.75 |      |           |      |
| P0   | 3.9  | 4.1  |      | Base qty. | 2500 |
| P1   | 7.9  | 8.1  |      | Bulk qty. | 2500 |
| P2   | 1.9  | 2.1  |      |           |      |
| R    | 40   |      |      |           |      |
| T    | 0.25 | 0.35 |      |           |      |
| W    | 15.7 | 16.3 |      |           |      |

## Revision history

**Table 11. Document revision history**

| Date        | Revision | Changes                                                                                                           |
|-------------|----------|-------------------------------------------------------------------------------------------------------------------|
| 02-May-2016 | 1        | Initial release.                                                                                                  |
| 22-Nov-2018 | 2        | Added <i>Section 4.2 DPAK (TO-252) type C package information</i> .<br>Minor text changes to improve readability. |
| 08-Jul-2019 | 3        | Updated <i>Section 4 Package information</i> .<br>Minor text changes.                                             |



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