

# MOSFET – N-Channel QFET®

600 V, 0.2 A, 11.5 Ω

## FQT1N60CTF-WS

### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

### Features

- 0.2 A, 600 V,  $R_{DS(on)} = 9.3 \Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 0.1 \text{ A}$
- Low Gate Charge (Typ. 4.8 nC)
- Low  $C_{rss}$  (Typ. 3.5 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS

( $T_C = 25^\circ\text{C}$  unless otherwise noted\*)

Symbol	Parameter	Value	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current Continuous ( $T_C = 25^\circ\text{C}$ ) Continuous ( $T_C = 100^\circ\text{C}$ )	0.2 0.12	A
$I_{DM}$	Drain Current – Pulsed (Note 1)	0.8	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	33	mJ
$I_{AR}$	Avalanche Current (Note 1)	0.2	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	0.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) Derate above $25^\circ\text{C}$	2.1 0.02	W W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	°C
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	°C

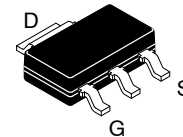
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2.  $L = 59 \text{ mH}$ ,  $I_{AS} = 1.1 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 0.2 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$ .

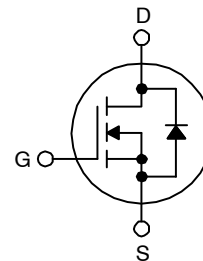


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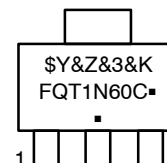
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SOT-223  
CASE 318H-01



### MARKING DIAGRAM



\$Y = ON Semiconductor Logo  
 &Z = Assembly Plant Code  
 &3 = 3-Digit Date Code Format  
 &K = 2-Digit Lot Run Traceability Code  
 FQT1N60C = Specific Device Code  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FQT1N60CTF-WS

## THERMAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient*	-	60	°C/W

\*When mounted on the minimum pad size recommended (PCB Mount)

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTIC

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^\circ C$	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu A$ , Referenced to 25°C	-	0.6	-	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 600 V, V_{GS} = 0 V$	-	-	25	$\mu A$
		$V_{DS} = 480 V, T_C = 125^\circ C$	-	-	250	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30 V, V_{DS} = 0 V$	-	-	±100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 10 V, I_D = 0.1 A$	-	9.3	11.5	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40 V, I_D = 0.1 A$ (Note 4)	-	0.75	-	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz$	-	130	170	pF
$C_{oss}$	Output Capacitance		-	19	25	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.5	6	pF
$Q_g$	Total Gate Charge at 10 V	$V_{DS} = 480 V, I_D = 1 A, V_{GS} = 10 V$ (Note 4 and 5)	-	4.8	6.2	nC
$Q_{gs}$	Gate to Source Gate Charge		-	0.7	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	2.7	-	nC

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 300 V, I_D = 1 A, R_G = 25 \Omega$ (Note 4 and 5)	-	7	24	ns
$t_r$	Turn-On Rise Time		-	21	52	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13	36	ns
$t_f$	Turn-Off Fall Time		-	27	64	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	0.2	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	0.8	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 V, I_{SD} = 0.2 A$	-	-	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 V, I_{SD} = 1 A, dI_F/dt = 100 A/\mu s$ (Note 4)	-	190	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	0.53	-	$\mu C$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse width  $\leq 300 \mu s$ , Duty Cycle  $\leq 2\%$ .
5. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

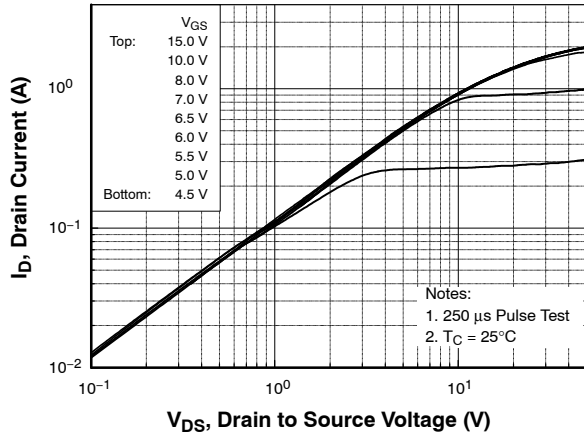


Figure 1. On-Region Characteristics

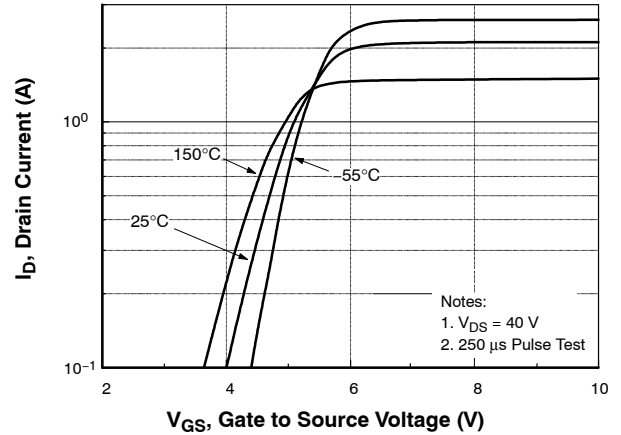


Figure 2. Transfer Characteristics

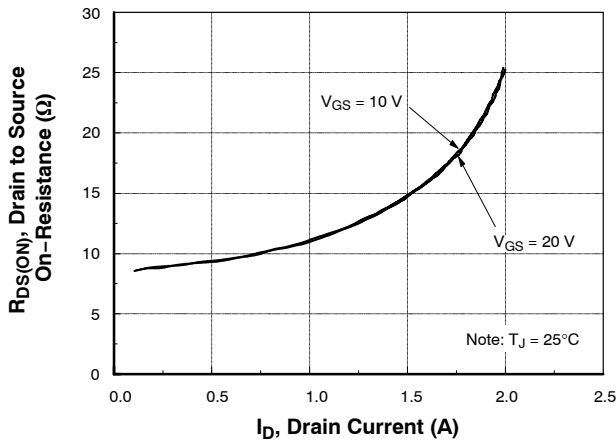


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

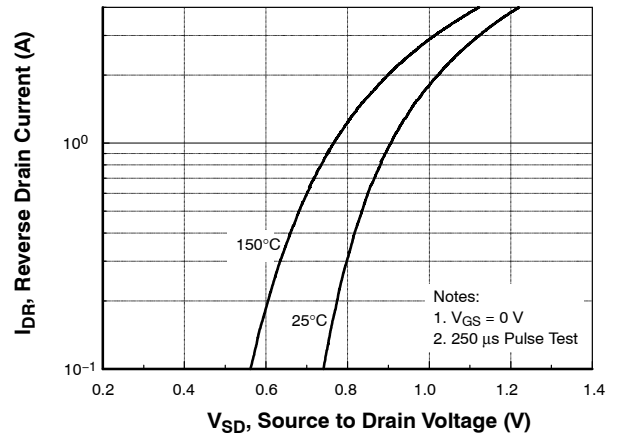


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

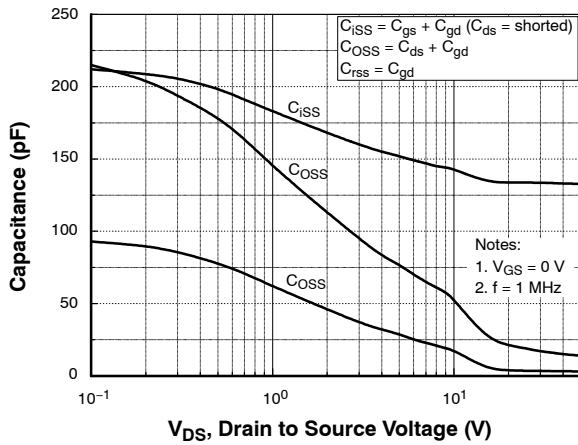


Figure 5. Capacitance Characteristics

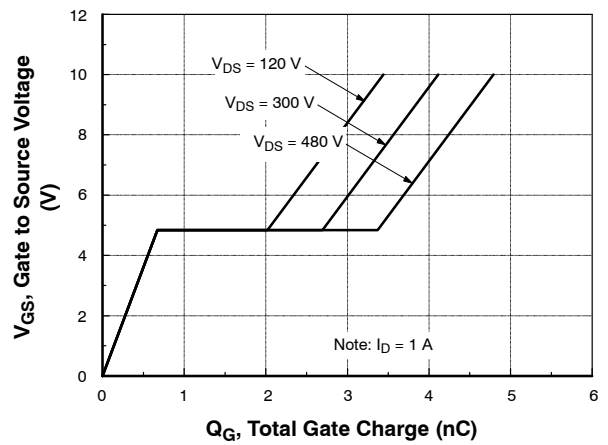


Figure 6. Gate Charge Characteristics

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## TYPICAL CHARACTERISTICS (Continued)

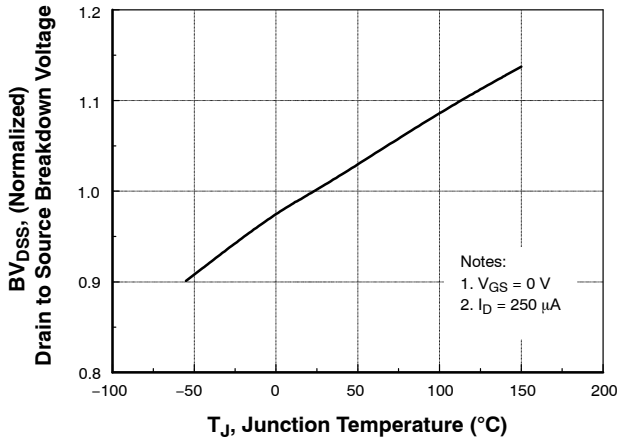


Figure 7. Breakdown Voltage Variation vs. Temperature

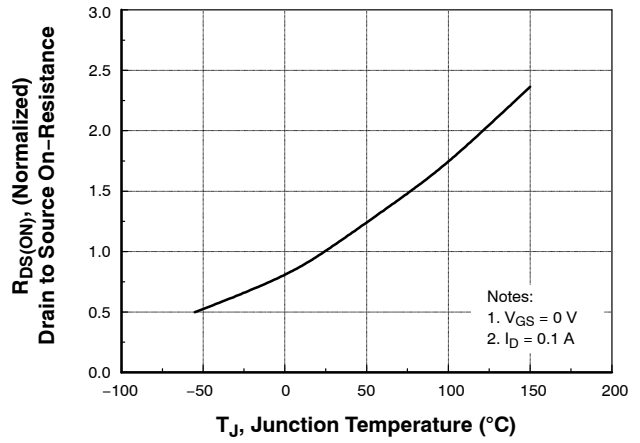


Figure 8. On-Resistance Variation vs. Temperature

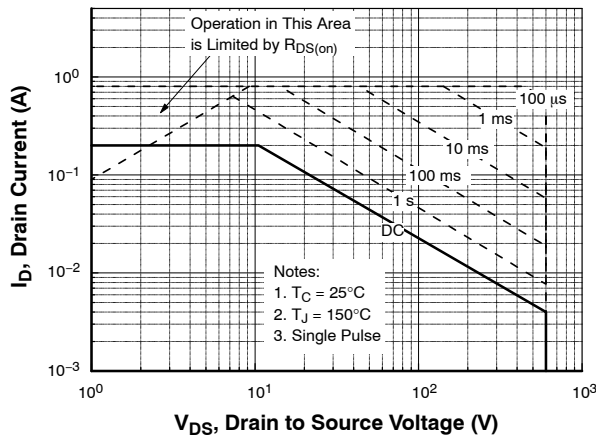


Figure 9. Maximum Safe Operating Area

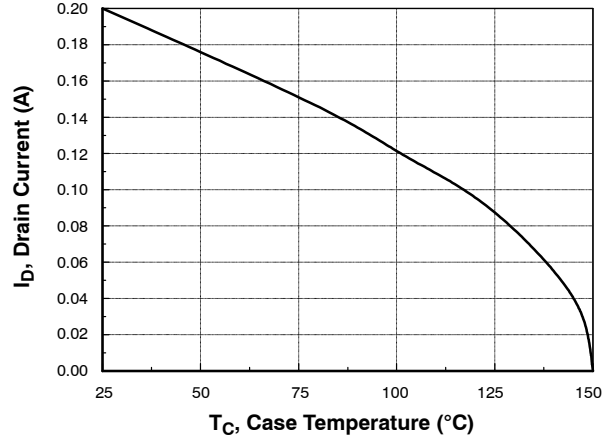


Figure 10. Maximum Drain Current vs. Case Temperature

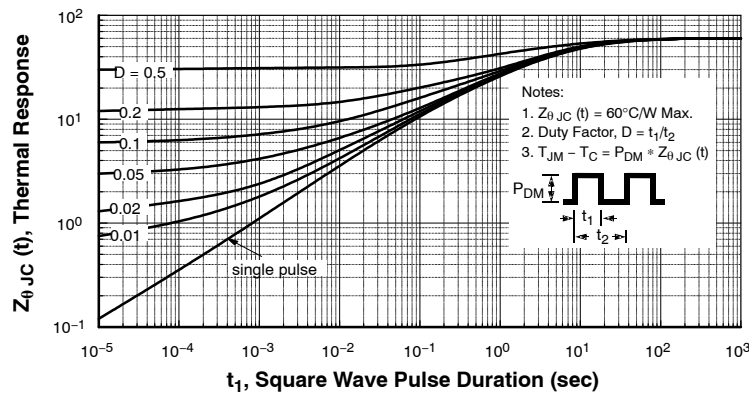


Figure 11. Transient Thermal Response Curve

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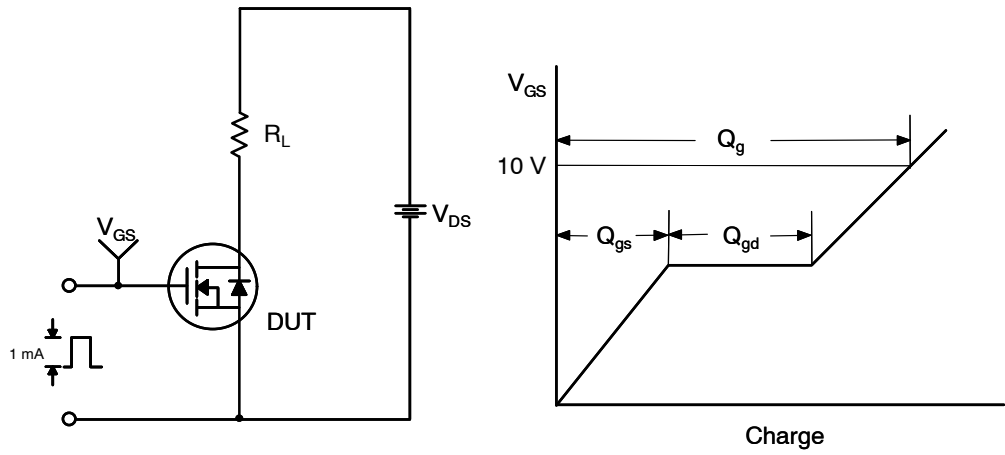


Figure 12. Gate Charge Test Circuit & Waveforms

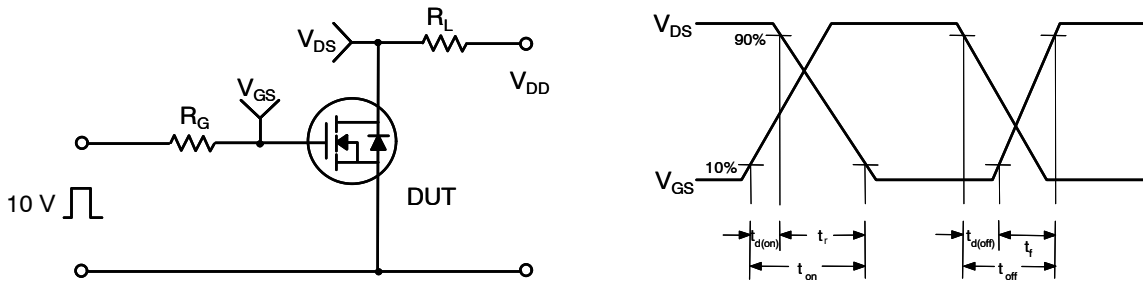


Figure 13. Resistive Switching Test Circuit & Waveforms

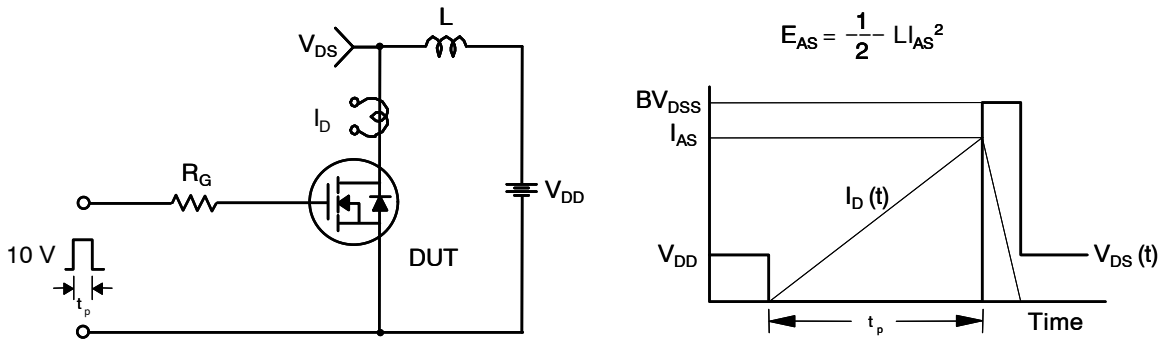


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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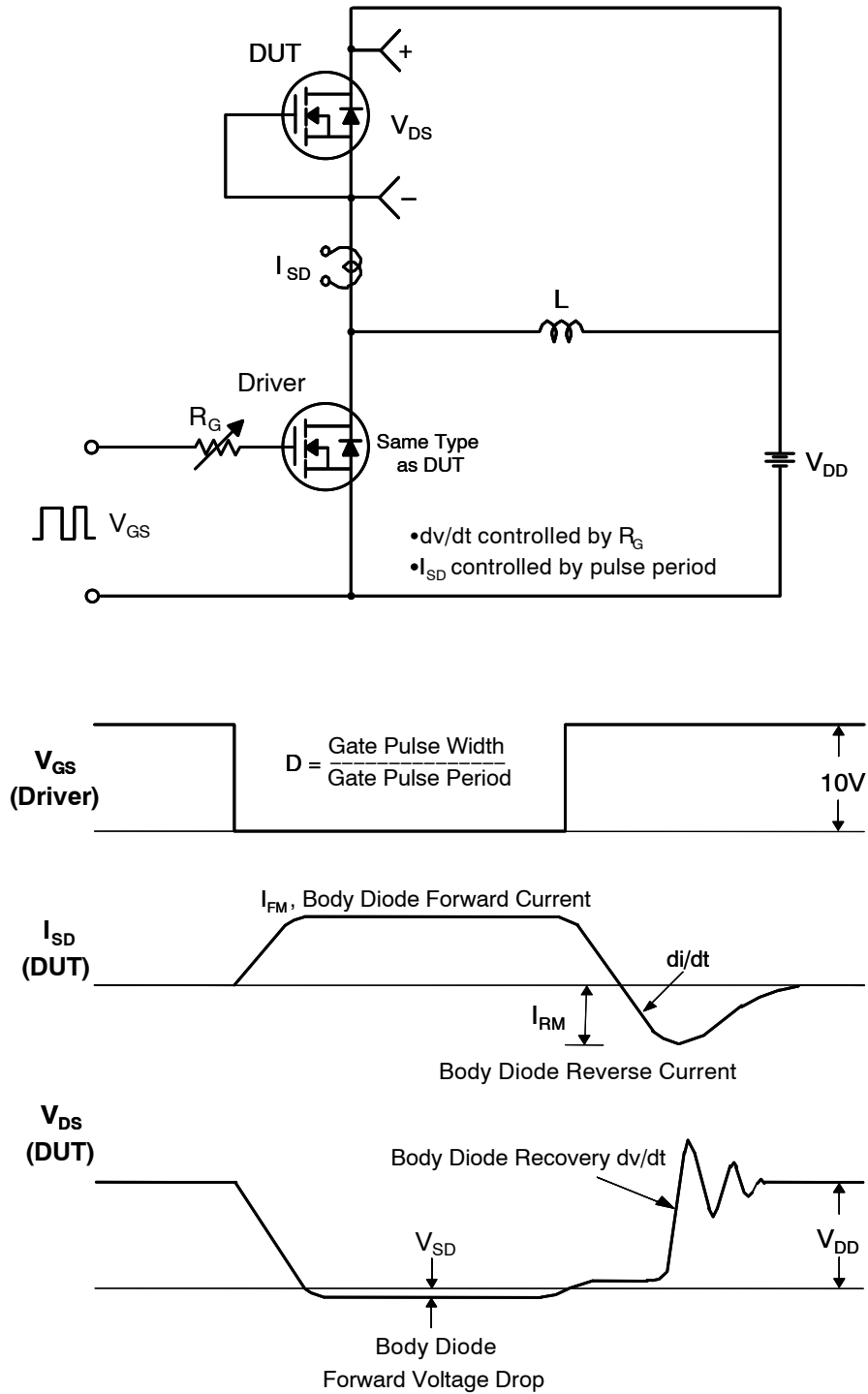


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQT1N60C	FQT1N60CTF-WS	SOT-223	330 mm	12 mm	4000

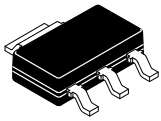
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

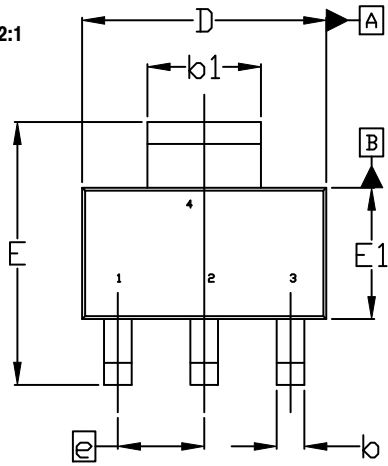
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CASE 318H  
ISSUE B

DATE 13 MAY 2020

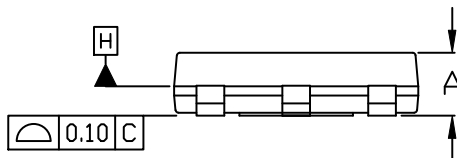
SCALE 2:1



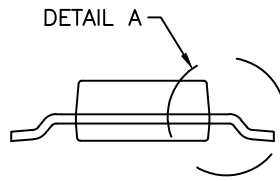
TOP VIEW

$\Phi 0.10 \text{ (M)}$  C A B

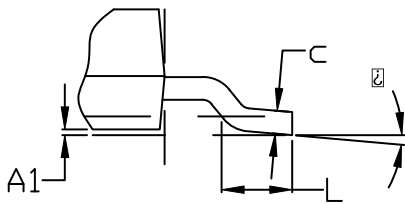
NOTE 7



SIDE VIEW

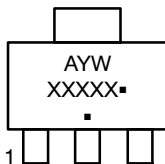


END VIEW



DETAIL A

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

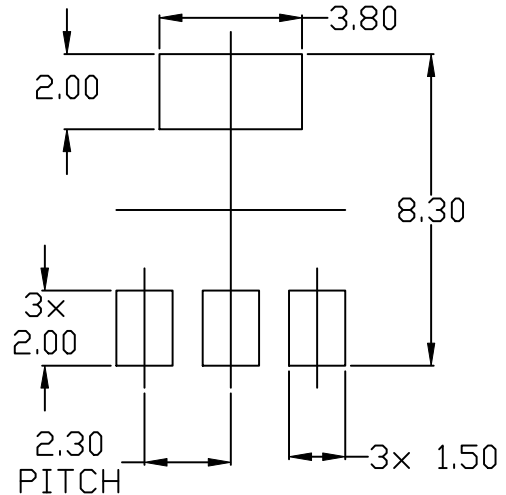
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
∠	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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