

NL17SH08

Single 2-Input AND Gate

The NL17SH08 is an advanced high speed CMOS 2-input AND gate fabricated with silicon gate CMOS technology.

The internal circuit is composed of multiple stages, including a buffer output which provides high noise immunity and stable output.

The NL17SH08 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the NL17SH08 to be used to interface 5.0 V circuits to 3.0 V circuits.

Features

- High Speed: $t_{PD} = 3.5 \text{ ns}$ (Typ) at $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation: $I_{CC} = 1.0 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- These are Pb-Free Devices

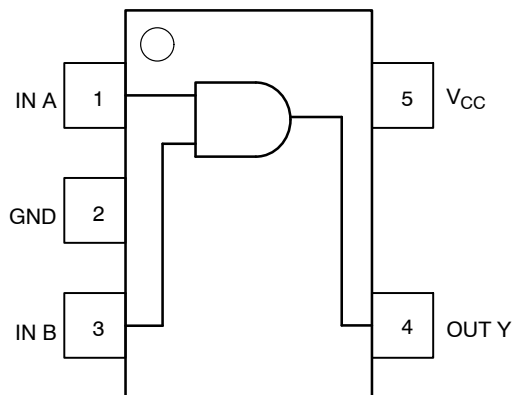


Figure 1. Pinout (Top View)

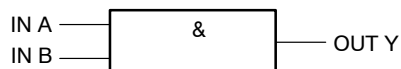


Figure 2. Logic Symbol



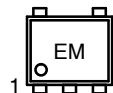
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MARKING DIAGRAM



SOT-953
CASE 527AE



E = Specific Device Code
M = Month Code

PIN ASSIGNMENT

| | |
|---|---------------|
| 1 | IN A |
| 2 | GND |
| 3 | IN B |
| 4 | OUT \bar{Y} |
| 5 | V_{CC} |

FUNCTION TABLE

| Inputs | | Output |
|--------|---|--------|
| A | B | Y |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|---|---|------------|
| V _{CC} | DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | DC Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V |
| I _{IK} | DC Input Diode Current | -20 | mA |
| I _{OK} | DC Output Diode Current | ±20 | mA |
| I _{OUT} | DC Output Sink Current | ±25 | mA |
| I _{CC} | DC Supply Current per Supply Pin | 50 | mA |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| T _L | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |
| T _J | Junction Temperature Under Bias | +150 | °C |
| P _D | Power Dissipation in Still Air | 50 | mW |
| MSL | Moisture Sensitivity | Level 1 | |
| F _R | Flammability Rating | Oxygen Index: 28 to 34 UL 94 V-0 @ 0.125 in | |
| I _{LATCHUP} | Latchup Performance | Above V _{CC} and Below GND at 125°C (Note 1) | ±100 mA |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|---------------------------------|-----|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V _{IN} | DC Input Voltage | 0.0 | 5.5 | V |
| V _{OUT} | DC Output Voltage | 0.0 | V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise and Fall Time | 0 | 100 | ns/V |
| | V _{CC} = 3.3 V ± 0.3 V | 0 | 20 | |
| | V _{CC} = 5.0 V ± 0.5 V | | | |

Device Junction Temperature versus Time to 0.1% Bond Failures

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

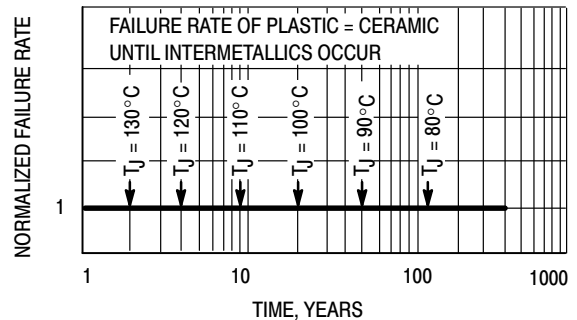


Figure 3. Failure Rate vs. Time Junction Temperature

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A ≤ 85°C | | -55°C to 125°C | | Unit |
|-----------------|---|--|--------------------------|----------------------------|-------------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 2.0 3.0 4.5 5.5 | 1.5 2.1 3.15 3.85 | | | 1.5 2.1 3.15 3.85 | | 1.5 2.1 3.15 3.85 | V | |
| V _{IL} | Maximum Low-Level Input Voltage | | 2.0 3.0 4.5 5.5 | | | 0.5 0.9 1.35 1.65 | | 0.5 0.9 1.35 1.65 | | 0.5 0.9 1.35 1.65 | V |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = -50 μA | 2.0 3.0 4.5 | 1.9 2.9 4.4 | 2.0 3.0 4.5 | | 1.9 2.9 4.4 | | 1.9 2.9 4.4 | | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA I _{OH} = -8 mA | 3.0 4.5 | 2.58 3.94 | | | 2.48 3.80 | | 2.34 3.66 | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 3.0 4.5 | | 0.0 0.0 0.0 | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | | 0.1 0.1 0.1 | V |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 4.5 | | | 0.36 0.36 | | 0.44 0.44 | | 0.52 0.52 | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 1.0 | | 10 | | 40 | μA |

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A ≤ 85°C | | -55 ≤ T _A ≤ 125°C | | Unit |
|--|---|--|-----------------------|------------|-------------|-----------------------|--------------|------------------------------|--------------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, Input A or B to Y | V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF | | 4.1 5.9 | 8.8 12.3 | | 10.5 14.0 | | 12.5 16.5 | ns |
| | | V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF | | 3.5 4.2 | 5.9 7.9 | | 7.0 9.0 | | 9.0 11.0 | |
| C _{IN} | Maximum Input Capacitance | | | 5.5 | 10 | | 10 | | 10 | pF |

| | | | | |
|-----------------|--|---|--|----|
| C _{PD} | Power Dissipation Capacitance (Note 2) | Typical @ 25°C, V _{CC} = 5.0 V | | pF |
| | | 11 | | |

2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NL17SH08

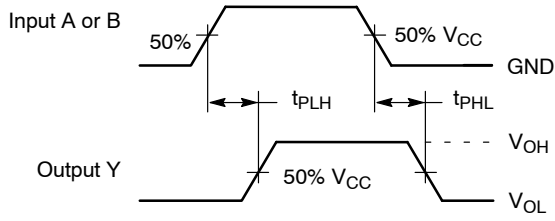
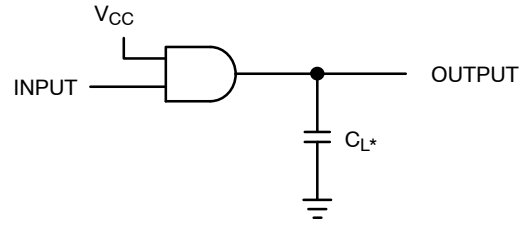


Figure 4. Switching Waveforms



*Includes all probe and jig capacitance.
A 1-MHz square input wave is recommended for propagation delay tests.

Figure 5. Test Circuit

DEVICE ORDERING INFORMATION

| Device | Package | Shipping [†] |
|---------------|----------------------|-----------------------|
| NL17SH08P5T5G | SOT-953 (Pb-Free) | 8000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

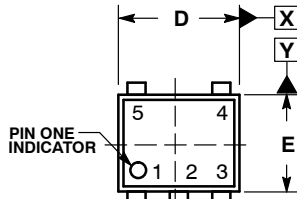
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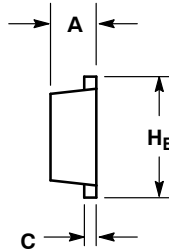
SCALE 4:1

SOT-953
CASE 527AE
ISSUE E

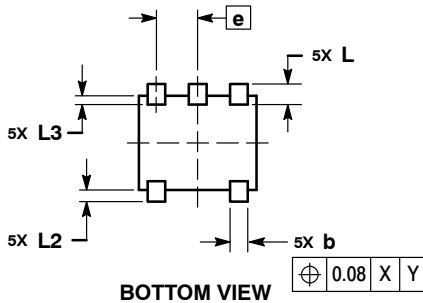
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TOP VIEW

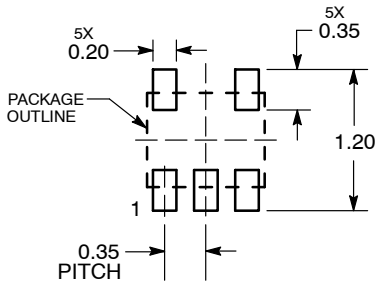


SIDE VIEW



BOTTOM VIEW

SOLDERING FOOTPRINT*



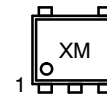
DIMENSIONS: MILLIMETERS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS | | |
|----------------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| C | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H _E | 0.95 | 1.00 | 1.05 |
| L | 0.175 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |
| L3 | --- | --- | 0.15 |

GENERIC MARKING DIAGRAM*



- X = Specific Device Code
- M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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