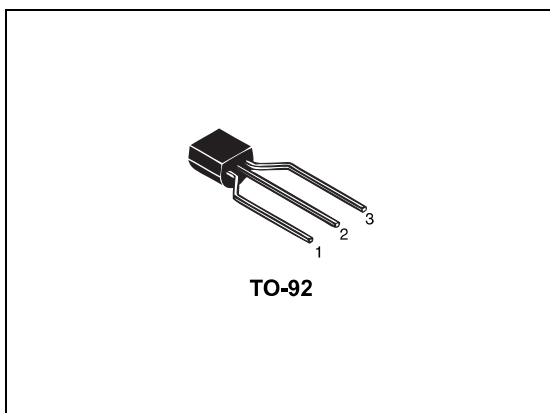
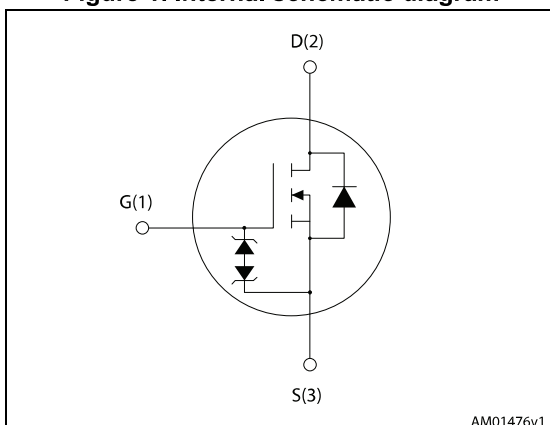


## N-channel 600 V, 6.7 $\Omega$ typ., 0.4 A SuperMESH3™ Power MOSFET in a TO-92 package

Datasheet – production data



**Figure 1. Internal schematic diagram**



### Features

| Order code    | $V_{DS}$ | $R_{DS(on)max}$ | $I_D$ | $P_{TOT}$ |
|---------------|----------|-----------------|-------|-----------|
| STQ1HN60K3-AP | 600 V    | 8 $\Omega$      | 0.4 A | 3 W       |

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics' SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

**Table 1. Device summary**

| Order code    | Marking | Package | Packaging |
|---------------|---------|---------|-----------|
| STQ1HN60K3-AP | 1HN60K3 | TO-92   | Ammopack  |

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter  | Value      | Unit             |
|----------------|--|------------|------------------|
| $V_{DS}$       | Drain- source voltage  | 600        | V                |
| $V_{GS}$       | Gate- source voltage   | $\pm 30$   | V                |
| $I_D^{(1)}$    | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$   | 0.4        | A                |
| $I_D^{(1)}$    | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$  | 0.25       | A                |
| $I_{DM}^{(2)}$ | Drain current (pulsed)   | 1.60       | A                |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$  | 3          | W                |
| $I_{AR}$       | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)                                   | 1.2        | A                |
| $E_{AS}$       | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 60         | mJ               |
| $dv/dt^{(3)}$  | Peak diode recovery voltage slope  | 5          | V/ns             |
| $T_J$          | Operating junction temperature   | -55 to 150 | $^\circ\text{C}$ |
| $T_{stg}$      | Storage temperature  |            | $^\circ\text{C}$ |

1. Current limited by package power capability
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 1.2\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 3. Thermal data**

| Symbol         | Parameter                             | Value | Unit                      |
|----------------|---------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max. | 42    | $^\circ\text{C}/\text{W}$ |

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

| Symbol                      | Parameter   | Test conditions  | Min. | Typ. | Max.     | Unit                           |
|-----------------------------|---|--|------|------|----------|--------------------------------|
| $V_{(\text{BR})\text{DSS}}$ | Drain-source breakdown voltage                          | $I_D = 1\text{ mA}$ , $V_{\text{GS}} = 0$  | 600  |      |          | V                              |
| $I_{\text{DSS}}$            | Zero gate voltage drain current ( $V_{\text{GS}} = 0$ ) | $V_{\text{DS}} = 600\text{ V}$<br>$V_{\text{DS}} = 600\text{ V}$ , $T_C = 125\text{ °C}$ |      |      | 1<br>50  | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{\text{GSS}}$            | Gate-body leakage current ( $V_{\text{DS}} = 0$ )       | $V_{\text{GS}} = \pm 20\text{ V}$  |      |      | $\pm 10$ | $\mu\text{A}$                  |
| $V_{\text{GS(th)}}$         | Gate threshold voltage                                  | $V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 50\text{ }\mu\text{A}$                          | 2    | 3.75 | 4.5      | V                              |
| $R_{\text{DS(on)}}$         | Static drain-source on-resistance                       | $V_{\text{GS}} = 10\text{ V}$ , $I_D = 0.6\text{ A}$                                     |      | 6.7  | 8        | $\Omega$                       |

**Table 5. Dynamic**

| Symbol                   | Parameter                             | Test conditions  | Min. | Typ. | Max. | Unit     |
|--------------------------|---------------------------------------|--|------|------|------|----------|
| $C_{\text{iss}}$         | Input capacitance                     | $V_{\text{DS}} = 50\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{\text{GS}} = 0$  | -    | 140  | -    | pF       |
| $C_{\text{oss}}$         | Output capacitance                    |  | -    | 13   | -    | pF       |
| $C_{\text{rss}}$         | Reverse transfer capacitance          |  | -    | 2    | -    | pF       |
| $C_{\text{o(tr)}}^{(1)}$ | Equivalent capacitance time related   | $V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0$   | -    | 9    | -    | pF       |
| $C_{\text{o(tr)}}^{(2)}$ | Equivalent capacitance energy related |  | -    | 6    | -    | pF       |
| $R_g$                    | Gate input resistance                 | $f = 1\text{ MHz}$ open drain  | -    | 10   | -    | $\Omega$ |
| $Q_g$                    | Total gate charge                     | $V_{\text{DD}} = 480\text{ V}$ , $I_D = 1.2\text{ A}$ ,<br>$V_{\text{GS}} = 10\text{ V}$<br><i>(see Figure 16)</i> | -    | 9.5  | -    | nC       |
| $Q_{\text{gs}}$          | Gate-source charge                    |  | -    | 1.5  | -    | nC       |
| $Q_{\text{gd}}$          | Gate-drain charge                     |  | -    | 6.5  | -    | nC       |

- $C_{\text{o(tr)}}^{(1)}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DS}}$
- $C_{\text{o(tr)}}^{(2)}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DS}}$

Table 6. Switching times

| Symbol       | Parameter           | Test conditions   | Min. | Typ. | Max | Unit |
|--------------|---------------------|---|------|------|-----|------|
| $t_{d(on)}$  | Turn-on delay time  | $V_{DD} = 300 \text{ V}$ , $I_D = 0.6 \text{ A}$ ,<br>$R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$<br>(see Figure 10) | -    | 7    | -   | ns   |
| $t_r$        | Rise time           |   | -    | 10   | -   | ns   |
| $t_{d(off)}$ | Turn-off-delay time |   | -    | 23   | -   | ns   |
| $t_f$        | Fall time           |   | -    | 31   | -   | ns   |

Table 7. Source drain diode

| Symbol          | Parameter                     | Test conditions   | Min. | Typ. | Max | Unit |
|-----------------|-------------------------------|---|------|------|-----|------|
| $I_{SD}$        | Source-drain current          |   | -    |      | 0.4 | A    |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |   | -    |      | 1.6 | A    |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 1.2 \text{ A}$ , $V_{GS} = 0$   | -    |      | 1.6 | V    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 1.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 60 \text{ V}$<br>(see Figure 11)                                    | -    | 180  |     | ns   |
| $Q_{rr}$        | Reverse recovery charge       |   | -    | 500  |     | nC   |
| $I_{RRM}$       | Reverse recovery current      |   | -    | 5.6  |     | A    |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 1.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 60 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$<br>(see Figure 11) | -    | 200  |     | ns   |
| $Q_{rr}$        | Reverse recovery charge       |   | -    | 570  |     | nC   |
| $I_{RRM}$       | Reverse recovery current      |   | -    | 6    |     | A    |

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 8. Gate-source Zener diode

| Symbol        | Parameter                     | Test conditions                         | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0$ | 30   | -    | -    | V    |

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

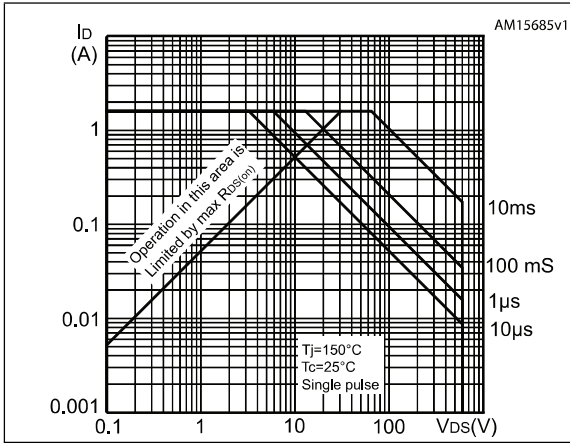


Figure 3. Thermal impedance

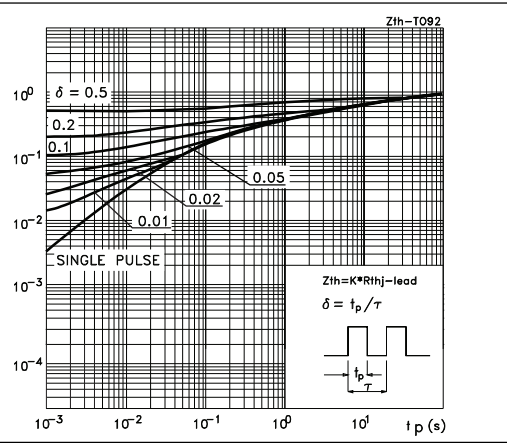


Figure 4. Output characteristics

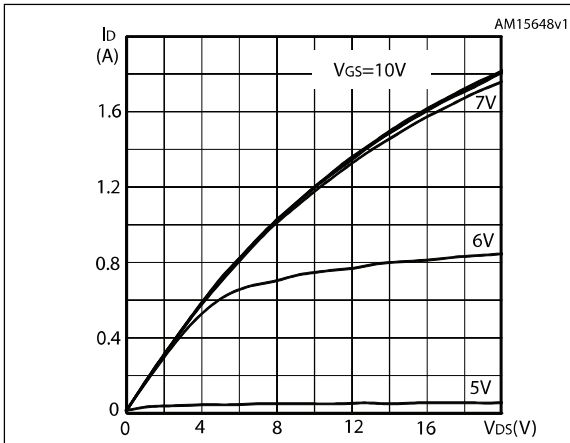


Figure 5. Transfer characteristics

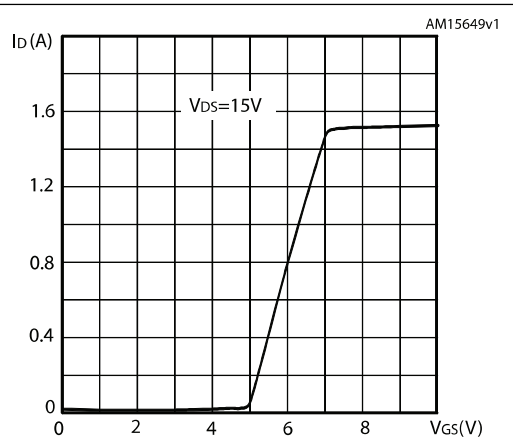


Figure 6. Normalized  $B_{V_{DS}}$  vs temperature

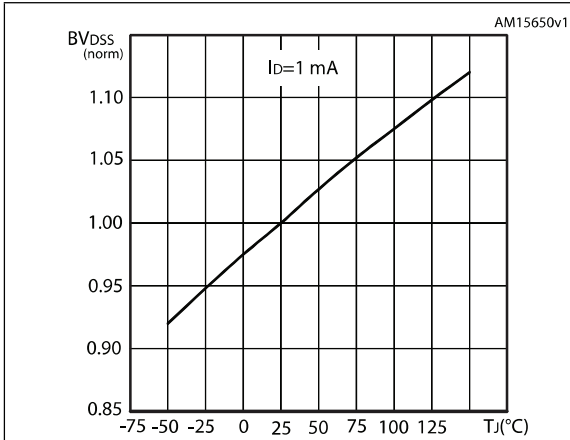


Figure 7. Static drain-source on-resistance

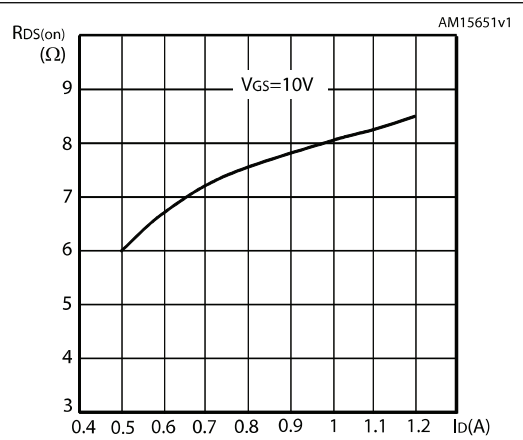


Figure 8. Gate charge vs gate-source voltage

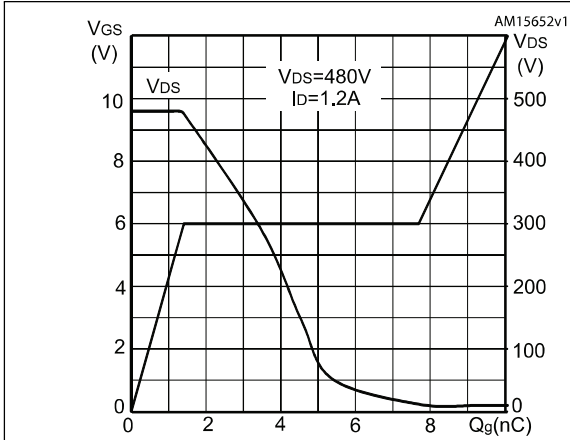


Figure 9. Capacitance variations

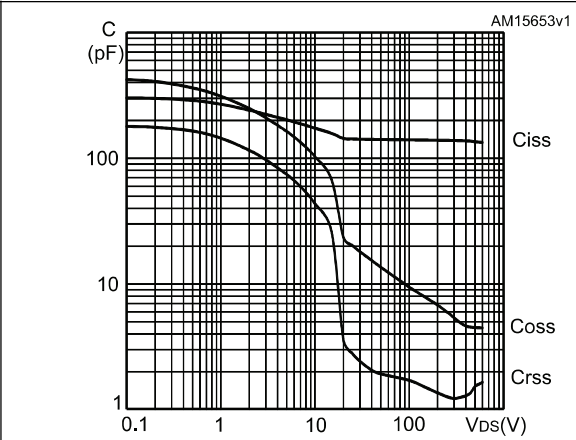


Figure 10. Normalized gate threshold voltage vs temperature

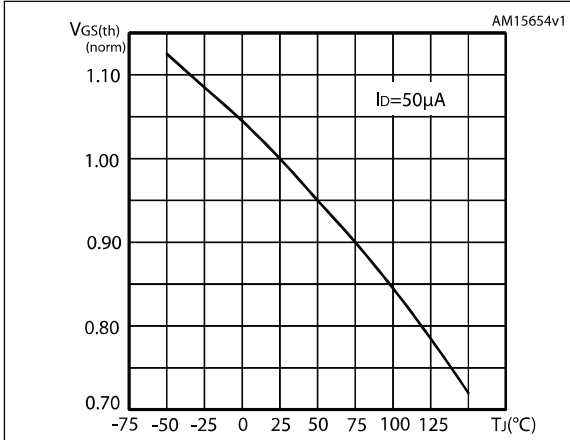


Figure 11. Normalized on-resistance vs temperature

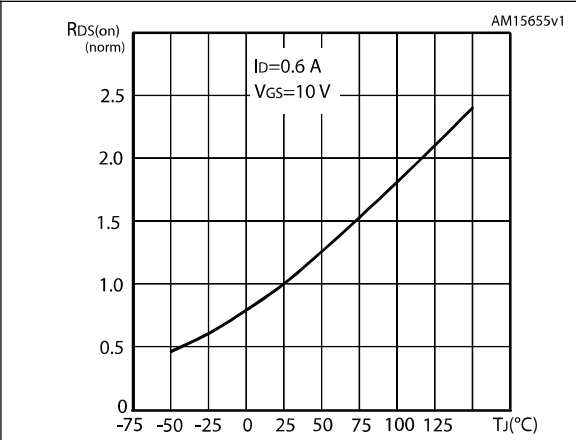


Figure 12. Source-drain diode forward characteristics

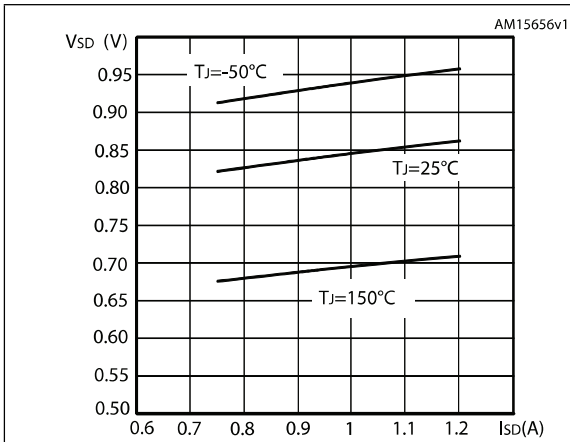


Figure 13. Output capacitance stored energy

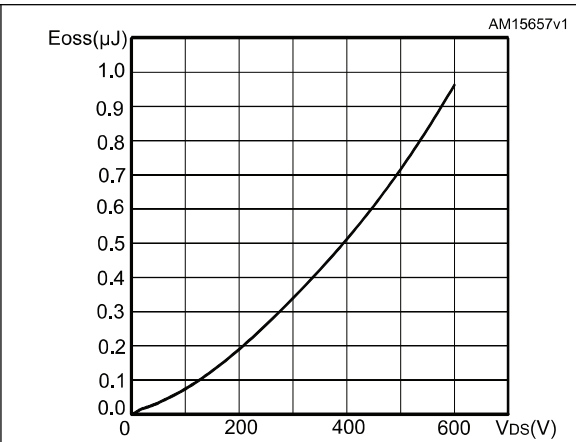
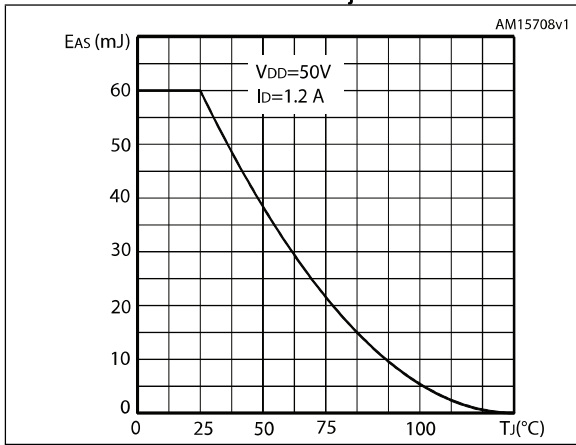


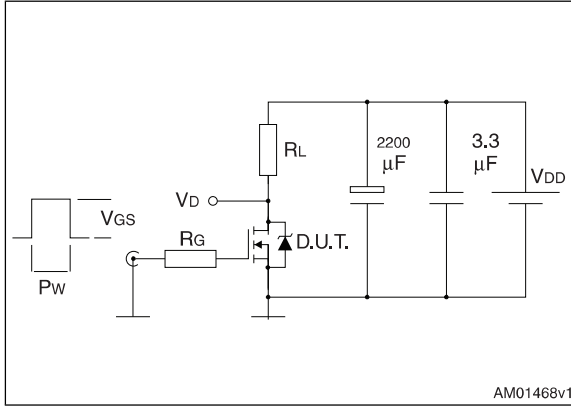
Figure 14. Maximum avalanche energy vs. starting  $T_j$





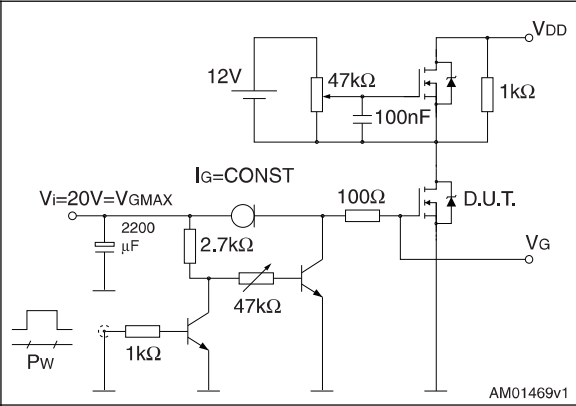
### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



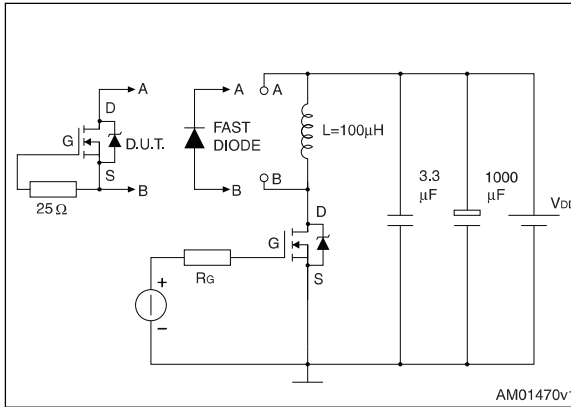
AM01468v1

Figure 16. Gate charge test circuit



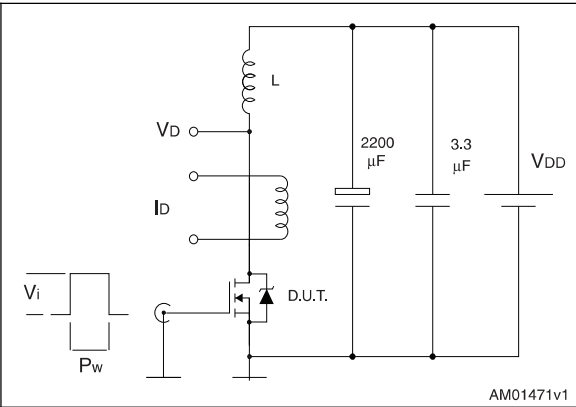
AM01469v1

Figure 17. Test circuit for inductive load switching and diode recovery times



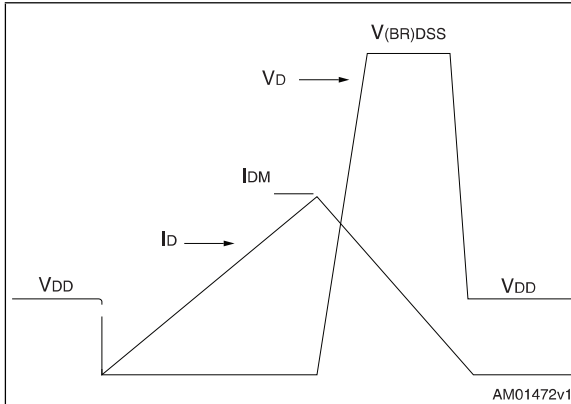
AM01470v1

Figure 18. Unclamped inductive load test circuit



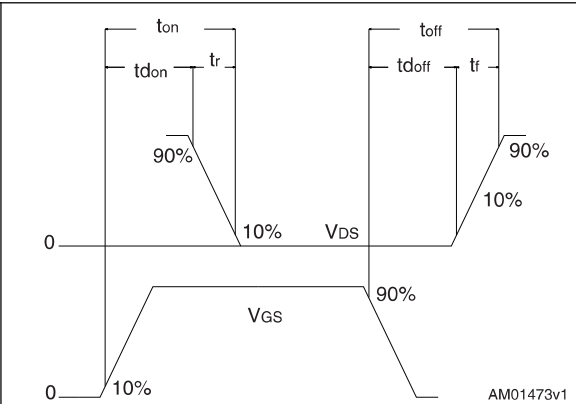
AM01471v1

Figure 19. Unclamped inductive waveform



AM01472v1

Figure 20. Switching time waveform



AM01473v1

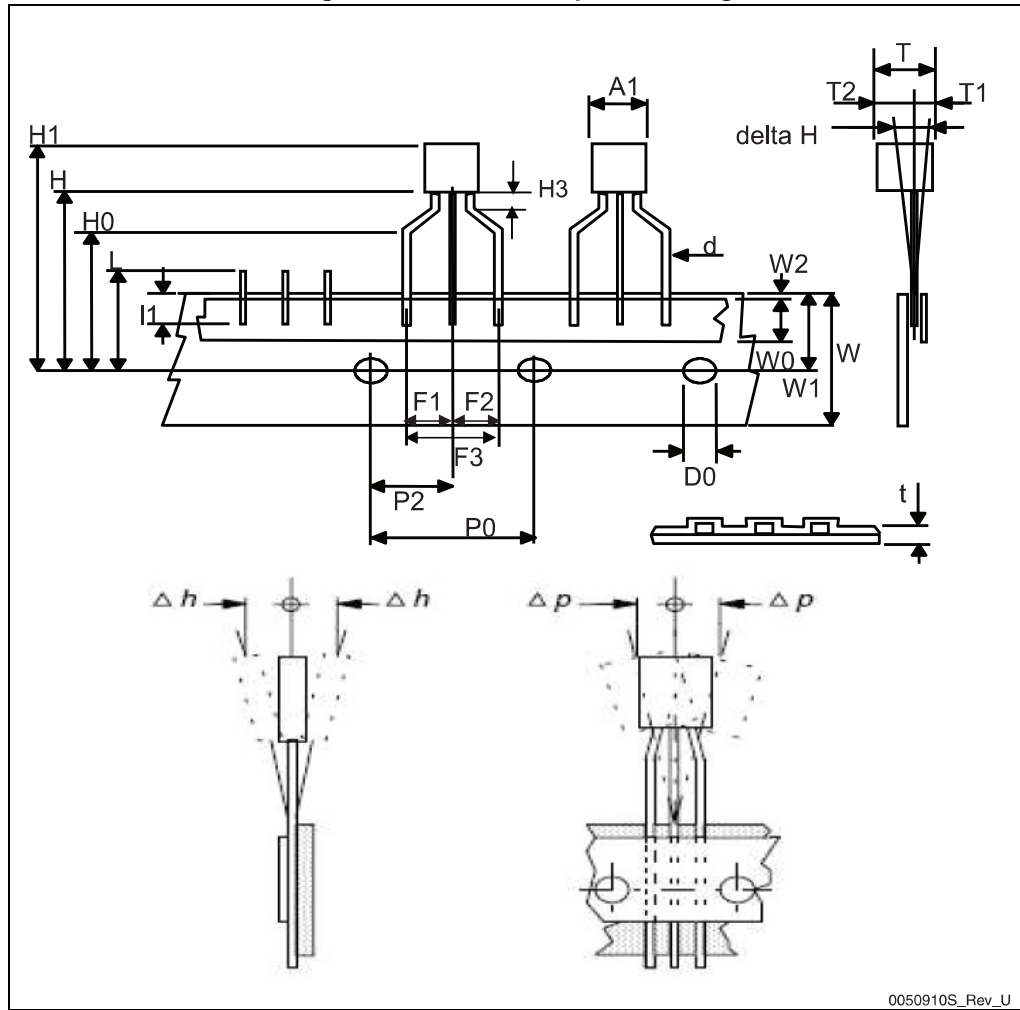
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. TO-92 ammopack mechanical data

| Dim.    | mm    |       |       |
|---------|-------|-------|-------|
|         | Min.  | Typ.  | Max.  |
| A1      |       |       | 4.80  |
| T       |       |       | 3.80  |
| T1      |       |       | 1.60  |
| T2      |       |       | 2.30  |
| d       | 0.45  | 0.47  | 0.48  |
| P0      | 12.50 | 12.70 | 12.90 |
| P2      | 5.65  | 6.35  | 7.05  |
| F1, F2  | 2.40  | 2.50  | 2.94  |
| F3      | 4.98  | 5.08  | 5.48  |
| delta H | -2.00 |       | 2.00  |
| W       | 17.50 | 18.00 | 19.00 |
| W0      | 5.50  | 6.00  | 6.50  |
| W1      | 8.50  | 9.00  | 9.25  |
| W2      |       |       | 0.50  |
| H       |       | 18.50 | 21.00 |
| H0      | 15.50 | 16.00 | 18.20 |
| H1      |       | 25.00 | 27.00 |
| H3      | 0.50  | 1.00  | 2.00  |
| D0      | 3.80  | 4.00  | 4.20  |
| t       |       |       | 0.90  |
| L       |       |       | 11.00 |
| l1      | 3.00  |       |       |
| delta P | -1.00 |       | 1.00  |

Figure 21. TO-92 ammopack drawing



0050910S\_Rev\_U

## 5 Revision history

Table 10. Document revision history

| Date        | Revision | Changes        |
|-------------|----------|----------------|
| 09-Apr-2013 | 1        | First release. |

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