MICROCHIP

Product Change Notification / SYST-10WZNI073

Date:

11-Aug-2022

Product Category:

Ethernet Switches

PCN Type:

Document Change

Notification Subject:

Data Sheet - KSZ9897R Data Sheet

Affected CPNs:

SYST-10WZNI073_Affected_CPN_08112022.pdf
SYST-10WZNI073_Affected_CPN_08112022.csv

Notification Text:

SYST-10WZNI073

Microchip has released a new Datasheet for the KSZ9897R Data Sheet of devices. If you are using one of these devices please read the document located at KSZ9897R Data Sheet.

Notification Status: Final

Description of Change:
-Section 5.1.4.69, "Global PM Available Register" The following has been defeatured in the document: 'low latency cut through mode' and 'time aware traffic scheduler per port'.
-Table 3-2, "Pin Descriptions" Updated Port Receive Error pin definition: from "MII Mode" to "MII/RMII Modes" and "RMII/RGMII Modes" to "RGMII Mode".
-Table 3.2.1, "Configuration Straps" Updated strapping pin high instructions from "a non-LED pin" to "any pin".
-Table 3-3, "Configuration Strap Descriptions" Updated In-Band Management to include the following note: "If using I2C, do not enable IBA."
-Section 4.1.7, "Auto-Negotiation" Updated auto-negotiation bypass paragraph, changing "operating mode" to "operating speed". Also added this sentence to the end of the paragraph: "With parallel detection, the duplex will always be half-duplex."
-Section 5.1.2.3, "In-Band Management (IBA) Control Register" Updated bit 31 IBA Enable definition to add the following note: "If using I2C, do not enable IBA."
-Section 5.1.4.69, "Global PM Available Register" Added new register to accommodate Packet Memory Available Block Count.
-Section 5.2.2.21, "Port Special Register" Added new register to accommodate Single-LED Mode Workaround Bit.
-Section 5.2.7.4, "Port Authentication Control Register" Updated bit 2 Access Control List (ACL) Enable definition from "0 = enable" to "0

= disable".

-Section 5.2.9.3, "Port Transmit Queue Memory Register" Added new register to accommodate Port N Transmit Queue Blocks Used.

-Section 5.4.1, "MMD LED Mode Register" Updated bit 4 definition by adding the following sentence: "For Single-LED mode, set this bit and also set bit 9 in register 0xN13C-0xN13D."

-Table 5-3, "Data Rate Selection Table for Ingress and Egress Rate Limiting" Updated 7d'1 - 7d'10 1000Mbps BPS definition from "1Mbps" to "10Mbps".

-Section 6.4.7, "Power-up and Reset Timing" For Note 3, updated first sentence from: "The recommended power down sequence is to power down the low voltage core before powering down the transceiver and digital I/O voltages, or to have all supplies power down in unison" to "The power supplies may be powered down in any sequence."

-Table 4-14, "Transmit Tail Tag Format (from Host to Switch)" Bit 7 changed to "15:11" and description changed to "Reserved".

-Section 2.1, "General Description," on page 8 Updated first bullet to indicate the non-blocking wire-speed Ethernet switch fabric supports 1 Gbps on RGMII.

-Section 4.1.5, "Pair-Swap, Alignment, and Polarity Check" Updated first bullet description.

-Section 4.3.3, "Back-Off Algorithm" Updated second sentence.

-Section 4.3.5, "Legal Packet Size" Simplified paragraph for clarity.

-Section 4.3.6, "Flow Control" Simplified last sentence of third paragraph.

-Table 4-10 Updated Action description for the Yes entry.

-Section 4.4.3.2.1, Tag Insertion and Removal Updated last paragraph of section.

-Section 4.4.8, "Multiple Spanning Tree Support" Updated second sentence.

-Table 4-17, "ACL Matching Rule Parameters for MD = 01" Corrected ENB[1:0] "01" and "10" definitions to match those in Table 4-16, "Matching Rule Options".

-Section 4.10, "In-Band Management" • Added to last sentence of first paragraph. • Added additional sentence to end of second paragraph. • Added additional sentence to end of sixth paragraph.

-Section 5.2.1.7, "Port Operation Control 0 Register" Updated bit 6 and 7 descriptions to include references to the MAC and additional clarification.

-Section 5.2.2.15, "PHY Remote Loopback Register" Simplified bit 8 description.

-Section 5.2.4.1, "Port MAC Control 0 Register," on page 128 Bit 0 made reserved.

-Section 6.4.7, "Power-up and Reset Timing," on page 180 Updated Note 1.

-Table 6-11 Added new "trw" entry to table.

Impacts to Data Sheet: None

Change Implementation Status: Complete

Date Document Changes Effective: 11 Aug 2022

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices:: N/A

Attachments:

KSZ9897R Data Sheet

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Affected Catalog Part Numbers (CPN)

KSZ9897RTXC
KSZ9897RTXI
KSZ9897RTXC-TR
KSZ9897RTXI-TR