Alliance Memory Inc.
511 Taylor Way, Suite 1, San Carlos, CA 94070
Main +1(650)610-6800
FAX +1(650)620-9211

Product Change Notification (PCN)

Date: June 1 , 2017

PCN TRACKING NO:PCN-29052017-01

Subject: Product Change Notification (PCN) for Alliance LPSRAM's (64K LPSRAM)

Description of Change:	Product will only be offered in a new Die Revision
Reason for Change	Product revision to provide continuous support to Alliance's customers
Traceability, Guidelines (lot, date code, markings, shipment date)	Traceable through marketing part #
Updated Datasheet Summary of Changes between New and Old part numbers	Part # has been changed and updated datasheets are posted on our website http://www.alliancememory.com/products/pdf/AS6C6264.pdf See table 1 Below

Table 1

Density	Organization	Alliance Part Number	Alliance New Part Number
64K	8K x 8	U6264BDC07LLG1	AS6C6264-55PCN
64K	8K x 8	U6264BDK07LLG1	AS6C6264-55PIN
64K	8K x 8	U6264BS2C07LLG1	AS6C6264-55SCN
64K	8K x 8	U6264BS2C07LLG1TR	AS6C6264-55SCNTR
64K	8K x 8	U6264BS2K07LLG1	AS6C6264-55SIN
64K	8K x 8	U6264BS2K07LLG1TR	AS6C6264-55SINTR
64K	8K x 8	AS6C6264A-70PIN	AS6C6264-55PIN
64K	8K x 8	AS6C6264A-70PCN	AS6C6264-55PCN
64K	8K x 8	AS6C6264A-70SIN	AS6C6264-55SIN
64K	8K x 8	AS6C6264A-70SINTR	AS6C6264-55SINTR
64K	8K x 8	AS6C6264A-70SCN	AS6C6264-55SCN
64K	8K x 8	AS6C6264A-70SCNTR	AS6C6264-55SCNTR

Last Time Buy Date:	December 31st 2017
Last Time Ship Date:	March 31st 2018
Sample Available Date:	Sample and Production available NOW New Die Rev. has been in production for 10 years
PCN Effective Date:	June 1st 2017

***Any orders after July 1st, 2017 are Non-cancelable / Non-Returnable and cannot be changed. Products cannot be returned in stock rotations after this date.**

Alliance Memory Inc.
511 Taylor Way, Suite 1, San Carlos, CA 94070
Main +1(650)610-6800
FAX +1(650)620-9211

Dear Valued Customer:

This letter provides End–of–Life (EOL) notice of ZMD 64K Low Power SRAM products with a 64k density. These ZMD wafer will move from the original ZMD design to the Alliance design in Q3-2017. Please note that the ZMD design and the Alliance design are both fabricated from Global Foundries in Singapore. The assembly (Greatek in Taiwan) and testing (ChipMos in Taiwan) will remain the same.

The delivery deadline is March 31st, 2018 with last time buy (LTB) deadline on December 31st , 2017. Please note that the standard shipment dates will apply in general
and extended delivery dates must be pre-arranged and accepted in writing by Alliance Memory Management.

Please see the below comparison between the ZMD design vs. the Alliance design. Samples are available now.

Please contact your local Alliance Memory representative if you have any questions regarding this information.

Yours sincerely,

David Bagby
President
Alliance Memory Inc.

Comparison between

AS6C6264-55XXN and AS6C6264A-70XXN – 64Kb LP-SRAM

Part Number&result / Parameter	AS6C6264-55PCN AS6C6264-55PIN AS6C6264-55SCN AS6C6264-55SCNTR AS6C6264-55SIN AS6C6264-55SINTR	AS6C6264A-70PCN AS6C6264A-70PIN AS6C6264A-70SCN AS6C6264A-70SCNTR AS6C6264A-70SIN AS6C6264A-70SINTR	Comparison Result
Wafer Process			
Power Supply	2.7V~5.5V	4.5V ~ 5.5V	Difference
Typical Power Dissipation of Normal Operation	Speed:55ns Average Operating Power supply Current Icc=45mA(Max.) Icc1=10mA(Max.) Standby Power 1μA Supply Current I_{SB1}= 50μA(Max.), C Temp I_{SB1}= 80μA(Max.), I Temp	Speed:70ns Average Operating Power supply Current Icc=55 mA (Max.) Icc1=3mA(Max.) Standby Power 1μA Supply Current I_{SB1}= 2μA(Max.),C Temp I_{SB1}= 5μA(Max.), I Temp	Difference
Operating Temperature	Industrial：-40°C to +85°C Commercial:0°C to +70°C	Industrial：-40°C to +85°C Commercial:0°C to +70°C	Same
Max Operating Speed	55ns	70ns	Same
Interface (Input/Output) Capacitance	Input Capacitance CIN: <6pF. Input/Output Capacitance CI/O: <8pF.	Input Capacitance CIN: <8pF. Output Capacitance CO: <10pF.	Difference
Interface Definition	Omit.(See datasheet)	Omit.(See datasheet)	Same. They are pin to pin.
Interface Material	Pb and Halogen Free	Pb and Halogen Free	Same
Timing Parameters	Refer to Table 1	Refer to Table 1	Difference
Timing Diagram & Command	Omit.(See datasheet)	Omit.(See datasheet)	Same
Capacity	64Kb	64Kb	Same
Package	28pin 330mil SOP 28pin 600mil PDIP	28pin 330 mil SOP 28pin 600mil PDIP	Same
Truth Table	Omit.(See datasheet)	Omit.(See datasheet)	same
Supply Time			AS6C6264 will replace AS6C6264A

Alliance Memory,Inc.
Main +1(650)610.6800
FAX +1(650)620.9211
511 Taylor Way, San Carlos,CA94070,USA.

Table 1 AS6C6264 & AS6C6264A AC ELECTRICAL CHARACTERISTICS comparison

READ CYCLE						
Parameter		AS6C6264		AS6C6264A		
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle Time	tRC	55	-	70	-	ns
Address Access Time	tAA	-	55	-	70	ns
Chip Enable Access Time	tACE	-	55	-	70	ns
Output Enable Access Time	tOE		30	-	40	ns
Chip Enable to Output in Low-Z	tCLZ*	10	-			ns
Output Enable to Output in Low-Z	tOLZ*	5	-	5	10	ns
Chip Disable to Output in High-Z	tCHZ*	-	20	0	25	ns
Output Disable to Output in High-Z	tOHZ*		20	-	30	ns
Output Hold from Address Change	tOH	10	-	5	-	ns
WRITE CYCLE						
Parameter		AS6C6264		AS6C6264A		
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**
Write Cycle Time	tWC	55	-	70	-	ns
Address Valid to End of Write	tAW	50	-	70	-	ns
Chip Enable to End of Write	tCW	50	-	65	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Write Pulse Width	tWP	45	-	50	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Data to Write Time Overlap	tDW	25	-	35	-	ns
Data Hold from End of Write Time	tDH	0	-	0	-	ns
Output Active from End of Write	tOW*	5	-			ns
Write to Output in High-Z	tWHZ*	-	20	0	30	ns

Alliance Memory,Inc.
Main +1(650)610.6800
FAX +1(650)620.9211
511 Taylor Way, San Carlos,CA94070,USA.

Comparison between

AS6C6264-55XXN and U6264BXXX07LLG1 – 64Kb LP-SRAM

Part Number&result / Parameter	AS6C6264-55PCN AS6C6264-55PIN AS6C6264-55SCN AS6C6264-55SCNTR AS6C6264-55SIN AS6C6264-55SINTR	U6264BDC07LLG1 U6264BDK07LLG1 U6264BS2C07LLG1 U6264BS2C07LLG1TR U6264BS2K07LLG1 U6264BS2K07LLG1TR	Comparison Result
Wafer Process			
Power Supply	2.7V~5.5V	4.5V ~ 5.5V	Difference
Typical Power Dissipation of Normal Operation	Speed:55ns Average Operating Power supply Current Icc=45mA(Max.) Icc1=10mA(Max.) Standby Power µA Supply Current I_{SB1}= 50µA(Max.), C Temp I_{SB1}= 80µA(Max.), I Temp	peed:70ns Average Operating Power supply Current Icc=55 mA (Max.) Icc1=3mA(Max.) Standby Power µA Supply Current I_{SB1}= 2µA(Max.),C Temp I_{SB1}= 5µA(Max.), I Temp	Difference
Operating Temperature	Industrial：-40°C to +85°C Commercial:0°C to +70°C	Industrial：-40°C to +85°C Commercial:0°C to +70°C	Same
Max Operating Speed	55ns	70ns	Same
Interface (Input/Output) Capacitance	Input Capacitance CIN: <6pF. Input/Output Capacitance CI/O: <8pF.	Input Capacitance CIN: <8pF. Output Capacitance CO: <10pF.	Difference
Interface Definition	Omit.(See datasheet)	Omit.(See datasheet)	Same. They are pin to pin.
Interface Material	Pb and Halogen Free	Pb and Halogen Free	Same
Timing Parameters	Refer to Table 1	Refer to Table 1	Difference
Timing Diagram & Command	Omit.(See datasheet)	Omit.(See datasheet)	Same
Capacity	64Kb	64Kb	Same
Package	28pin 330mil SOP 28pin 600mil PDIP	28pin 330 mil SOP 28pin 600mil PDIP	Same
Truth Table	Omit.(See datasheet)	Omit.(See datasheet)	same
Supply Time			AS6C6264 will replace U6264B

Alliance Memory,Inc.
Main +1(650)610.6800
FAX +1(650)620.9211
511 Taylor Way, San Carlos,CA94070,USA.

Table 1 AS6C6264 & U6264B AC ELECTRICAL CHARACTERISTICS comparison

READ CYCLE						
Parameter		AS6C6264		U6264B		
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**
Read Cycle Time	tRC	55	-	70	-	ns
Address Access Time	tAA	-	55	-	70	ns
Chip Enable Access Time	tACE	-	55	-	70	ns
Output Enable Access Time	tOE		30	-	40	ns
Chip Enable to Output in Low-Z	tCLZ*	10	-			ns
Output Enable to Output in Low-Z	tOLZ*	5	-	5	10	ns
Chip Disable to Output in High-Z	tCHZ*	-	20	0	25	ns
Output Disable to Output in High-Z	tOHZ*		20	-	30	ns
Output Hold from Address Change	tOH	10	-	5	-	ns
WRITE CYCLE						
Parameter		AS6C6264		U6264B		
	Symbol	**Min**	**Max**	**Min**	**Max**	**Unit**
Write Cycle Time	tWC	55	-	70	-	ns
Address Valid to End of Write	tAW	50	-	70	-	ns
Chip Enable to End of Write	tCW	50	-	65	-	ns
Address Set-up Time	tAS	0	-	0	-	ns
Write Pulse Width	tWP	45	-	50	-	ns
Write Recovery Time	tWR	0	-	0	-	ns
Data to Write Time Overlap	tDW	25	-	35	-	ns
Data Hold from End of Write Time	tDH	0	-	0	-	ns
Output Active from End of Write	tOW*	5	-			ns
Write to Output in High-Z	tWHZ*	-	20	0	30	ns