S-8550 Series

STEP-DOWN, BUILT-IN FET, SYNCHRONOUS RECTIFICATION, PWM CONTROL SWITCHING REGULATORS

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Rev.5.0_02

The S-8550 Series is a CMOS synchronous rectification step-down switching regulator which mainly consists of a reference voltage circuit, an oscillator, an error amplifier, a phase compensation circuit, a PWM controller, an under voltage lockout circuit (UVLO), a current limit circuit, and a power MOS FET. The oscillation frequency is high at 1.2 MHz, so a high efficiency, large output current, step-down switching regulator can be achieved by using small external parts.
The built-in synchronous rectification circuit makes achieving high efficiency easier compared with conventional step-down switching regulators. A ceramic capacitor can be used as an output capacitor. High-density mounting is supported by adopting packages small SOT-23-5 and super-small and thin SNT-8A.

■ Features

- Oscillation frequency: 1.2 MHz
- Input voltage range: 2.0 V to 5.5 V
- Output voltage range: Arbitrarily settable by external output voltage setting resistor
- Output current: 600 mA
- Reference voltage: 0.6 V ±2.0%
- Efficiency: 92%
- Soft-start function: 1 ms typ.
- Shutdown function: Shutdown current consumption : 1.0 μA max.
- Built-in current limit circuit
- Pch power MOS FET on-resistance: 0.4 Ω typ.
- Nch power MOS FET on-resistance: 0.3 Ω typ.
- Constant continuous mode operation (no light load mode)
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

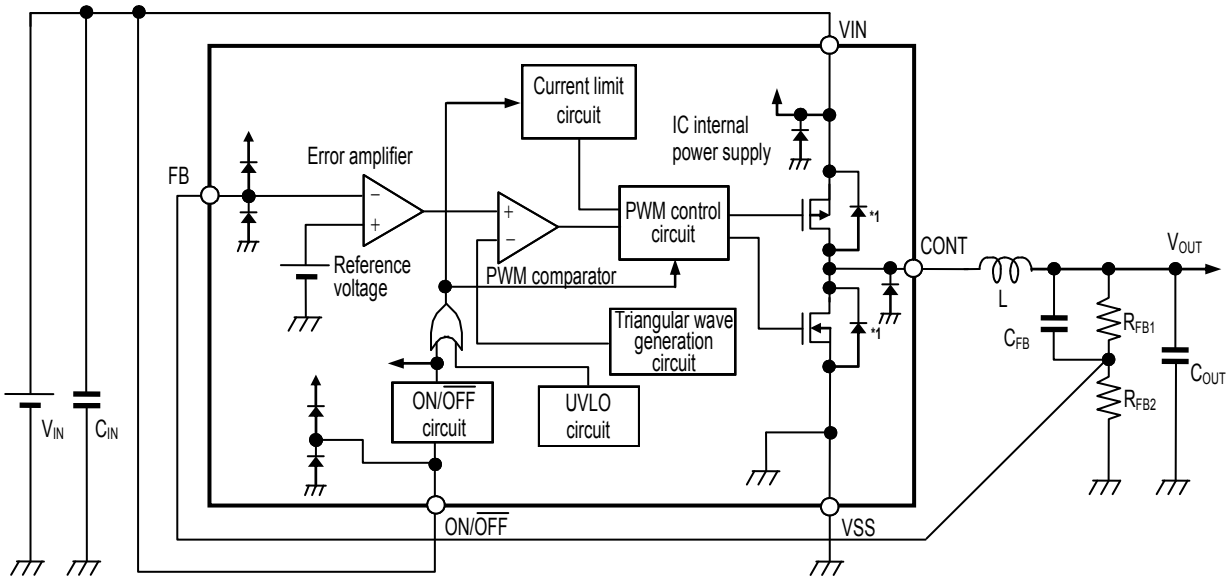
- Mobile devices, such as mobile phones, Bluetooth devices, wireless devices, digital audio players, digital still cameras, portable DVD players, and portable CD players

■ Packages

- SOT-23-5
- SNT-8A

■ Block Diagram

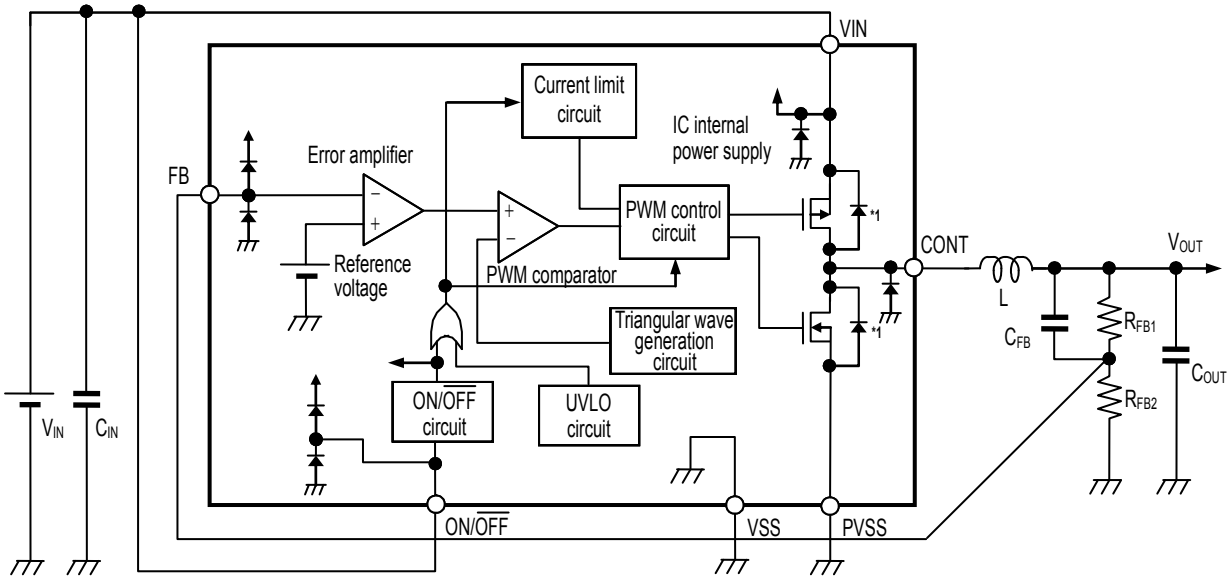
1. SOT-23-5



***1.** Parasitic diode

Figure 1

2. SNT-8A



***1.** Parasitic diode

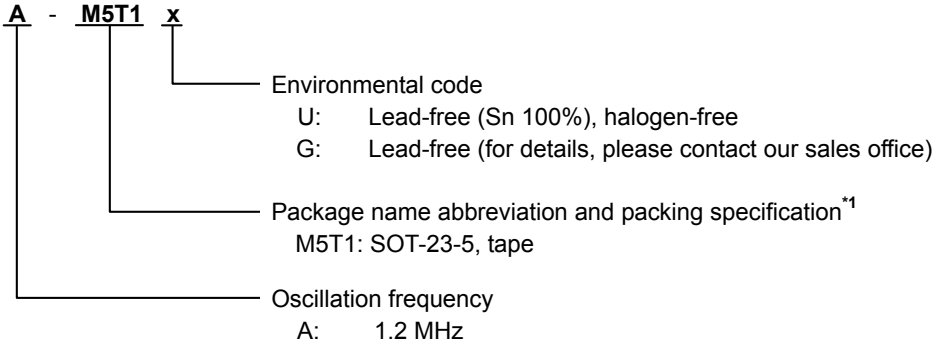
Figure 2

■ Product Name Structure

1. Product name

1. 1 SOT-23-5

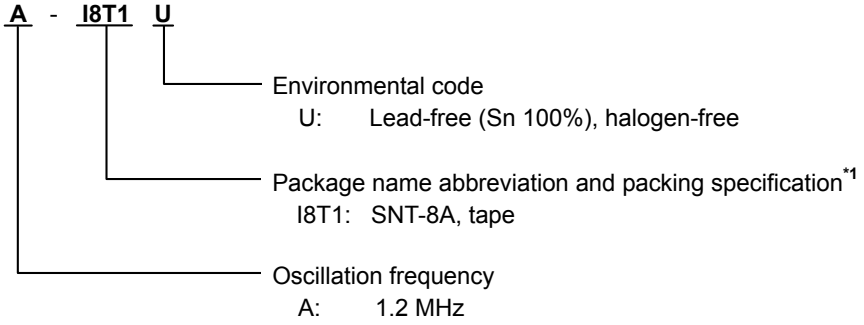
S-8550 A A - M5T1 x



***1.** Refer to the tape drawing.

1. 2 SNT-8A

S-8550 A A - I8T1 U



***1.** Refer to the tape drawing.

2. Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

■ Pin Configurations

1. SOT-23-5

Top view

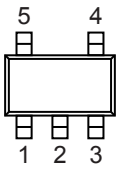


Figure 3

Table 1

Pin No.	Symbol	Description
1	VIN	IC power supply pin
2	VSS	GND pin
3	ON/$\overline{OFF}$	Shutdown pin "H" : Power on (normal operation) "L" : Power off (standby)
4	FB	Output voltage feedback pin
5	CONT	External inductor connection pin

2. SNT-8A

Top view

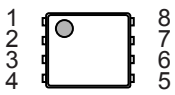


Figure 4

Table 2

Pin No.	Symbol	Description
1	FB	Output voltage feedback pin
2	NC*1	No connection
3	VSS*2	Small signal GND Pin
4	ON/$\overline{OFF}$	Shutdown pin "H" : Power on (normal operation) "L" : Power off (standby)
5	VIN	IC power supply pin
6	PVSS*2	Power GND pin
7	NC*1	No connection
8	CONT	External inductor connection pin

***1.** The NC pin is electrically open.
The NC pin can be connected to VIN, VSS or PVSS.

***2**. Connect VSS and PVSS to GND.

■ Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

(Unless otherwise specified: Ta = 25°C, V_{SS} = 0 V)

Item		Symbol	Absolute Maximum Rating	Unit
VIN pin voltage		V_{IN}	V_{SS} − 0.3 to V_{SS} + 6.0	V
FB pin voltage		V_{FB}	V_{SS} − 0.3 to V_{IN} + 0.3	V
CONT pin voltage		V_{CONT}	V_{SS} − 0.3 to V_{IN} + 0.3	V
ON/$\overline{OFF}$ pin voltage		$V_{ON/\overline{OFF}}$	V_{SS} − 0.3 to V_{IN} + 0.3	V
CONT pin current		I_{CONT}	1300	mA
Power dissipation	SOT-23-5	P_D	600[*1]	mW
	SNT-8A		450[*1]	mW
Operating temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on printed circuit board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name: JEDEC STANDARD51-7

Caution 1. The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

2. Since this IC has a built-in power MOS FET, make sure that dissipation of the power MOS FET does not exceed the allowable power dissipation of the package. (Refer to Figure 5.)
Generally, dissipation of a switching regulator can be calculated by the following equation.
Dissipation = (100 (%) − efficiency (%)) / efficiency (%) × output voltage × load current
The greater part of dissipation depends on the built-in power MOS FET, however, dissipation of the inductor is also included.
In addition, since power dissipation of the package also changes according to a mounting board or a mounting state, fully check them using an actually mounted mode.

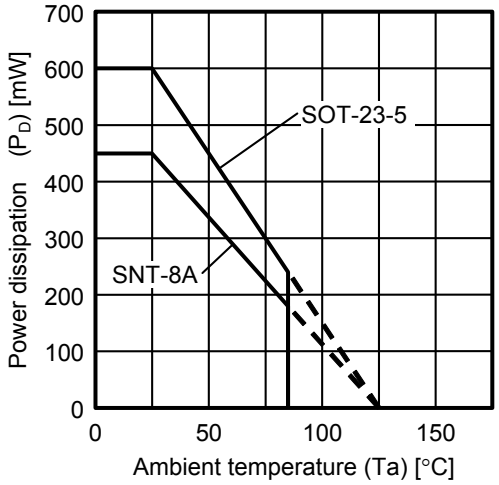


Figure 5 Power Dissipation of Package (Mounted on Board)

■ Electrical Characteristics

Table 4 Electrical Characteristics

(Unless otherwise specified: V_{IN} = 3.6 V, V_{OUT} = 1.8 V (the conditions in **Table 5**), Ta = +25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operating input voltage	V_{IN}	–	2.0	–	5.5	V	2
Output voltage range*1	V_{OUT}	V_{IN} = $V_{OUT(S)}$ + 0.4 V to 5.5 V	1.1	–	4.0	V	2
FB voltage	V_{FB}	V_{IN} = $V_{OUT(S)}$ + 0.4 V to 5.5 V	0.588	0.6	0.612	V	2
FB voltage temperature coefficient	$\frac{\Delta V_{FB}}{\Delta Ta}$	Ta = −40°C to +85°C	–	±100	–	ppm/°C	2
FB pin input current	I_{FB}	V_{IN} = 2.0 V to 5.5 V, FB pin	−0.1	–	+0.1	μA	1
Current consumption during shutdown	I_{SSS}	V_{IN} = 2.0 V to 5.5 V, $V_{ON/\overline{OFF}}$ = 0 V	–	–	1.0	μA	1
Current consumption 1	I_{SS1}	f_{osc} = 1.2 MHz, no external parts, V_{FB} = $V_{FB(S)}$ × 1.1 V	–	200	400	μA	1
Power MOS FET on-resistance	R_{PFET}	I_{CONT} = 100 mA	–	0.4	0.6	Ω	1
	R_{NFET}	I_{CONT} = −100 mA	–	0.3	0.5		
Power MOS FET leakage current	I_{LSW}	V_{IN} = 2.0 V to 5.5 V, $V_{ON/\overline{OFF}}$ = 0 V, V_{CONT} = 0 or 3.6 V	–	±0.01	±0.5	μA	1
Limit current	I_{LIM}	–	800	1000	1200	mA	1
Oscillation frequency	f_{osc}	–	1.02	1.2	1.38	MHz	2
Soft-start time	t_{SS}	Time required to reach 90% of $V_{OUT(S)}$	0.7	1.0	1.3	ms	2
High level input voltage	V_{SH}	V_{IN} = 2.0 V to 5.5 V, ON/$\overline{OFF}$ pin	0.9	–	–	V	2
Low level input voltage	V_{SL}	V_{IN} = 2.0 V to 5.5 V, ON/$\overline{OFF}$ pin	–	–	0.3	V	2
High level input current	I_{SH}	V_{IN} = 2.0 V to 5.5 V, ON/$\overline{OFF}$ pin	−0.1	–	0.1	μA	1
Low level input current	I_{SL}	V_{IN} = 2.0 V to 5.5 V, ON/$\overline{OFF}$ pin	−0.1	–	0.1	μA	1
UVLO detection voltage	V_{UVLO}	–	1.4	1.6	1.78	V	2

***1.** $V_{OUT(S)}$ is the output voltage set value, and V_{OUT} is the typ. value of the actual output voltage.
$V_{OUT(S)}$ can be set depending on the ratio between the V_{FB} value and output voltage set resistors (R_{FB1}, R_{FB2}).
For details, refer to "■ **External Parts Selection**".

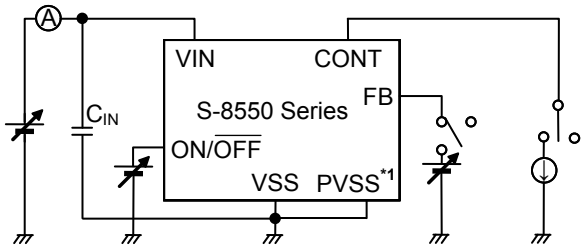
■ External Parts When Measuring Electrical Characteristics

Table 5 External Parts

Element Name	Symbol	Constant	Manufacturer	Part Number
Inductor	L	3.3 μH	Taiyo Yuden Co., Ltd.	NR4018T3R3M
Input capacitor	C_{IN}	4.7 μF	TDK Corporation	C3216X7R1E475K
Output capacitor	C_{OUT}	10 μF	TDK Corporation	C3216X7R1C106K
Output voltage set resistor 1	R_{FB1}	36 kΩ	Rohm Co., Ltd.	MCR03 Series 3602
Output voltage set resistor 2	R_{FB2}	18 kΩ	Rohm Co., Ltd.	MCR03 Series 1802
Phase compensation capacitor	C_{FB}	68 pF	Murata Manufacturing Co., Ltd.	GRM1882C1H680J

■ Test Circuits

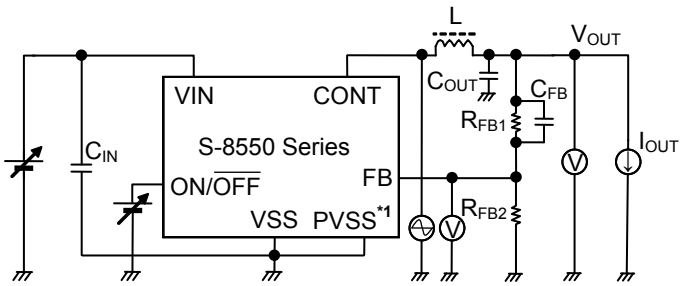
1.



***1**. PVSS pin is unavailable for the S-8550 Series with SOT-23-5.

Figure 6

2.



***1**. PVSS pin is unavailable for the S-8550 Series with SOT-23-5.

Figure 7

■ Operation

1. Synchronous rectification PWM control step-down switching regulator

1. 1 Synchronous rectification

The synchronous rectification method lowers voltage drop to greatly reduce power dissipation since an Nch power MOS FET, having resistance much lower than conventional switching regulators, is used.
In conventional switching regulators, current flows in the diode connected between the GND and CONT pins when the Pch power MOS FET is off. The forward drop voltage (V_f) of such diodes is large, between 0.3 V to 0.7 V, so the power dissipation used to be very large. Synchronous rectification ultra-low resistance Nch transistors repeat on and off, in synchronization with the operation of the Pch driver, in the reverse cycle of the Pch driver. Moreover, the built-in P and N through prevention circuit helps much reduction of power consumption during operation.

1. 2 PWM control

The S-8550 Series is a switching regulator using a pulse width modulation method (PWM) and features low current consumption.
In conventional PFM control switching regulators, pulses are skipped when the output load current is low, causing a fluctuation in the ripple frequency of the output voltage, resulting in an increase in the ripple voltage.
In the S-8550 Series, the switching frequency does not change, although the pulse width changes from 0% to 100% corresponding to each load current. The ripple voltage generated from switching can thus be removed easily using a filter because the switching frequency is constant.

2. Soft-start function

The soft-start circuit built in the S-8550 Series controls the rush current and the overshoot of the output voltage when powering on, the ON/$\overline{\text{OFF}}$ pin is switched from the “L” level to the “H” level, or the UVLO operation is released. A reference voltage adjustment method is adopted as the soft-start method.

3. Shutdown pin

This pin stops or starts step-up operations.
Switching the shutdown pin to the “L” level stops operation of all the internal circuits and reduces the current consumption significantly. DO NOT use the shutdown pin in a floating state because it is not pulled up or pulled down internally. DO NOT apply voltage of between 0.3 V and 0.9 V to the shutdown pin because applying such a voltage increases the current consumption. If the shutdown pin is not used, connect it to the VIN pin.

Table 6

Shutdown Pin	CR Oscillation Circuit	Output Voltage
“H”	Operates	Set value
“L”	Stops	Hi-Z

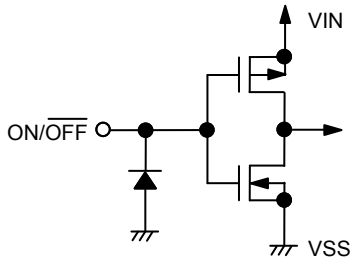


Figure 8

4. Current limit circuit

A current limit circuit is built in the S-8550 Series.
The current limit circuit monitors the current that flows in the Pch power MOS FET and limits current in order to prevent thermal destruction of the IC due to an overload or magnetic saturation of the inductor.
When a current exceeding the current limit detection value flows in the Pch power MOS FET, the current limit circuit operates and turns off the Pch power MOS FET since the current limit detection until one clock of the oscillator ends. The Pch power MOS FET is turned on in the next clock and the current limit circuit resumes current detection operation. If the value of the current that flows in the Pch power MOS FET remains the current limit detection value or more, the current limit circuit functions again and the same operation is repeated. Once the value of the current that flows in the Pch power MOS FET is lowered up to the specified value, the normal operation status restores. A slight overshoot is generated in the output voltage when the current limit is released.
The current limit detection value is fixed to 1 A (typ.) in the IC. If the time taken for the current limit to be detected is shorter than the time required for the current limit circuit in the IC to detect, the current value that is actually limited increases. Generally, the voltage difference between the VIN and VOUT pins is large, the current limit detection status is reached faster and the current value increases.

5. 100% duty cycle

The S-8550 Series operates up to the maximum duty cycle at 100%. Even when the input voltage is lowered up to the output voltage value set using the external output voltage setting resistor, the Pch power MOS FET is kept on and current can be supplied to the load. The output voltage at this time is the input voltage from which the voltage drop due to the direct resistance of the inductor and the on-resistance of the Pch power MOS FET are subtracted.

6. UVLO function

The S-8550 Series includes a UVLO (under-voltage lockout) circuit to prevent the IC from malfunctioning due to a transient status when power is applied or a momentary drop of the supply voltage. When UVLO is in the detection state, the Pch and Nch power MOS FETs stop switching operation, and the CONT pin become Hi-Z. Once the S-8550 Series is in the UVLO detection status, the soft-start function is reset, but the soft-start operates by the releasing operation of UVLO after that.
Note that the other internal circuits operate normally and that the status is different from the power-off status.
The hysteresis width is set for the UVLO circuit to prevent a malfunction due to a noise that is generated in the input voltage. A voltage about 150 mV (typ.) higher than the UVLO detection voltage is the release voltage.

■ Operation Principle

The S-8550 Series is a step-down synchronous rectification switching regulator based on constant PWM control. **Figure 9** shows the basic circuit diagram.

A step-down switching regulator starts current supply by the input voltage (V_{IN}) when the Pch power MOS FET is turned on and holds energy in the inductor at the same time. When the Pch power MOS FET is turned off, the current held in the inductor is released. The released current flows in the smoothing circuit, with the energy loss held minimum, supplies the output voltage (V_{OUT}) lower than V_{IN}. V_{OUT} is kept constant by controlling the switching frequency (f_{osc}) and ON time (t_{on}). With the PWM control method, V_{OUT} is made constant by controlling the ON time with f_{OSC} unchanged.

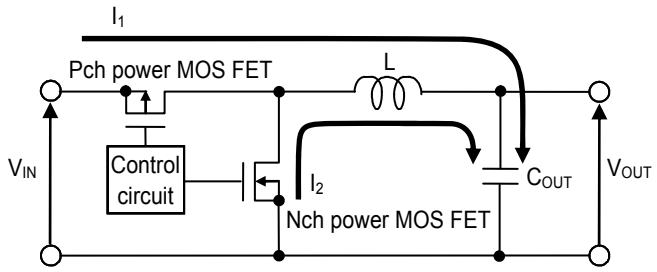


Figure 9 Basic Circuit Drawing of Step-down Switching Regulator

1. Continuous mode

The following explains how the current flows to the inductor when the step-down operation is constant and stable.

When the Pch power MOS FET is turned on, current I_1 flows in the direction shown by the arrow in **Figure 9**, and energy is stored in the inductor (L). When the output capacitor (C_{OUT}) is charged, supply of the output current (I_{OUT}) is started at the same time. The inductor current (I_L) gradually increases in proportion to the ON time (t_{ON}) of the Pch power MOS FET as shown in **Figure 10** (changes from I_L min. to I_L max.). When the Pch power MOS FET is turned off, the Nch power MOS FET is turned on and I_L tries to hold I_L max. Consequently, current I_2 flows in the direction shown by the arrow in **Figure 9**. As a result, I_L gradually decreases and reaches I_L min. when the OFF time (t_{OFF}) has elapsed. When t_{OFF} has elapsed, the Nch power MOS FET is turned off and the next cycle is entered. The above sequence is repeated.

As explained in the above, the continuous mode refers to the operation in the current cycle in which I_L linearly changes from I_L min. to I_L max. Even if I_L min. is less than 0 A, I_L min. keeps flowing (backflow current flows).

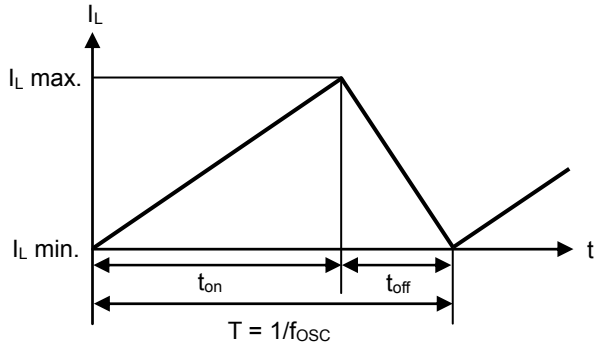


Figure 10 Continuous Mode (Current Cycle of Inductor Current (I_L))

2. Backflow current

The S-8550 Series performs PWM synchronous rectification even if I_L min. is less than 0 A, so a backflow current is generated in V_{IN} and the backflow current becomes maximum when no load is applied (Refer to **Figure 11**). Use the following equation to calculate the maximum backflow current value, which should be taken into consideration when designing.

Duty (I_{OUT} = 0) = V_{OUT} / V_{IN}

Example : V_{IN} = 3.6 V, V_{OUT} = 1.8 V …… Duty = 50%

$\Delta I_L = \Delta V / L \times t_{on} = (V_{IN} - V_{OUT}) \times Duty / (L \times f_{OSC})$

Example : V_{IN} = 3.6 V, V_{OUT} = 1.8 V, f_{OSC} = 1.2 MHz, L = 3.3 μH …… ΔI_L = 227 mA

I_L max. = ΔI_L / 2 = 113.5 mA, I_L min. = $-\Delta I_L$ / 2 = −113.5 mA

The current value waveform of the inductor is a triangular wave, of which the maximum value is I_L max. and the minimum value is I_L min. (negative value), and the negative value (the portion marked by diagonal lines in **Figure 11**) backflows when no load is applied (Refer to **Figure 11**).
If about 113.5 mA of I_{OUT} flows in the above conditions, the minimum value (I_L min.) of the triangular wave is made 0 mA and no backflow current flows.
When an input capacitor (C_{IN}) is connected, the backflow current is absorbed by C_{IN}, thus reducing the backflow current to flow in the power supply. Be sure to connect an input capacitor to reduce backflow current to the power supply (Refer to **Figure 12**).

The above presents the conditions required to prevent backflow current from flowing, which is only a guideline. Perform sufficient confirmation using an actual application.

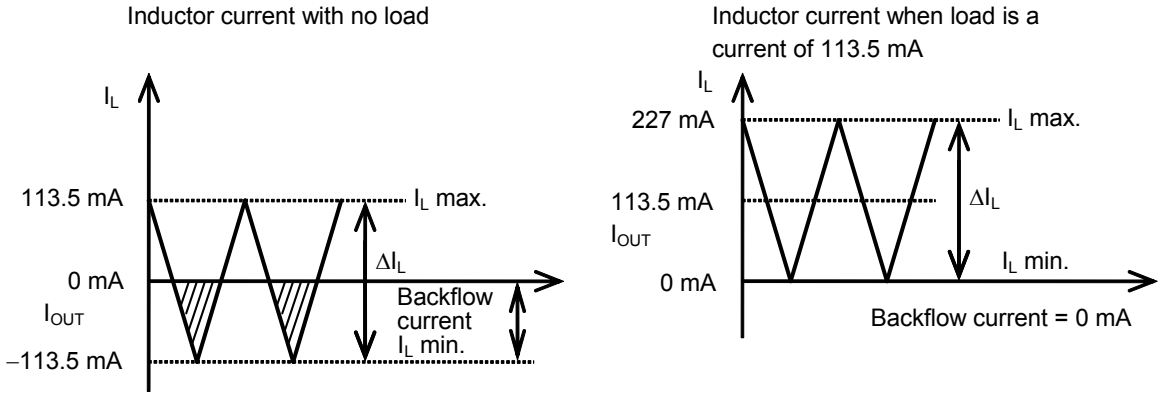


Figure 11 Example of Conditions to Prevent Backflow Current from Flowing

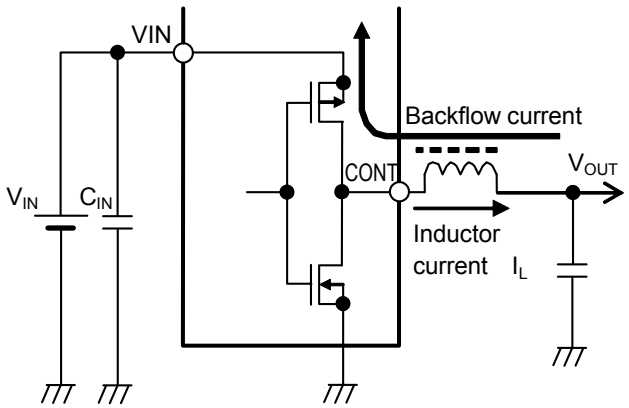


Figure 12 Backflow Current

■ External Parts Selection

1. Inductor

The inductance (L value) has a strong influence on the maximum output current (I_{OUT}) and efficiency (η).
The peak current (I_{PK}) increases by decreasing L and the stability of the circuit improves and I_{OUT} increases. If L is decreased further, the current drive capability of the external transistor is insufficient and I_{OUT} decreases.
If the L value is increased, the loss due to I_{PK} of the power MOS FET decreases and the efficiency becomes maximum at a certain L value. Further increasing L decreases the efficiency due to the increased loss of the DC resistance of the inductor.
The recommended L value for the S-8550 Series is 3.3 μH.
When selecting an inductor, note the allowable current of the inductor. If a current exceeding this allowable current flows through the inductor, magnetic saturation occurs, substantially lowering the efficiency.
Therefore, select an inductor so that I_{PK} does not exceed the allowable current. I_{PK} is expressed by the following equations in the discontinuous mode and continuous mode.

$$I_{PK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times f_{OSC} \times L \times V_{IN}}$$

f_{OSC} = Oscillation frequency

Table 7 Typical Inductors

Manufacturer	Part Number	L Value	DC Resistance	Rated Current	Dimensions (L × W × H) [mm]
Taiyo Yuden Co., Ltd.	NR4018T3R3M	3.3 μH	0.07 Ω max.	1.23 A max.	4.0 × 4.0 × 1.8
	NR3012T3R3M	3.3 μH	0.1 Ω max.	0.91 A max.	3.0 × 3.0 × 1.2
Sumida Corporation	CDRH3D16/HP-3R3	3.3 μH	0.085 Ω max.	1.40 A max.	4.0 × 4.0 × 1.8
	CDRH2D11/HP-3R3	3.3 μH	0.173 Ω max.	0.9 A max.	3.2 × 3.2 × 1.2
TDK Corporation	VLF4012AT-3R3M	3.3 μH	0.12 Ω max.	1.3 A max.	3.7 × 3.5 × 1.2
	VLF3010AT-3R3M	3.3 μH	0.17 Ω max.	0.87 A max.	2.6 × 2.8 × 1.0
FDK Corporation	MIP3226D3R3M	3.3 μH	0.104 Ω max.	1.2 A max.	3.2 × 2.6 × 1.0
	MIPS2520D3R3M	3.3 μH	0.156 Ω max.	1.0 A max.	2.5 × 2.0 × 1.0

2. Capacitors (C_{IN}, C_{OUT})

A ceramic capacitor can be used for the input (C_{IN}) and output (C_{OUT}) sides. C_{IN} lowers the power supply impedance and averages the input current to improve efficiency. Select C_{IN} according to the impedance of the power supply to be used. The recommended capacitance is 4.7 μF for the S-8550 Series when a general lithium ion rechargeable battery is used.
Select as C_{OUT} a capacitor with large capacitance and small ESR for smoothing the ripple voltage. The optimum capacitor selection depends on the L value, capacitance value, wiring, and application (output load). Select C_{OUT} after sufficient evaluation under actual use conditions.

3. Output voltage setting resistors (R_{FB1}, R_{FB2}), capacitor for phase compensation (C_{FB})

With the S-8550 Series, V_{OUT} can be set to any value by external divider resistors. Connect the divider resistors across the VOUT and VSS pins. Because V_{FB} = 0.6 V typ., V_{OUT} can be calculated by this equation.

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \times 0.6$$

Connect divider resistors R_{FB1} and R_{FB2} as close to the IC to minimize effects from of noise. If noise does have an effect, adjust the values of R_{FB1} and R_{FB2} so that $R_{FB1} + R_{FB2} < 100\ k\Omega$.
C_{FB} connected in parallel with R_{FB1} is a capacitor for phase compensation.
By setting the zero point (the phase feedback) by adding capacitor C_{FB} to output voltage setting resistor R_{FB1} in parallel, the feedback loop gains the phase margin. As a result, the stability can be obtained. In principle, to use the portion how much the phase has feed back by the zero point effectively, define C_{FB} referring to the following equation.

$$C_{FB} \cong \frac{1}{2 \times \pi \times R_{FB1} \times 70\ kHz}$$

This equation is the reference.

The followings are explanation regarding the proper setting.
To use the portion how much the phase has feed back by the zero point effectively, set R_{FB1} and C_{FB} so that the zero point goes into the higher frequency than the pole frequency of L and C_{OUT}. The following equations are the pole frequency of L and C_{OUT} and the zero point frequency by C_{FB} and R_{FB1}.

$$f_{pole} \cong \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$f_{zero} \cong \frac{1}{2 \times \pi \times R_{FB1} \times C_{FB}}$$

The transient response can be improved by setting the zero point frequency in the range of lower frequency. However, since the gain becomes higher in the range of high frequency, the total phase of feedback loop delays 180° or more by setting the zero point frequency in the significantly lower range. As a result, the gain cannot be 0 dB or lower in the frequency range thus the operation might be unstable. Determine the proper value after the sufficient evaluation under the actual condition.
The typical constants by our evaluation are in **Table 8**.

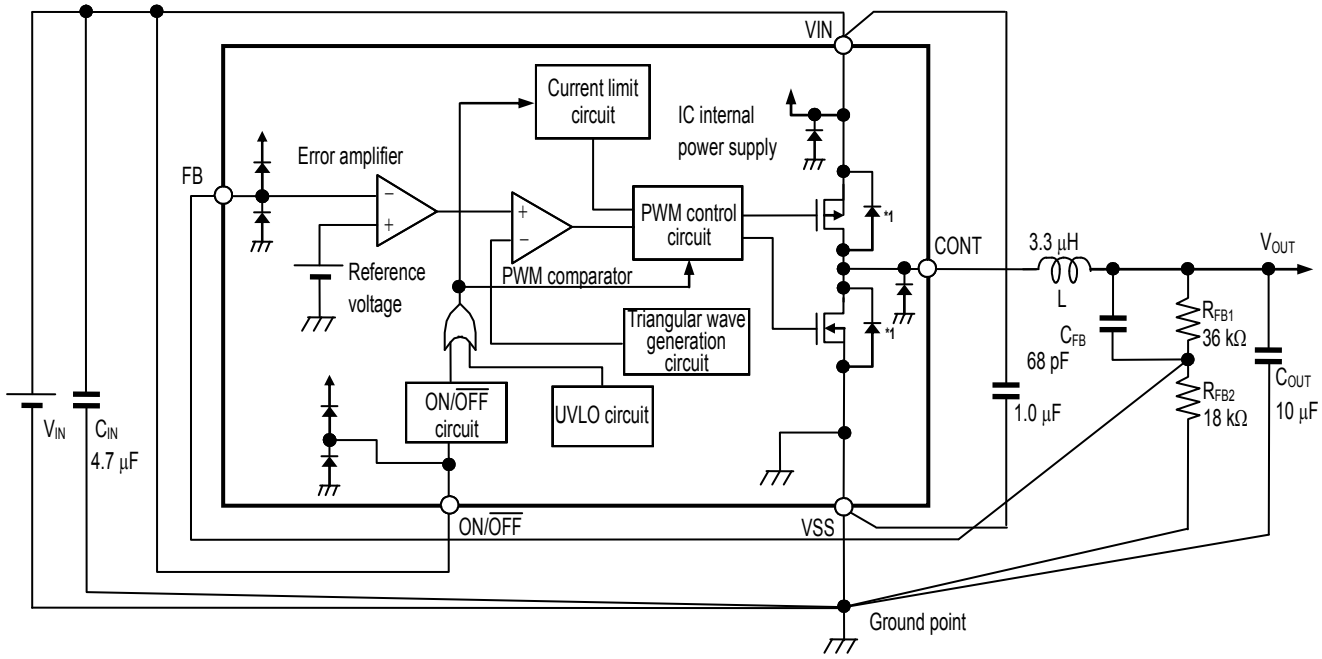
Table 8 Constant for External Parts

V_{OUT}(s) [V]	R_{FB1} [kΩ]	R_{FB2} [kΩ]	C_{FB} [pF]	L [μH]*1	C_{OUT} [μF]*1
1.1	36	43	56	3.3	10
1.8	36	18	68	3.3	10
3.3	36	8	120	3.3	10
4.0	51	9	100	3.3	10

***1.** The recommended parts in **Table 5**

■ Standard Circuits

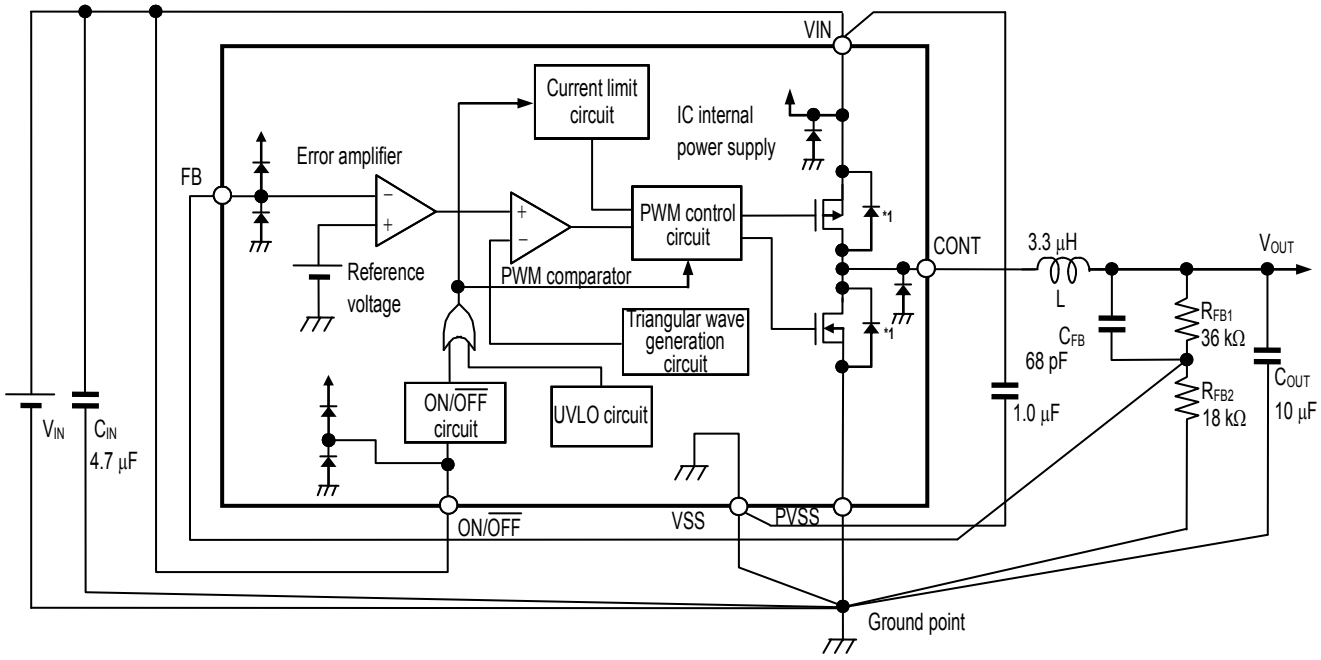
1. SOT-23-5



***1.** Parasitic diode

Figure 13

2. SNT-8A



***1.** Parasitic diode

Figure 14

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using an actual application to set the constants.

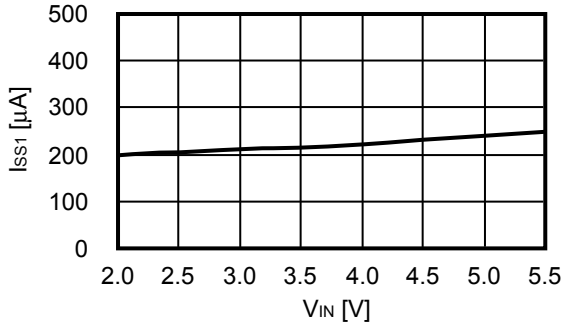
■ Precaution

- Mount external capacitors, diodes, and inductors as close as possible to the IC, and make a one-point grounding.
- Characteristics ripple voltage and spike noise occur in IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply used, fully check them using an actually mounted model.
- The 1.0 μF capacitance connected between the VIN and VSS pins is a bypass capacitor. It stabilizes the power supply in the IC when application is used with a heavy load, and thus effectively works for stable switching regulator operation. Allocate the bypass capacitor as close to the IC as possible, prioritized over other parts.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- The power dissipation of the IC greatly varies depending on the size and material of the board to be connected. Perform sufficient evaluation using an actual application before designing.
- ABLIC Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does ABLIC Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

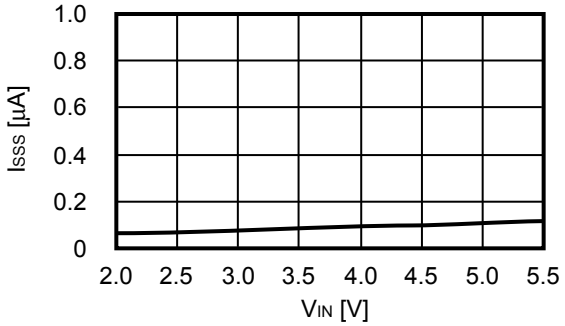
■ Characteristics (Typical Data)

1. Example of Major Power Supply Dependence Characteristics (Ta = +25°C)

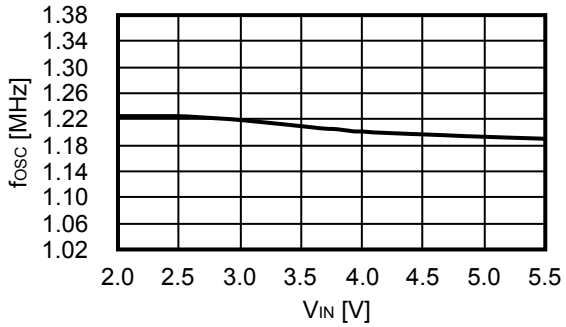
1. 1 Current consumption 1 (I_{SS1}) vs. Input voltage (V_{IN})



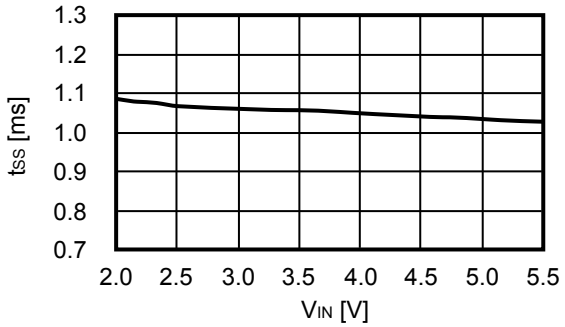
1. 2 Current consumption during shutdown (I_{SSS}) vs. Input voltage (V_{IN})



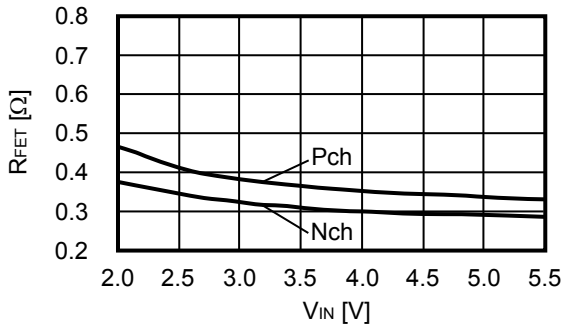
1. 3 Oscillation frequency (f_{osc}) vs. Input voltage (V_{IN})



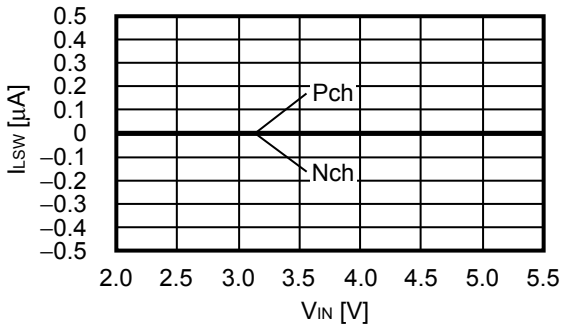
1. 4 Soft-start time (t_{SS}) vs. Input voltage (V_{IN})



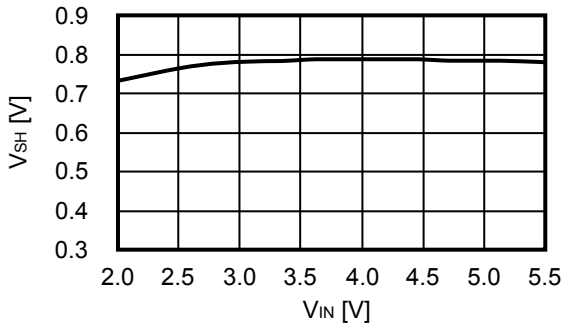
1. 5 Power MOS FET on-resistance (R_{FET}) vs. Input voltage (V_{IN})



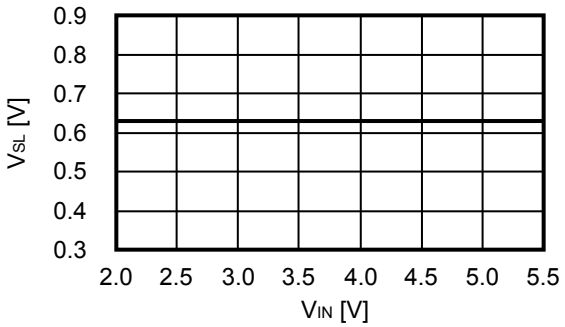
1. 6 Power MOS FET leakage current (I_{LSW}) vs. Input voltage (V_{IN})



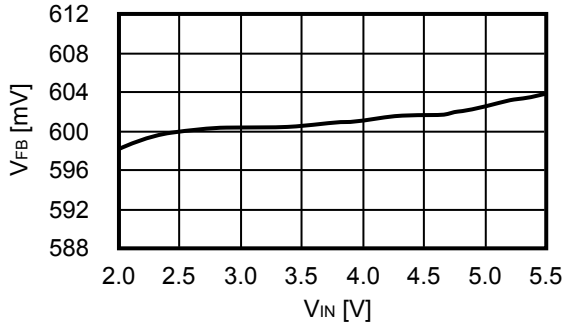
1. 7 ON/$\overline{\text{OFF}}$ pin input voltage"H" (V_{SH}) vs. Input voltage (V_{IN})



1. 8 ON/$\overline{\text{OFF}}$ pin input voltage"L" (V_{SL}) vs. Input voltage (V_{IN})

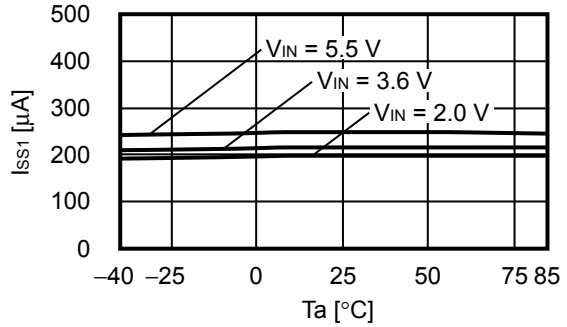


1. 9 FB voltage (V_{FB}) vs. Input voltage (V_{IN})

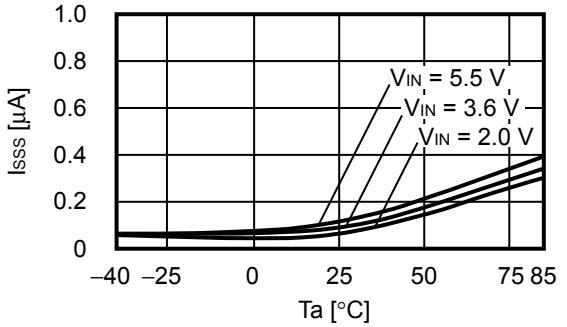


2. Example of Major Temperature Characteristics (Ta = –40 to +85°C)

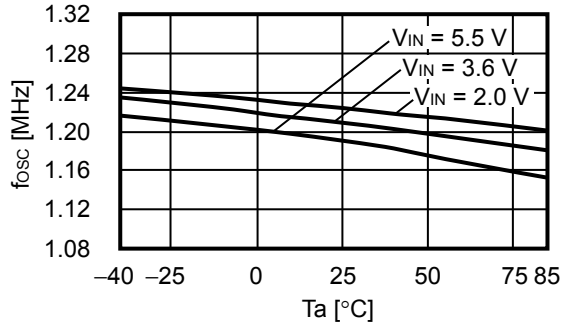
2. 1 Current consumption 1 (I_{SS1}) vs. Temperature (Ta)



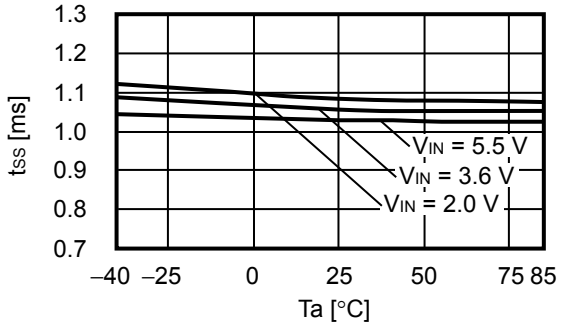
2. 2 Current consumption during shutdown (I_{SSS}) vs. Temperature (Ta)



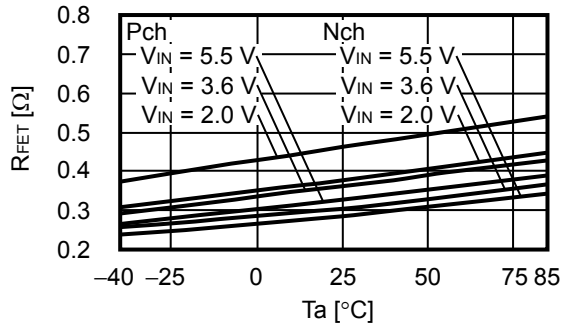
2. 3 Oscillation frequency (f_{osc}) vs. Temperature (Ta)



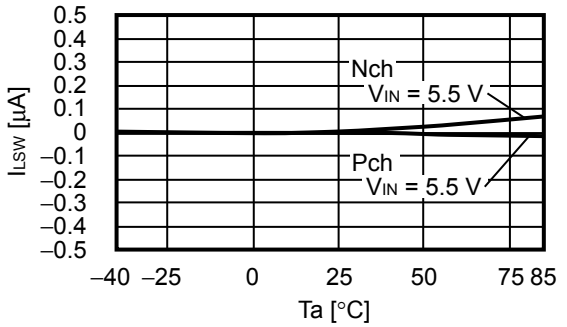
2. 4 Soft-start time (t_{SS}) vs. Temperature (Ta)



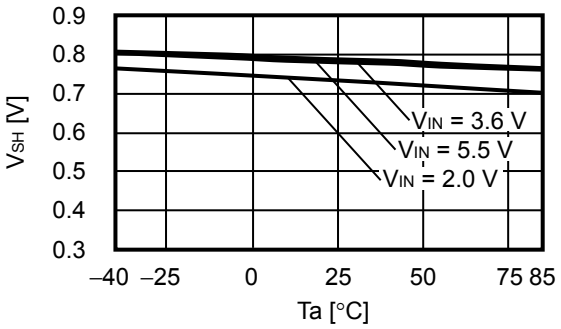
2. 5 Power MOS FET on-resistance (R_{FET}) vs. Temperature (Ta)



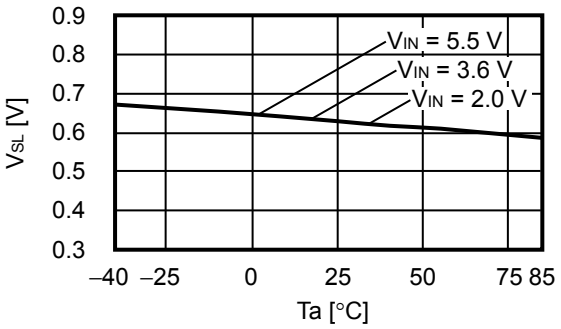
2. 6 Power MOS FET leakage current (I_{LSW}) vs. Temperature (Ta)



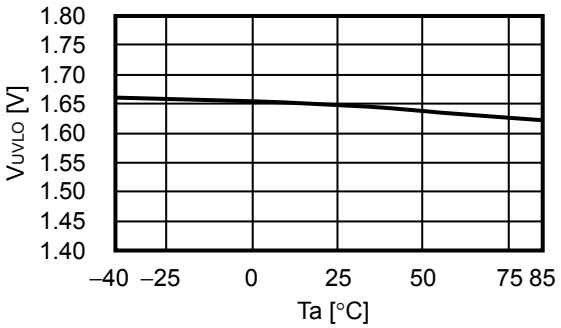
2. 7 ON/$\overline{OFF}$ pin input voltage"H" (V_{SH}) vs. Temperature (Ta)



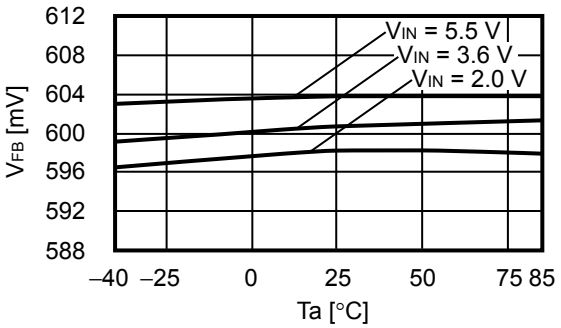
2. 8 ON/$\overline{OFF}$ pin input voltage"L" (V_{SL}) vs. Temperature (Ta)



2. 9 UVLO detection voltage (V_{UVLO}) vs. Temperature (Ta)



2. 10 FB voltage (V_{FB}) vs. Temperature (Ta)

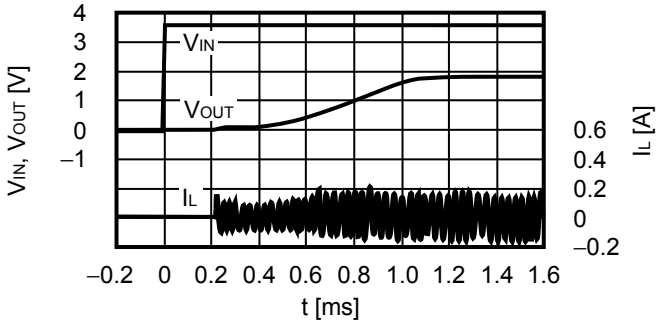


3. Examples of Transient Response Characteristics

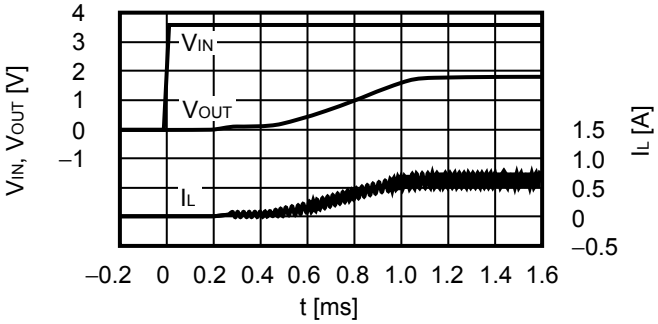
(Unless otherwise specified, the used parts are ones shown in ■ **External Parts When Measuring Electrical Characteristics**.)

3. 1 Powering ON (V_{OUT} = 1.8 V, V_{IN} = 0 V → 3.6 V, Ta = +25°C)

(1) I_{OUT} = 1 mA

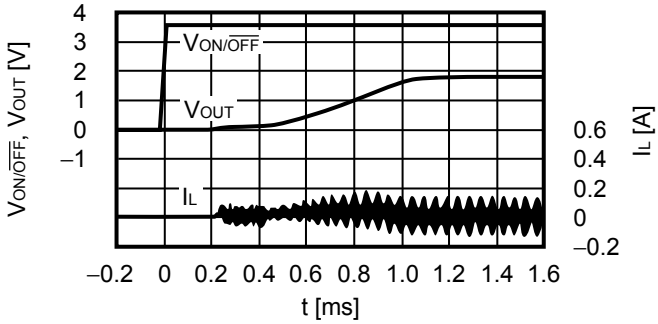


(2) I_{OUT} = 600 mA

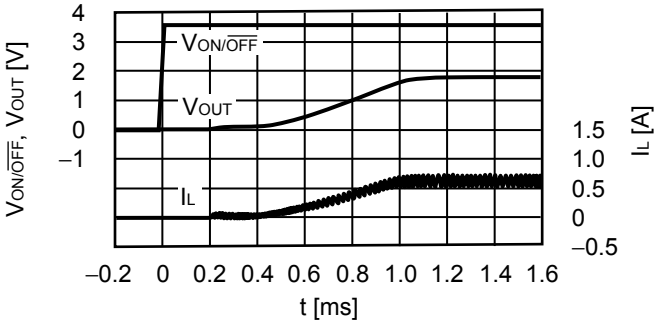


3. 2 Shutdown pin response (V_{OUT} = 1.8 V, V_{IN} = 3.6 V, $V_{ON/\overline{OFF}}$ = 0 V → 3.6 V, Ta = +25°C)

(1) I_{OUT} = 1 mA

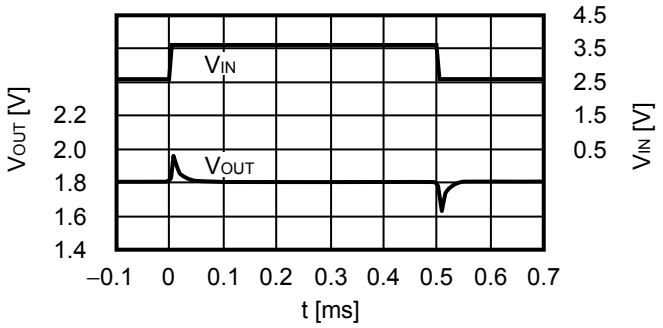


(2) I_{OUT} = 600 mA

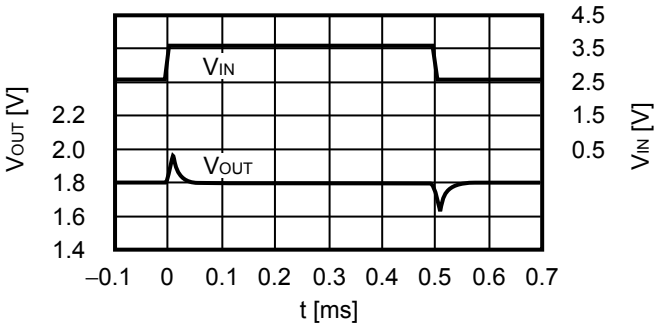


3. 3 Power supply fluctuations (V_{OUT} = 1.8 V, Ta = +25°C)

(1) I_{OUT} = 1 mA, V_{IN} = 2.6 V → 3.6 V → 2.6 V

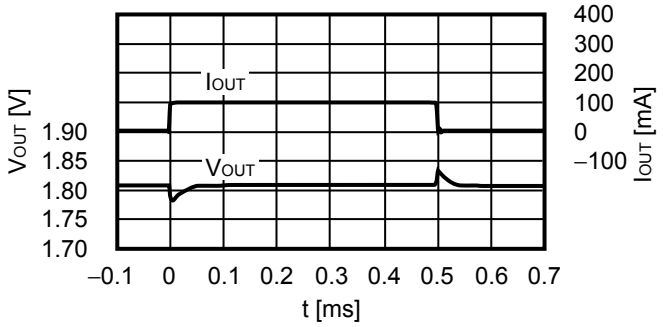


(2) I_{OUT} = 600 mA, V_{IN} = 2.6 V → 3.6 V → 2.6 V

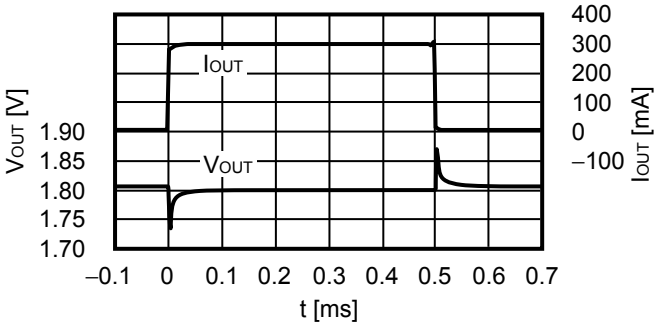


3. 4 Load fluctuations (V_{OUT} = 1.8 V, V_{IN} = 3.6 V, Ta = +25°C)

(1) I_{OUT} = 0.1 mA → 100 mA → 0.1 mA



(2) I_{OUT} = 0.1 mA → 300 mA → 0.1 mA



■ Reference Data

1. Reference data for external parts

Table 9 Properties of External Parts

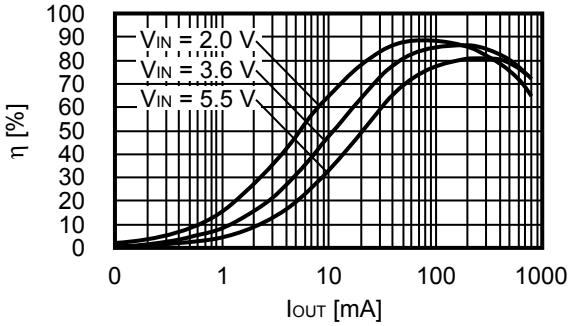
Element Name	Product Name	Manufacture	Characteristics
Inductor	NR4018T3R3M	Taiyo Yuden Co., Ltd	3.3 μH, DCR_{MAX} = 0.07 Ω, I_{MAX} = 1.23 A
Input capacitor	C3216X7R1E475K	TDK Corporation	4.7 μF
Output capacitor	C3216X7R1C106K	TDK Corporation	10 μF

Caution The values of the external parts are based on the materials provided by each manufacturer. However, consider the characteristics of the original materials when using the above products.

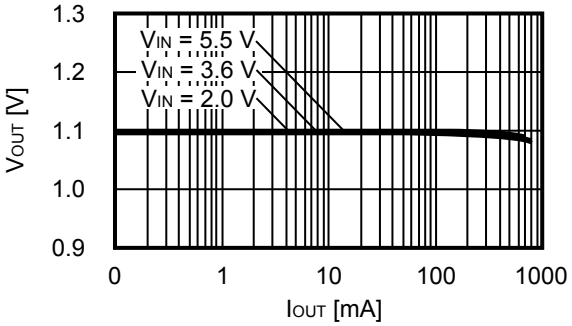
2. Output current (I_{OUT}) vs. Efficiency (η) Characteristics and Output current (I_{OUT}) vs. Output voltage (V_{OUT}) Characteristics

2. 1 V_{OUT} = 1.1 V (R_{FB1} = 36 kΩ, R_{FB2} = 43 kΩ)

(1) Output current (I_{OUT}) vs. Efficiency (η)

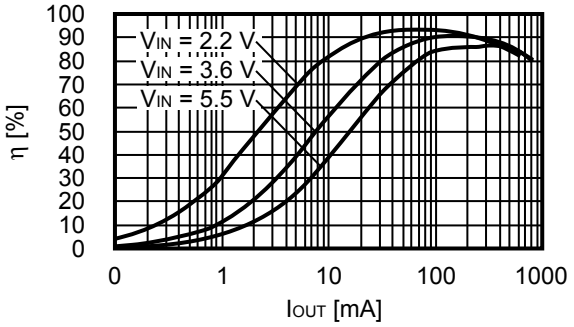


(2) Output current (I_{OUT}) vs. Output voltage (V_{OUT})

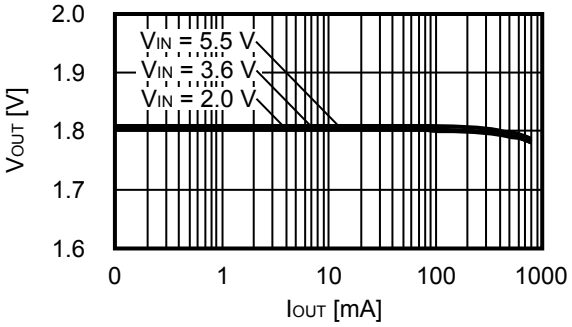


2. 2 V_{OUT} = 1.8 V (R_{FB1} = 36 kΩ, R_{FB2} = 18 kΩ)

(1) Output current (I_{OUT}) vs. Efficiency (η)

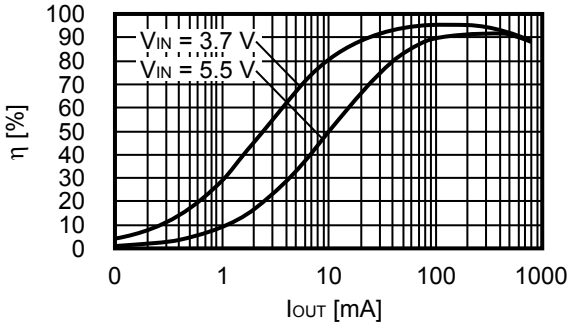


(2) Output current (I_{OUT}) vs. Output voltage (V_{OUT})

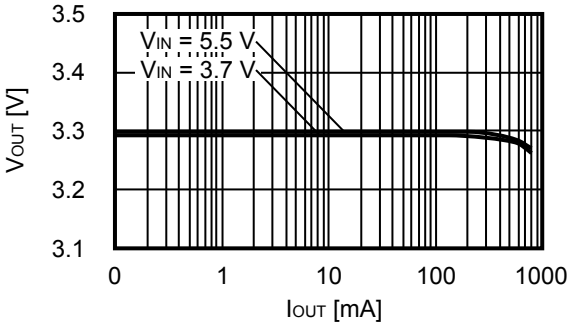


2. 3 V_{OUT} = 3.3 V (R_{FB1} = 36 kΩ, R_{FB2} = 8 kΩ)

(1) Output current (I_{OUT}) vs. Efficiency (η)

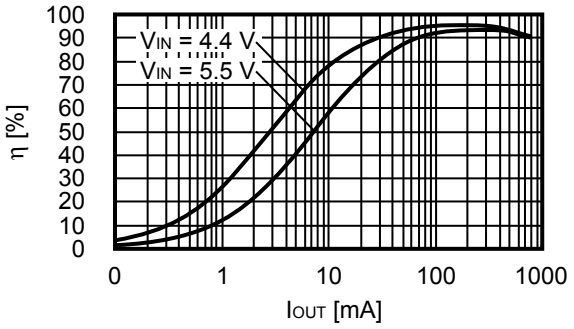


(2) Output current (I_{OUT}) vs. Output voltage (V_{OUT})

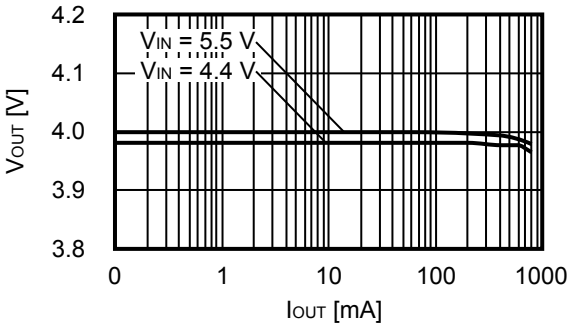


2. 4 V_{OUT} = 4.0 V (R_{FB1} = 51 kΩ, R_{FB2} = 9 kΩ)

(1) Output current (I_{OUT}) vs. Efficiency (η)



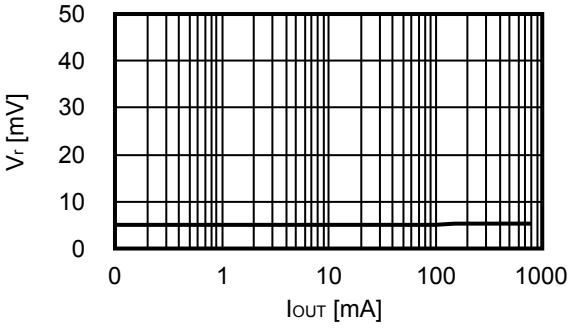
(2) Output current (I_{OUT}) vs. Output voltage (V_{OUT})



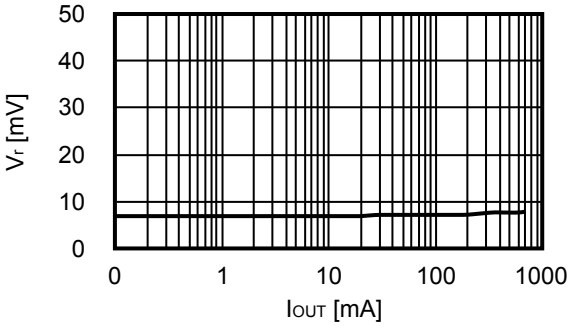
3. Output current (I_{OUT}) vs. Ripple voltage (V_r) Characteristics

3. 1 V_{OUT} = 1.1 V (R_{FB1} = 36 kΩ, R_{FB2} = 43 kΩ)

(1) V_{IN} = 3.6 V

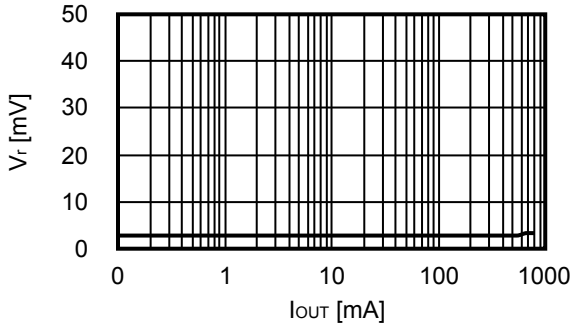


(2) V_{IN} = 5.5 V

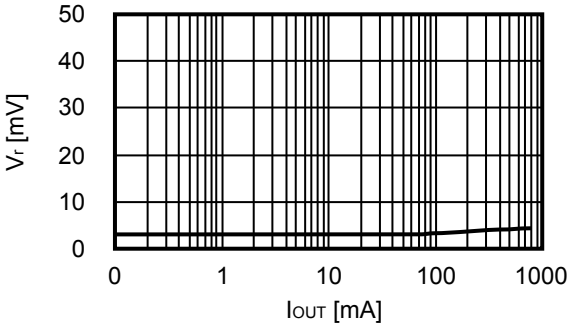


3. 2 V_{OUT} = 1.8 V (R_{FB1} = 36 kΩ, R_{FB2} = 18 kΩ)

(1) V_{IN} = 3.6 V

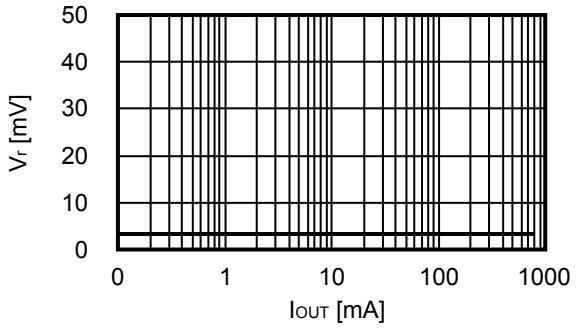


(2) V_{IN} = 5.5 V

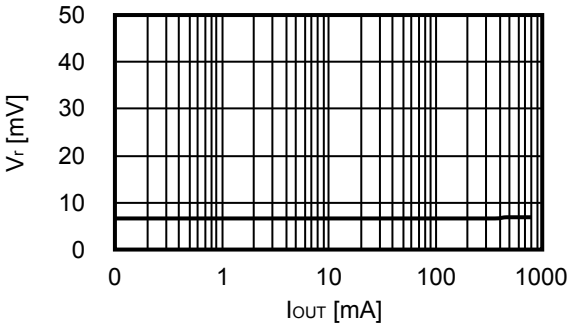


3. 3 V_{OUT} = 3.3 V (R_{FB1} = 36 kΩ, R_{FB2} = 8 kΩ)

(1) V_{IN} = 3.6 V

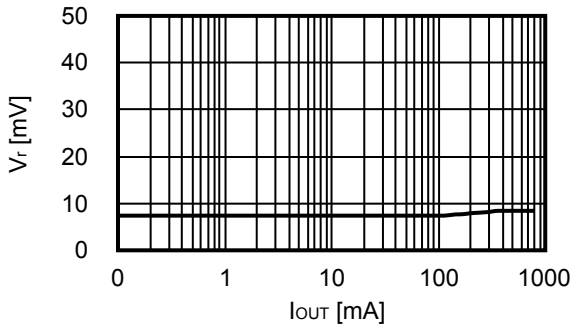


(2) V_{IN} = 5.5 V



3. 4 V_{OUT} = 4.0 V (R_{FB1} = 51 kΩ, R_{FB2} = 9 kΩ)

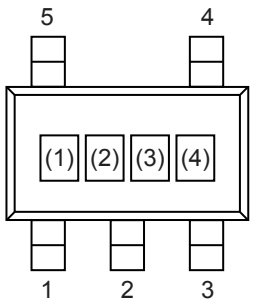
(1) V_{IN} = 5.5 V



■ Marking Specifications

1. SOT-23-5

Top view



(1) to (3): Product code (Refer to **Product name vs. Product code**.)
(4): Lot number

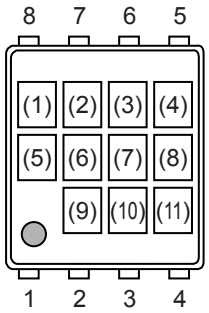
Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8550AA-M5T1x	R	5	A

Remark 1. x: G or U
2. Please select products of environmental code = U for Sn 100%, halogen-free products.

2. SNT-8A

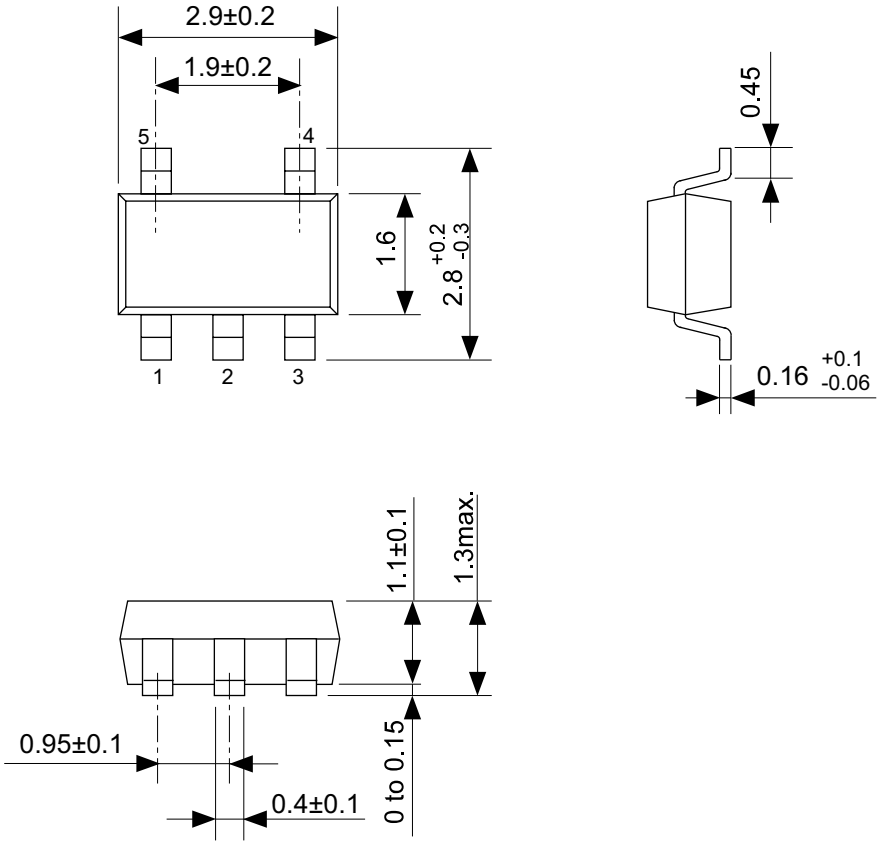
Top view



(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5), (6): Blank
(7) to (11): Lot number

Product name vs. Product code

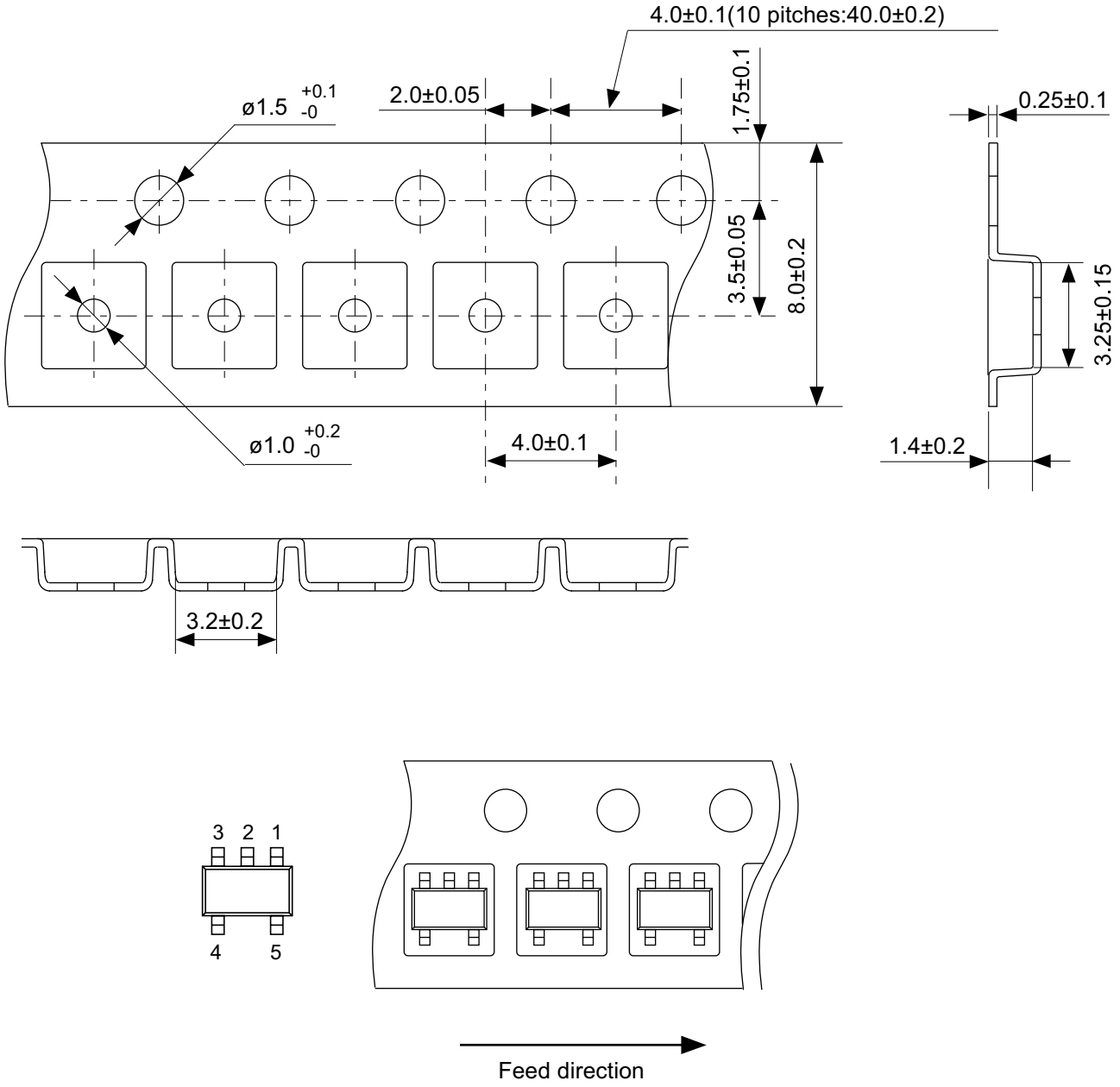
Product name	Product code		
	(2)	(3)	(4)
S-8550AA-I8T1U	R	5	A



No. MP005-A-P-SD-1.3

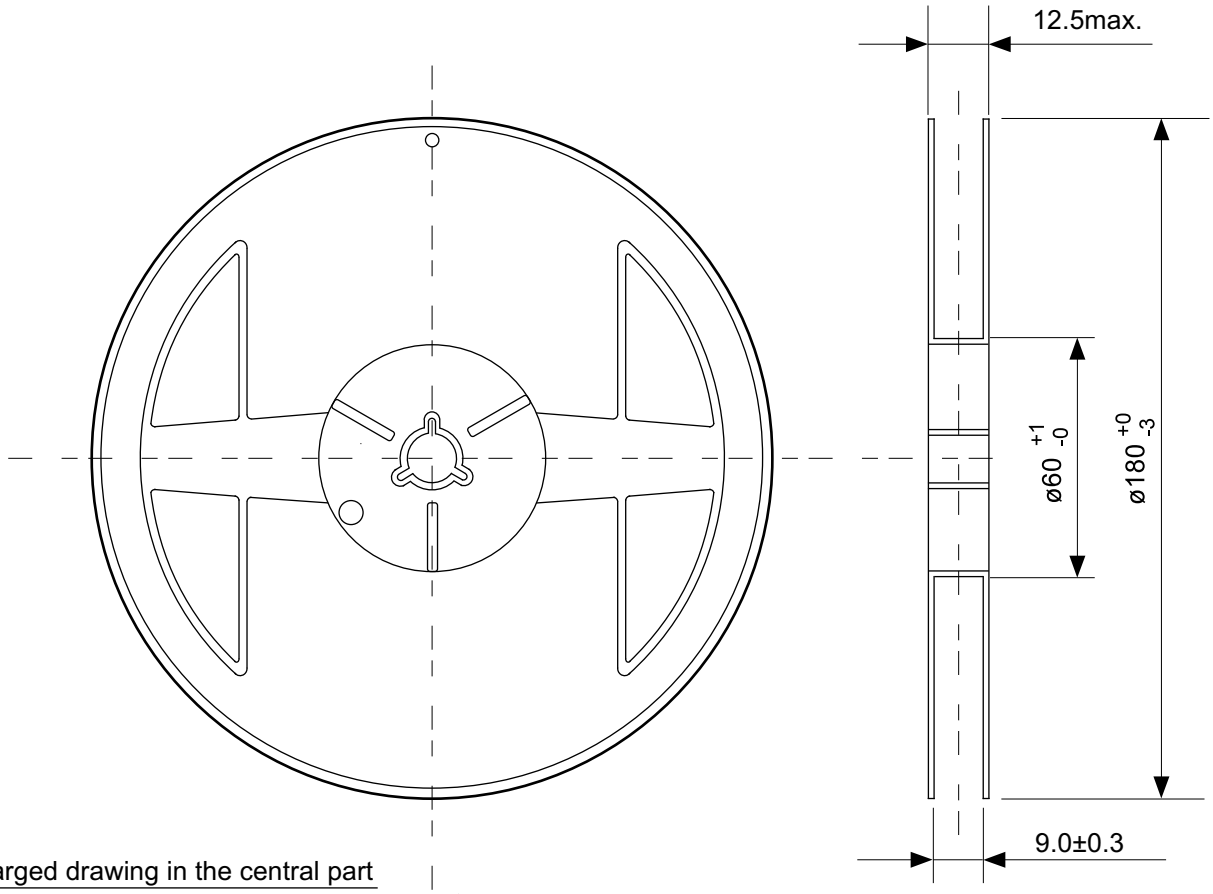
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

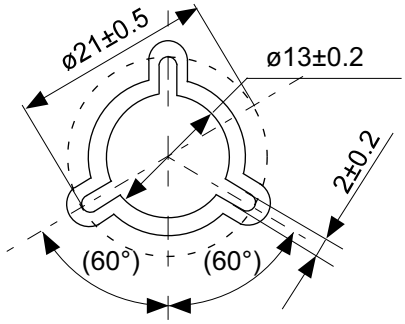


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

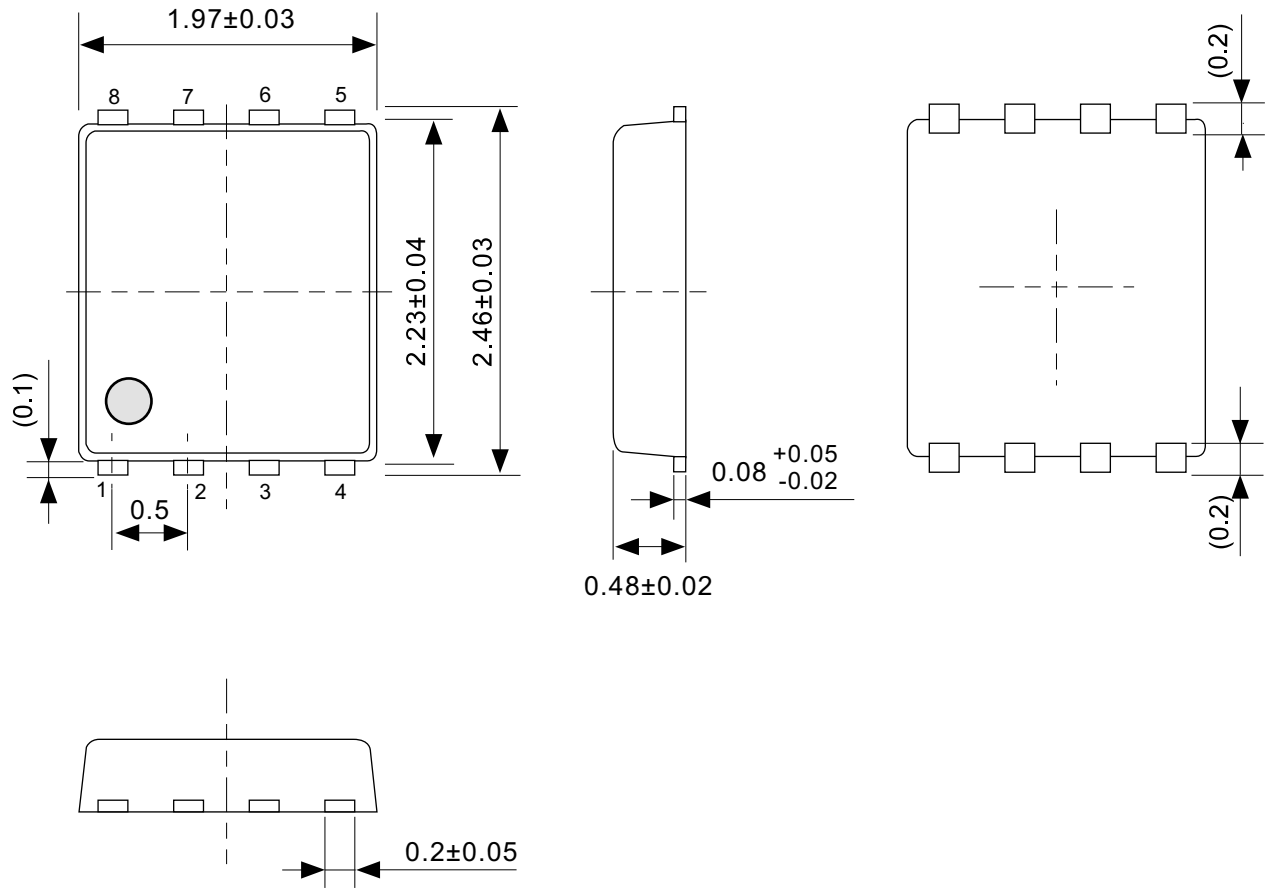


Enlarged drawing in the central part



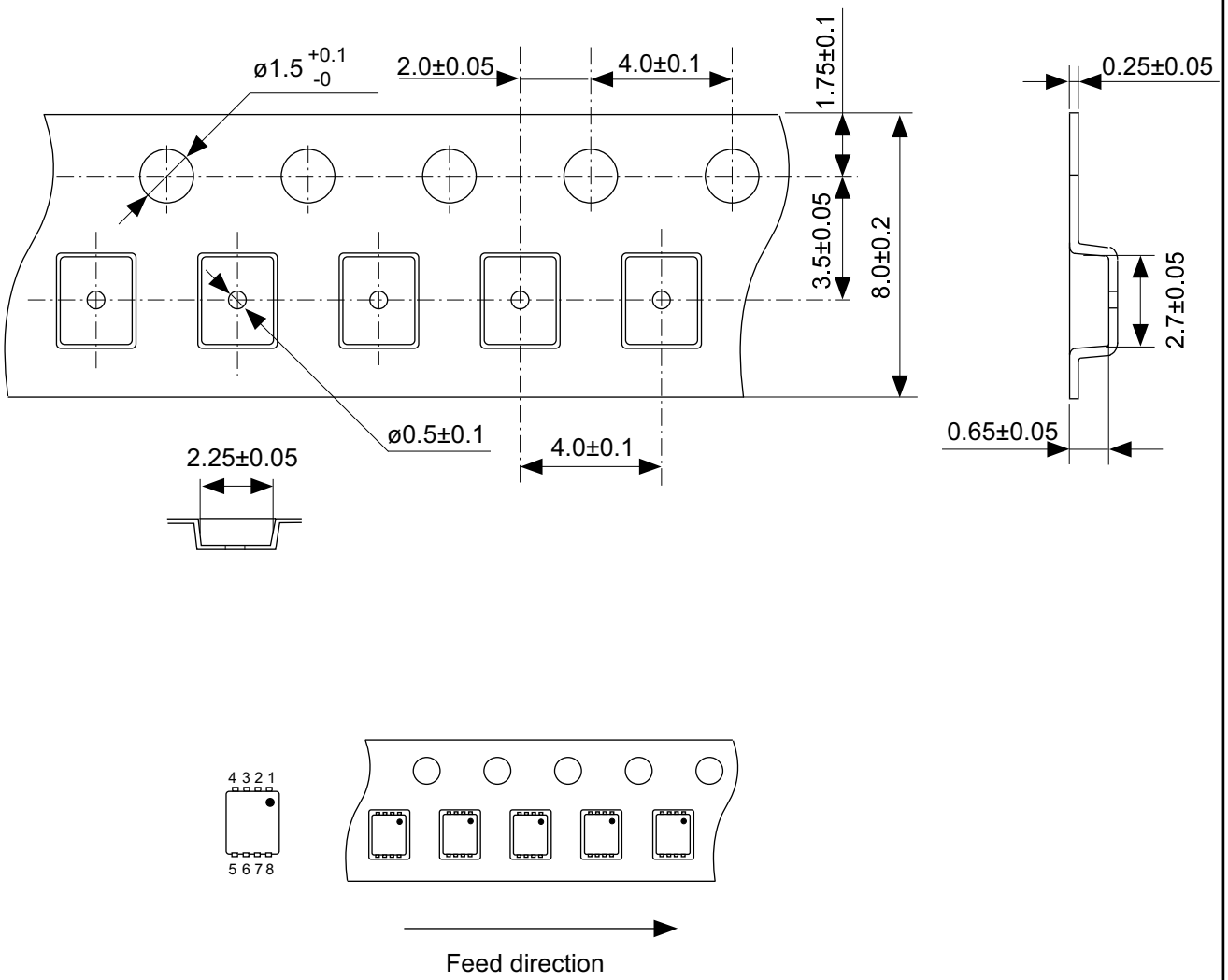
No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



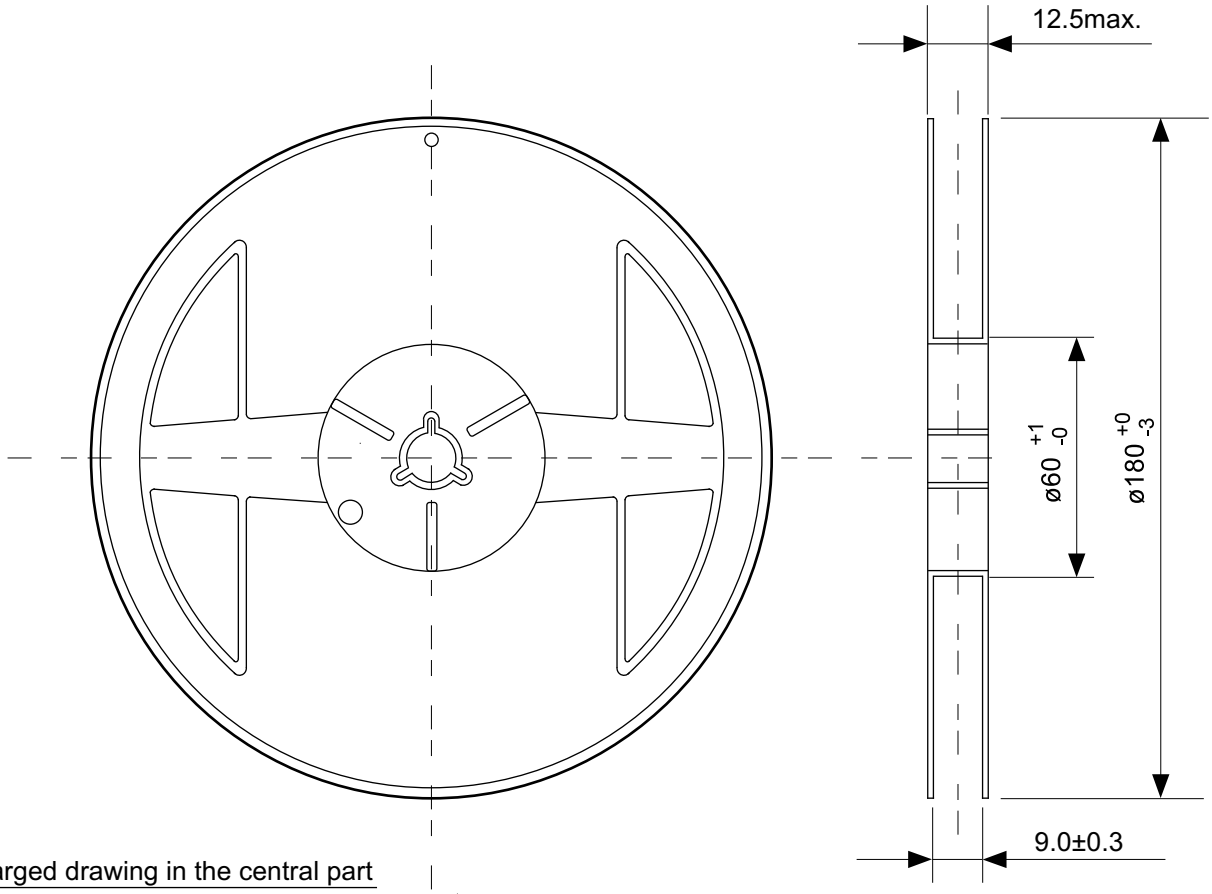
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

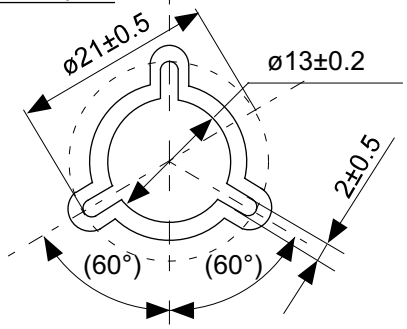


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

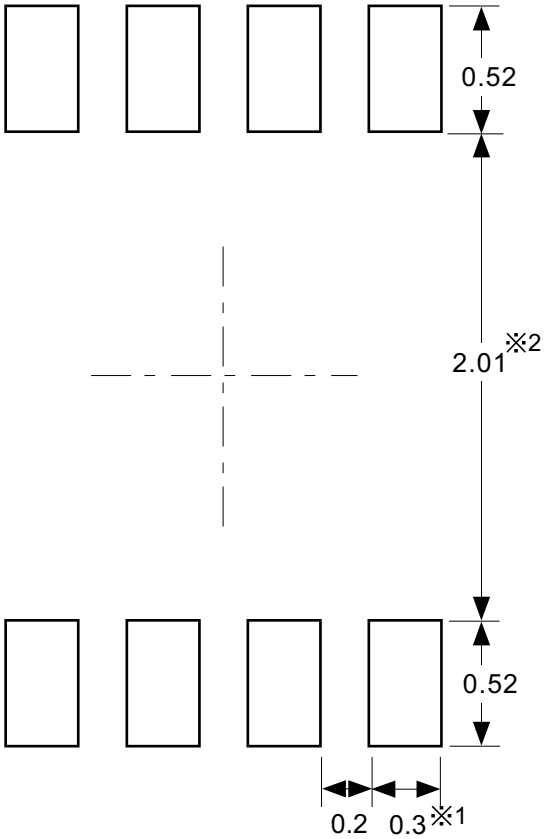


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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