ALPHA & OMEGA SEMICONDUCTOR

AOT460
N-Channel Enhancement Mode Field Effect Transistor

General Description

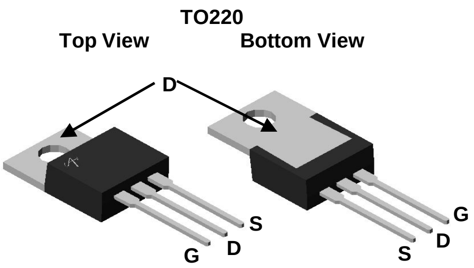
The AOT460/L uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in UPS, high current switching applications.
AOT460and AOT460L are electrically identical.

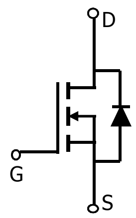
- -RoHS Compliant
- -Halogen Free

Features

V_{DS} (V) = 60V
I_D = 85 A (VGS = 10V) → $I_D = 85$ A ($V_{GS} = 10$V)
$R_{DS(ON)} < 7.5m\Omega$ ($V_{GS} = 10$V)

100% UIS Tested!





Absolute Maximum Ratings T_A=25℃ unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current[G]	T_C=25℃	I_D	85	A
	T_C=100℃		66	
Pulsed Drain Current [C]		I_{DM}	340	
Avalanche Current [C]		I_{AR}	80	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	320	mJ
Power Dissipation [B]	T_C=25℃	P_D	268	W
	T_C=100℃		134	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	℃

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	Steady-State	$R_{\theta JA}$	45	60	℃/W
Maximum Junction-to-Case [B]	Steady-State	$R_{\theta JC}$	0.45	0.56	℃/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250uA, V_{GS}=0V		60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V				10	μA
			T_J=55°C			50	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA		2	2.95	4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V		340			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=30A			6.3	7.5	mΩ
			T_J=125°C		10.5	13	
g_{FS}	Transconductance	V_{DS}=5V, I_D=30A			90		S
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]					85	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz			3800	4560	pF
C_{oss}	Output Capacitance				430		pF
C_{rss}	Reverse Transfer Capacitance				190		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz			1.5	2.3	Ω
SWITCHING PARAMETERS							
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=30A			68	88	nC
Q_g(4.5V)	Total Gate Charge				33		nC
Q_{gs}	Gate Source Charge				15		nC
Q_{gd}	Gate Drain Charge				19		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=1Ω, R_{GEN}=3Ω			18		ns
t_r	Turn-On Rise Time				35		ns
$t_{D(off)}$	Turn-Off DelayTime				44		ns
t_f	Turn-Off Fall Time				23		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=30A, dI/dt=100A/μs			53	64	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=30A, dI/dt=100A/μs			98		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25° C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C.
G. The maximum current rating is limited by bond-wires.
Rev1: Jan. 2009

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

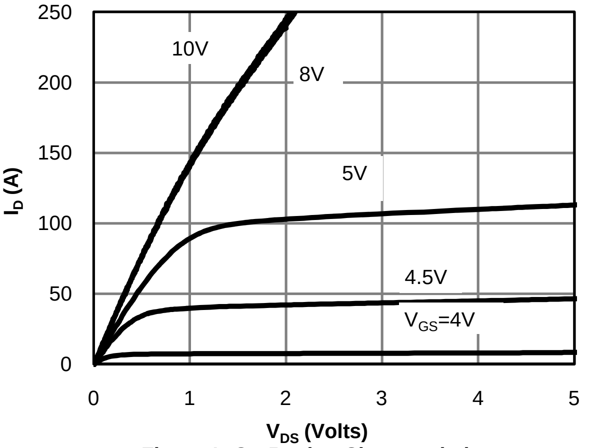


Figure 1: On-Region Characteristics

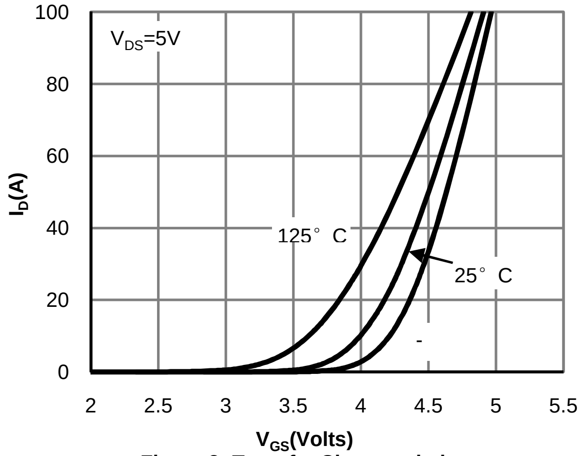


Figure 2: Transfer Characteristics

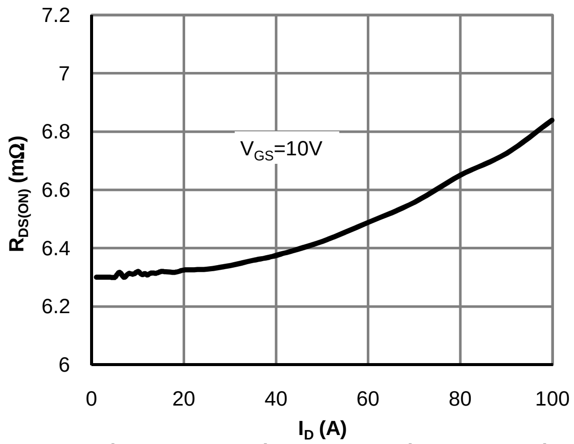


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

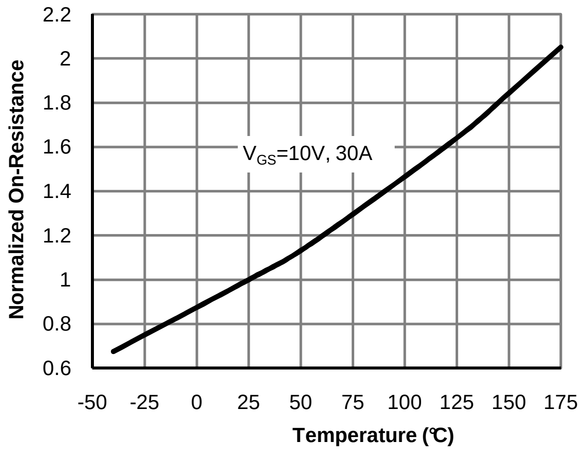


Figure 4: On-Resistance vs. Junction Temperature

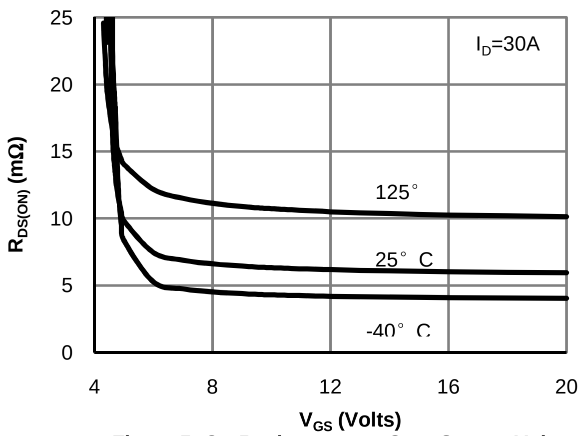


Figure 5: On-Resistance vs. Gate-Source Voltage

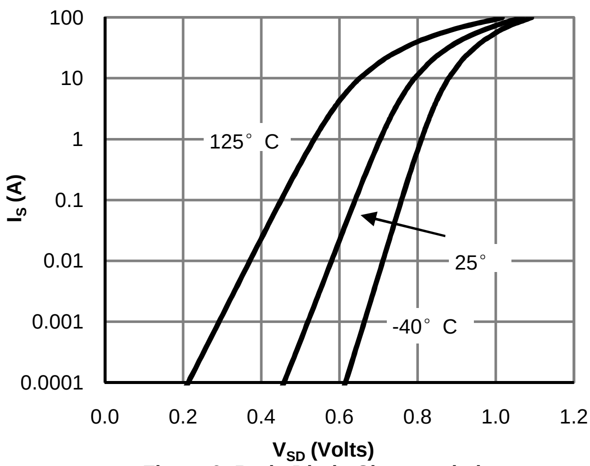


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

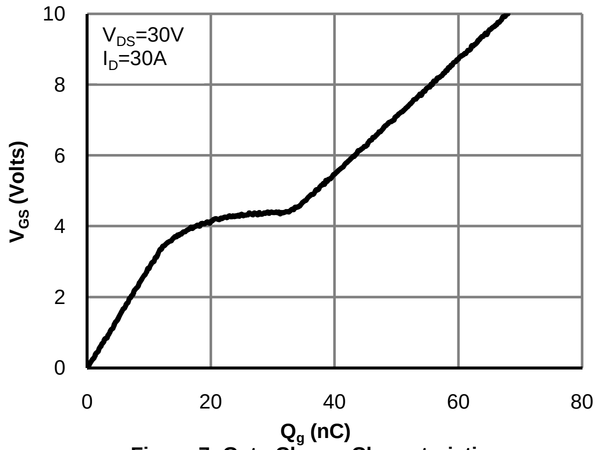


Figure 7: Gate-Charge Characteristics

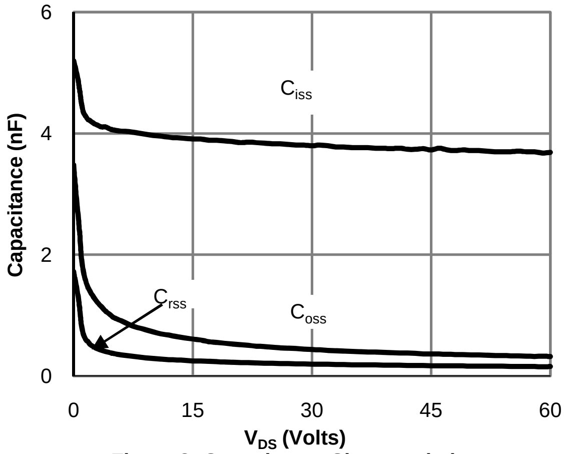


Figure 8: Capacitance Characteristics

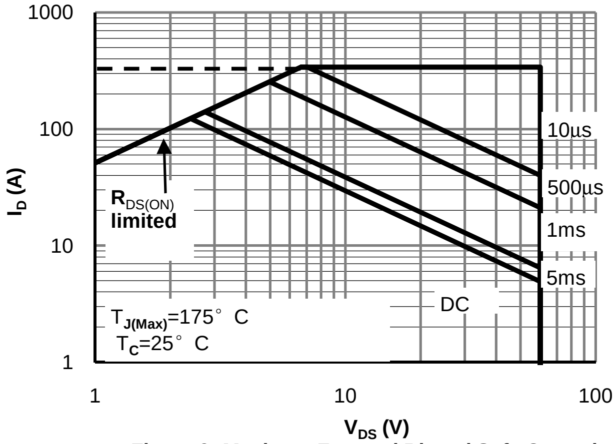


Figure 9: Maximun Forward Biased Safe Operating Area (Note F)

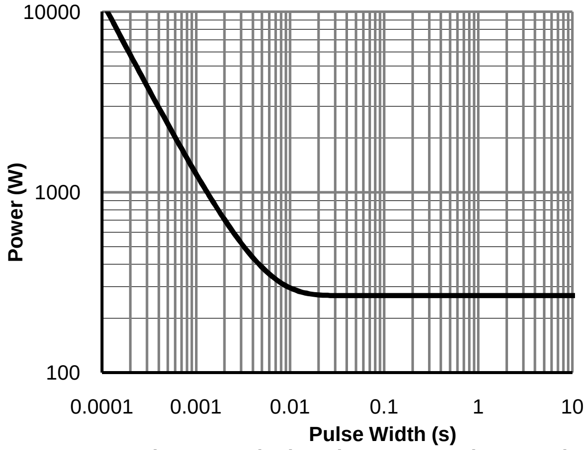


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

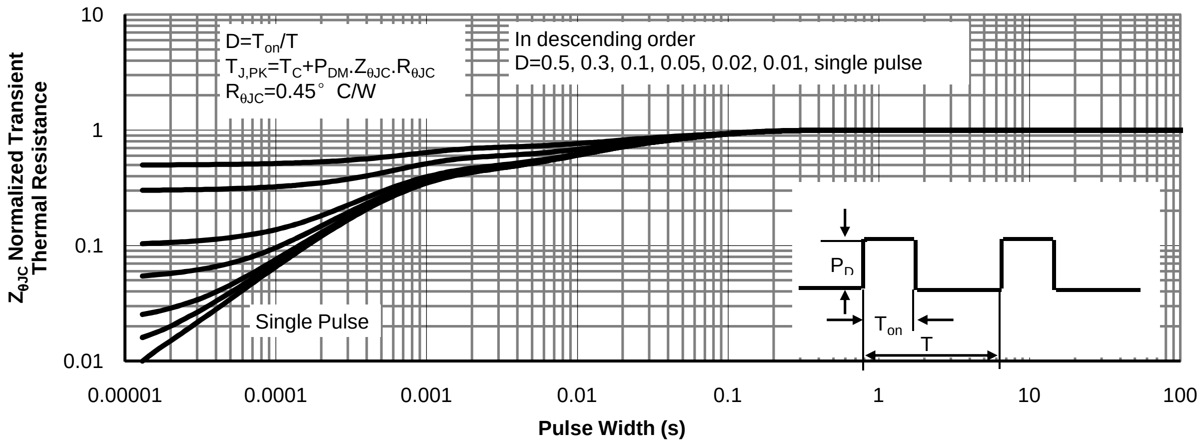


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

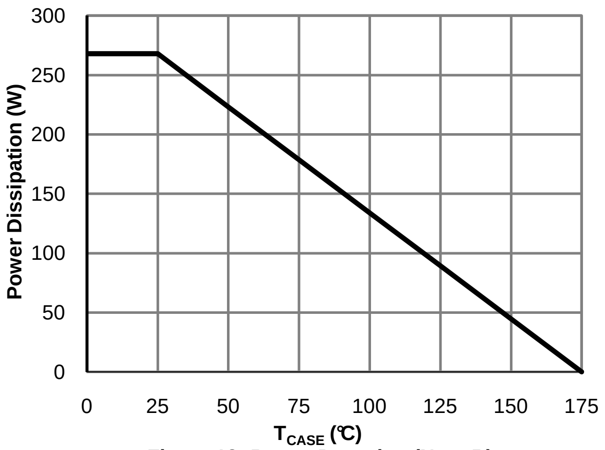


Figure 13: Power De-rating (Note B)

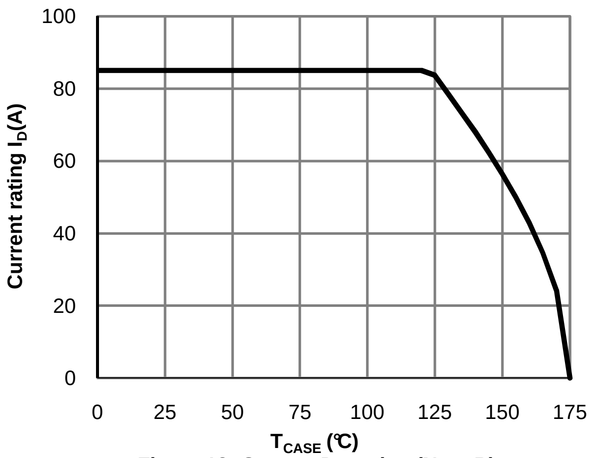


Figure 12: Current De-rating (Note B)

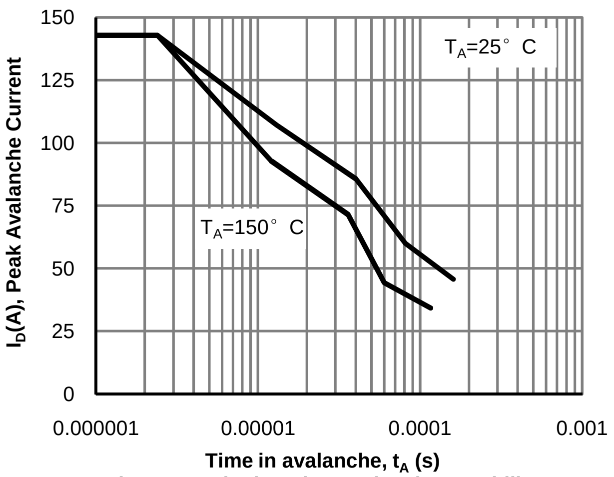
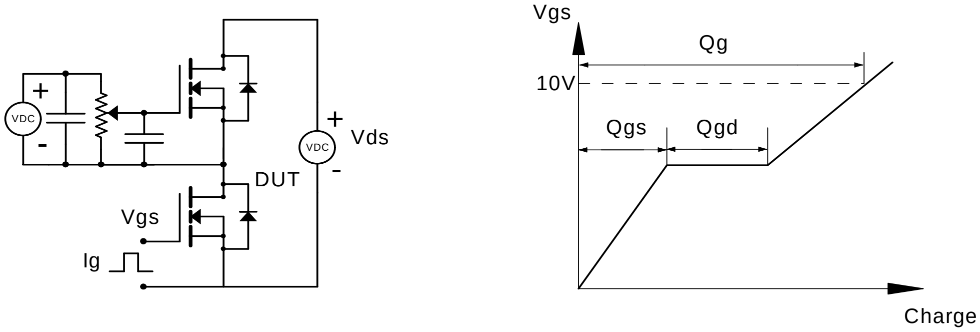
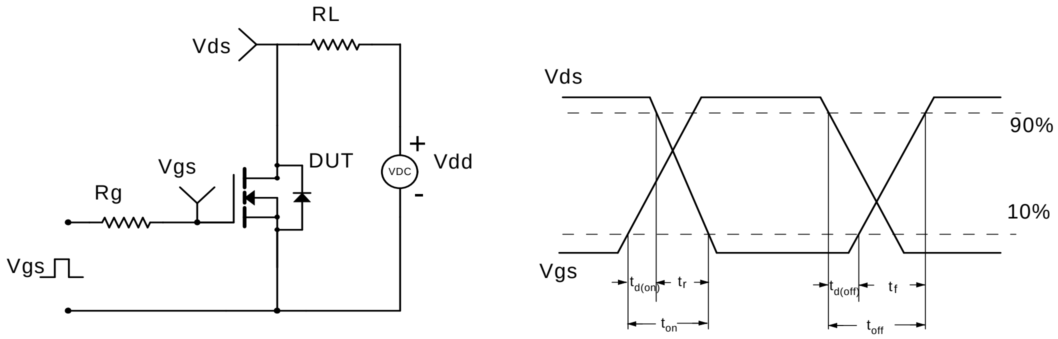


Figure 10: Single Pulse Avalanche capability

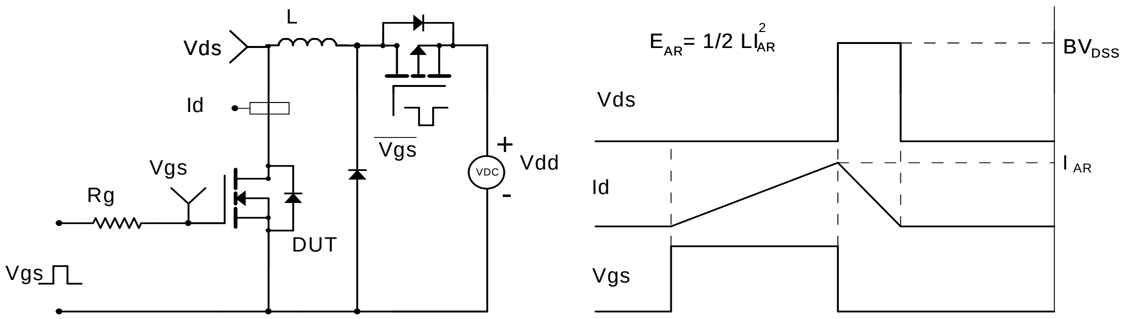
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms