

### Applications

- 3G/HD/SD-SDI Video Switchers
- 3G/HD/SD-SDI Video Routers
- 3G/HD/SD-SDI Video Distribution Amplifiers
- DVB-ASI Equipment

### Features

- SMPTE 259-C, 292, 424M, and DVB ASI Compliant
- Greater than 0.6 UI Input Jitter Tolerance
- Integrated 50  $\Omega$  input termination
- Input equalization and output de-emphasis for 40" of FR4 trace

- 230 mW power consumption (1.2 V operation)
- Integrated regulators for multi-voltage operation (1.2 V - 3.3 V)
- Electrically independent input, output, and core supply rails
- Output enable/disable and configurable auto or manual bypass mode
- Automatic and manual modes for rate indication and selection
- Loss of Lock (LOL), Loss of Signal (LOS) and data rate Indication
- Two-wire and four-wire serial interface programmability
- Industrial operating temperature range (-40 °C to +85 °C)
- Optional recovered serial clock output

The M21245 is a serial digital video reclocker with integrated trace equalization and automatic rate detect (ARD) circuitry. It operates at SDI data rates ranging from 270 Mbps to 2970 Mbps and is compliant to SMPTE 424M, SMPTE 292, and SMPTE 259M-C. At 270 Mbps it also supports DVB-ASI.

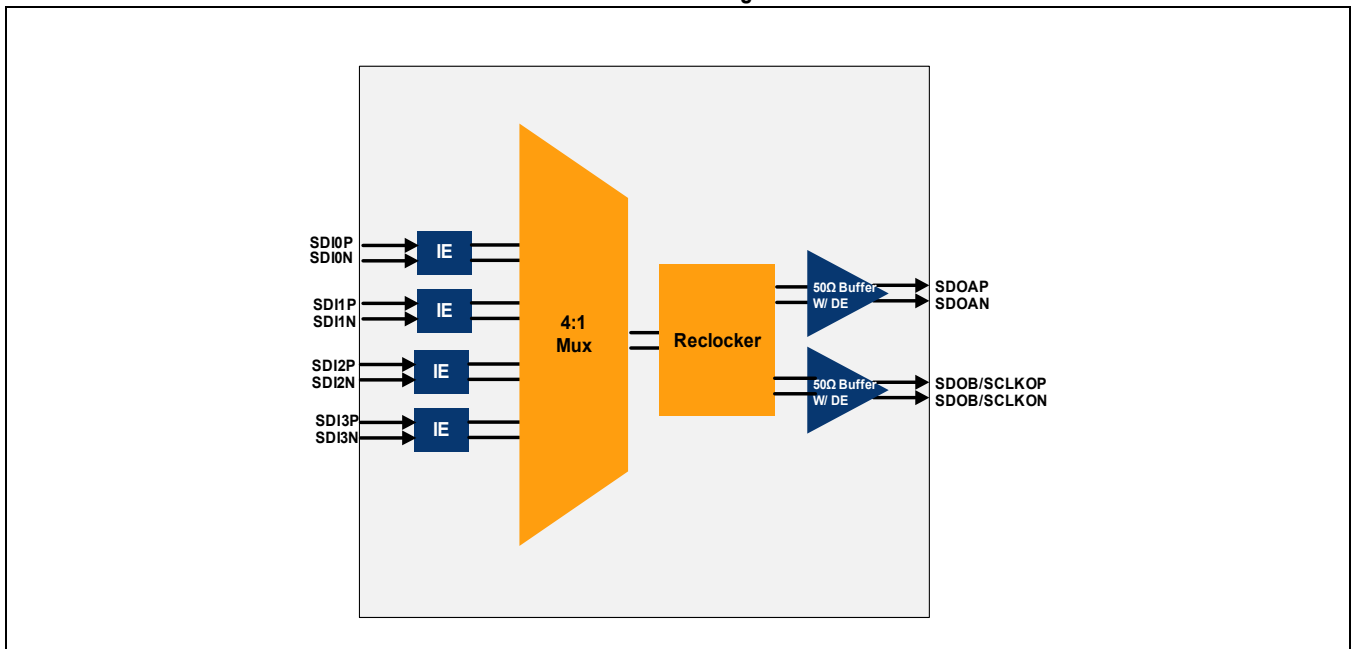
The M21245 has an input jitter tolerance (IJT) of greater than 0.6 unit intervals (UI) and can provide retimed serial outputs with very low output jitter. The reclocker requires a single external 27 MHz crystal, which is used as the reference clock for all four channels. It includes per-lane analog input equalization for up to 40" of FR4 trace and two connectors in addition to output de-emphasis.

This device features integrated supply regulators allowing it to be powered from 1.2 V, 1.8 V, 2.5 V, or 3.3 V supply voltages. When operating at 1.2 V, it consumes only 230 mW at 3G-SDI. Furthermore, the power rails for the core, input, and output circuitry are electrically independent and as such may be connected to different voltage rails on the board. This feature allows the M21245 to be DC-coupled to any upstream or downstream device regardless of its input/output voltage level.

The device may be configured by setting the internal registers through standard two-wire and four-wire interfaces.

The M21245 is offered in a green and RoHS compliant, 6 mm x 6 mm, 40-pin QFN package.

M21245 Block Diagram



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### Ordering Information

Part Number	Package	Operating Temperature
M21245G-15*	6x6 mm, 40-pin QFN package	-40 °C to 85 °C

\* The letter "G" designator after the part number indicates that the device is RoHS compliant. The RoHS compliant devices are backwards compatible with 225 °C reflow profiles.

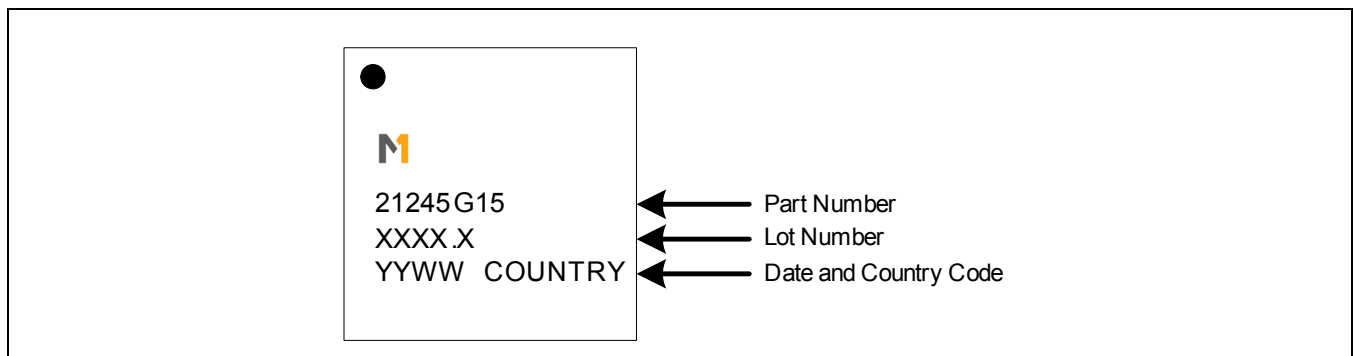
### Revision History

Revision	Level	Date	Description
V6	Released	December 2015	Updated package drawing, <a href="#">Figure 3-12</a> . Package effective as of July 2014. Added package dimensions, <a href="#">Figure 3-13</a> .
H (V5)	Released	July 2012	<a href="#">Section 4.6.2</a> : Revised four-wire interface description.
G (V4)	Released	January 2012	<a href="#">Table 1-8</a> : Added 2-state input to $V_{IH}$ and $V_{IL}$ . <a href="#">Section 4.9</a> : Advised using a 10 k $\Omega$ pull-up to $DV_{DDIO}$ when in "interrupt mode."
F (V3)	Released	January 2011	In the previous revision of this device, M21245G-14, the Loss of Lock (LOL) alarm would be erroneously triggered when pathological signals were used. As a workaround, MACOM recommended masking the faulty LOL alarm by setting register 96h bit[6] to 1b. In the latest version, M21245G-15, the faulty algorithm has been corrected. Therefore, the requirement to mask the LOL alarm has been removed from this data sheet. Please note that this change has been made to be fully backwards compatible, so setting register 96h bit[6] to 1b, while unnecessary, will not affect the function or performance of the device. Ordering Information: Updated part number from -14 to 15. <a href="#">Table 1-7</a> : Updated XTAL and reference clock electrical specifications, input Impedance typical from 400 k $\Omega$ to 200 $\Omega$ i input amplitude range from 1.6 V-2.0 V to 0.8 V to 1.2 V and max rise/fall times from 1 ns max to 2 ns typical and 6 ns max. <a href="#">Table 1-8</a> : Updated $V_{OH}$ from 0.75 to 0.80 x $DV_{DDIO}$ and $I_{OL}$ from 24 mA to 3 mA. <a href="#">Figure 3-1</a> : Updated the pinout diagram to reflect new pin naming convention. <a href="#">Table 3-1</a> : Updated table to reflect new pin naming convention. <a href="#">Figure 3-6</a> : Updated figure from pull-down to pull-up. <a href="#">Table 5-1</a> : Updated register map table. Added all registers needed to perform EEPROM checksum. Register 0Ah: Added this register to provide programmability to SDOB De-emphasis. Register 0Eh: De-featured xAlarm status mode. Register 0Eh: Modified Interrupt mode xAlarm pulse widths to reflect their true value with respect to a 10K $\Omega$ pull up resistor. Register 82h: Updated chip version from 03h to 04h. <a href="#">Figure 4-3</a> : Updated self bias diagram to reflect conditions necessary for self biased mode. <a href="#">Section 4.6.2</a> : Updated to include the detailed timing description for four-wire interface when conducting a write operation followed by a read operation. <a href="#">Table 4-6</a> : Updated the EEPROM Addresses. <a href="#">Table 4-7</a> : Updated the EEPROM Addresses. <a href="#">Section 4.7.1</a> : Clock Recovery: Updated the data to clock delay to 60 ps. <a href="#">Section 4.2</a> : Included conditions necessary for self biased mode. <a href="#">Section 4.6.1</a> : Added note defeating xAlarm pin in hardware control mode. <a href="#">Section 4.9</a> : De-featured xAlarm pin in hardware mode and limited xAlarm pin usage to Interrupt Mode only.

### Revision History

Revision	Level	Date	Description
E (V2)	Released	August 2010	Status for floating logic state for pin MF4 changed from reclocker bypass to normal operation in <a href="#">Table 3-1</a> and <a href="#">Table 4-2</a> . Status for floating logic state for pin MF5 changed from reclocker bypass to normal operation in <a href="#">Table 3-1</a> and <a href="#">Table 4-2</a> . Changed MF4 and MF5 levels in <a href="#">Table 3-1</a> . Added note to <a href="#">Figure 4-3</a> . Changed MF4 and MF5 levels in <a href="#">Table 4-2</a> . Changed MF3 function description in <a href="#">Table 4-5</a> .
D (V1)	Released	May 2010	Refer to D revision for details.
C (V1P)	Preliminary	April 2010	Refer to C revision for details.
B (V2A)	Advance	October 2009	Refer to B revision for details.
A (V1A)	Advance	September 2008	Initial release.

### M21245 Marking Diagram



## 1.0 Electrical Characteristics

Unless noted otherwise, specifications apply for typical recommended operating conditions shown in Table 1-2, with  $DV_{DDO} = 1.2\text{ V}$ ,  $AV_{DDCORE} = 1.2\text{ V}$ ,  $DV_{DDCORE} = 1.2\text{ V}$ ,  $AV_{DDI} = 1.2\text{ V}$ , CML inputs/outputs at 800 mV differential ( $R_{LOAD} = 50\ \Omega$ ), and PRBS  $2^{10} - 1$  test pattern at 2.97 Gbps.

**Table 1-1. Absolute Maximum Ratings**

Symbol	Parameter	Note	Minimum	Maximum	Unit
$AV_{DDI}$	Analog supply for input circuitry	1, 3	-0.5	3.6	V
$AV_{DDO}$	Analog supply for output circuitry	1, 3	-0.5	3.6	V
$DV_{DDIO}$	Digital supply for input/output circuitry	1, 3	-0.5	3.6	V
$DV_{DDCORE}$	Digital core positive supply	1, 3	-0.5	1.5	V
$AV_{DDCORE}$	Analog core positive supply	1, 3	-0.5	1.5	V
$T_{STORE}$	Storage temperature	1, 3	-65	150	°C
$V_{IN, CMOS}$	DC input voltage (CMOS)	1, 3	-0.5	$DV_{DDIO} + 0.5$	V
$V_{IN}$	DC input voltage (PCML)	1, 3	-0.5	$AV_{DDI} + 0.5$	V
$V_{ESD, HBM}$	Human Body Model (HBM)	1, 2, 3	-2	2	kV
$V_{ESD, CDM}$	Charge Device Model (CDM)	1, 2, 3	-500	500	V
LU	Latch up @ 85 °C	1, 3	-150	150	mA
$I_{IN, PCML}$	Maximum high-speed input current	1, 3	-100	100	mA

**NOTES:**

1. Exposure of the device beyond the minimum/maximum limits may cause permanent damage. Limits listed in the above table are stress limits only, and do not imply functional operation within these limits.
2. HBM and CDM per JEDEC class 2 (JESD22-A114-B).
3. Limits listed in the above table are stress limits only and do not imply functional operation within these limits.

**Table 1-2. Recommended Operating Conditions**

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
DV <sub>DDIO</sub>	Digital I/O positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV <sub>DDI</sub>	Analog input positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV <sub>DDO</sub>	Analog output positive supply	—	1.14	1.2, 1.8, 2.5, or 3.3	3.47	V
AV <sub>DCCORE</sub>	Analog core positive supply	—	1.14	1.2	1.26	V
DV <sub>DCCORE</sub>	Digital core positive supply	—	1.14	1.2	1.26	V
T <sub>CASE</sub>	Case temperature	—	-40	25	+85	°C

**Table 1-3. Power Consumption Specifications**

Symbol	Parameter	Conditions	Note	Typical	Maximum	Unit
P <sub>TOTAL</sub>	Total power consumption	AV <sub>DDI</sub> = AV <sub>DDO</sub> =DV <sub>DDIO</sub> =DV <sub>DCCORE</sub> = AV <sub>DCCORE</sub> = 1.2 V SDO Swing Level 1	1, 3	230	290	mW
			1, 4	250	350	
P <sub>TOTAL</sub>	Total power consumption	AV <sub>DDI</sub> = AV <sub>DDO</sub> =DV <sub>DDIO</sub> =DV <sub>DCCORE</sub> = AV <sub>DCCORE</sub> = 1.2 V SDO Swing Level 2	1, 3	240	300	mW
			1, 4	260	360	
P <sub>TOTAL</sub>	Total power consumption	DV <sub>DCCORE</sub> = AV <sub>DCCORE</sub> = 1.2 V AV <sub>DDI</sub> = DV <sub>DDIO</sub> = 1.2 V AV <sub>DDO</sub> = 1.8 V SDO Swing Level 3	1, 3	260	370	mW
			1, 4	270	450	
		DV <sub>DCCORE</sub> = AV <sub>DCCORE</sub> = 1.2 V AV <sub>DDI</sub> = DV <sub>DDIO</sub> = 3.3 V AV <sub>DDO</sub> = 3.3 V SDO Swing Level 3	2, 3	720	1070	

**NOTE:**

1. Internal regulators disabled.
2. Internal regulators enabled.
3. SDOB/SCLK disabled.
4. SDOB/SCLK enabled.
5. Airflow = 0 m/s.

**Table 1-4. SDI High Speed (Positive Current Mode Logic) Input Electrical Specifications**

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDI input data rate	SD Operation (SMPTE 259M,C)		—	270	—	Mbps
		HD Operation (SMPTE 292)		—	1485, 1483.5	—	Mbps
		3G Operation (SMPTE 424M)		—	2970, 2967	—	Mbps
		Reclocker bypassed		18	—	3400	Mbps
$V_{IN}$	Differential input voltage	At the chip input (point blank) Input equalization disabled LOS enabled (default setting)	1, 3	300	800	1600	mV <sub>PPD</sub>
$V_{ICM}$	Input common mode voltage	At the chip input (point blank) Input equalization disabled LOS enabled		$AV_{DDI}-0.6$	—	$AV_{DDI}+0.1$	V
$R_{IN}$	Input termination to $AV_{DDI}$			40	50	60	$\Omega$
IE	Input equalization		2	—	0, 2, 4, 6	—	dB

**NOTE:**

- For example: 1200 mV<sub>PP</sub> differential = 600 mV<sub>PP</sub> for each single-ended terminal.
- These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
- When using long traces and input equalization enabled, MACOM recommends a minimum input swing of 400 mV<sub>PPD</sub>. With pathological patterns, DC-coupling produces the best results.

Table 1-5. SDO High Speed (Positive Current Mode Logic) Output Electrical Specifications

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
DR	SDO output data rate	SD operation (SMPTE 259M,C)		—	270	—	Mbps
		HD operation (SMPTE 292)		—	1485, 1483.5	—	
		3G operation (SMPTE 424M)		—	2970, 2967	—	
		Reclocker bypassed		18	—	3400	
F <sub>CLOCK</sub>	Serial clock output frequency	SD operation (SMPTE 259M,C)	1, 7	—	270	—	MHz
		HD operation (SMPTE 292)		—	1485, 1483.5	—	
		3G operation (SMPTE 424M)		—	2970, 2967	—	
V <sub>OUT</sub>	Differential output swing (peak to peak, differential)	Swing level 1	2	470	600	720	mV <sub>PPD</sub>
		Swing level 2	2	600	800	970	
		Swing level 3	2,3	960	1200	1500	
V <sub>OCM</sub>	Output common mode voltage	DC-coupled	2, 6	—	AV <sub>DDO</sub> -V <sub>OUT</sub> /4	—	
t <sub>R</sub> /t <sub>F</sub>	SDO output rise/fall time	From 20%-80% of the swing for all levels		—	85	130	ps
t <sub>R</sub> /t <sub>F</sub> DIFF	Rise/Fall time mismatch	From 20%-80% of the swing for all levels	6	—	—	30	ps
DCD <sub>DATA</sub>	Output duty cycle distortion	For all data rates	4	—	—	15	ps
R <sub>OUT</sub>	Output termination to AV <sub>DDO</sub>			40	50	60	Ω
DE	Output de-emphasis		5	—	0, 2, 4, 6	—	dB

**NOTE:**

- Serial clock output enabled.
- Differential swing is maximum output level (de-emphasis is disabled or maximum level when de-emphasis is enabled), maximum level includes overshoot.
- 1200 mV swing level requires AV<sub>DDO</sub> to be 1.8 V or higher.
- Measured in reclocked mode.
- These values correspond to: off, small, medium, and large respectively. The small setting is not available in hardware mode.
- Guaranteed by design.
- See Section 4.7 for information on clock data alignment.

**Table 1-6. Reclocker Specifications**

Symbol	Parameter	Conditions	Note	Minimum	Typical	Maximum	Unit
$t_{LOCK}$	Lock time (asynchronous)	Automatic rate detection enabled	1	—	—	6	ms
$F_{LBW, PEAK}$	Loop bandwidth peaking	—	1	—	0.1	—	dB
$F_{LBW}$	Loop bandwidth (nominal setting)	3G operation (2.97 Gbps)	1	—	1.7	—	MHz
		HD operation (1.485 Gbps)	1	—	0.85	—	
		SD operation (270 Mbps)	1	—	0.17	—	
$J_{TOL}$	Input jitter tolerance	3G, HD, and SD operation	2	> 0.6	—	—	UI p-p
$J_{GEN}$	Total output jitter	3G operation (2.97 Gbps)	2, 3	—	0.07	0.11	UI p-p
		HD operation (1.485 Gbps)	2, 3	—	0.04	0.06	
		SD operation (270 Mbps)	2, 3	—	0.02	0.05	

**NOTE:**

- 0.2 UI input jitter applied at SDI input.
- Measured with PRBS2<sup>10</sup>-1.
- Input jitter = 20 ps p-p.

**Table 1-7. XTALP/N and Reference Clock Electrical Specifications**

Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$F_{REF}$	XTAL/Ref clock frequency	3	—	27	—	MHz
$F_{REF, ppm}$	XTAL/Ref clock frequency accuracy	—	-100	0	100	ppm
$C_{LOAD}$	XTAL load capacitance	1	—	20	—	pF
$CLOCK_{JITT}$	Jitter (RMS)	2, 4	—	—	1	ps
$CLOCK_{DCT}$	Reference clock duty cycle tolerance	2	40	—	60	%
$R_{IN}$	Input impedance	2, 5	200	750	1500	$\Omega$
$V_{IN}$	Input amplitude	2	0.8	—	1.2	V
$t_R/t_F$	Rise/Fall time	2, 6	—	2	6	ns

**NOTE:**

- This capacitance is supplied internally (no external cap is required).
- When using an external reference clock source, this should be AC-coupled through a 0.1  $\mu$ F capacitor.
- When using an external clock a small increase in jitter may be seen. For best performance a crystal is recommended.
- Jitter bandwidth is from 12 kHz to 20 MHz.
- Measured with TDR module.
- 10% to 90% rise and fall times.



**Table 1-8. Digital Input/Output Electrical Characteristics**

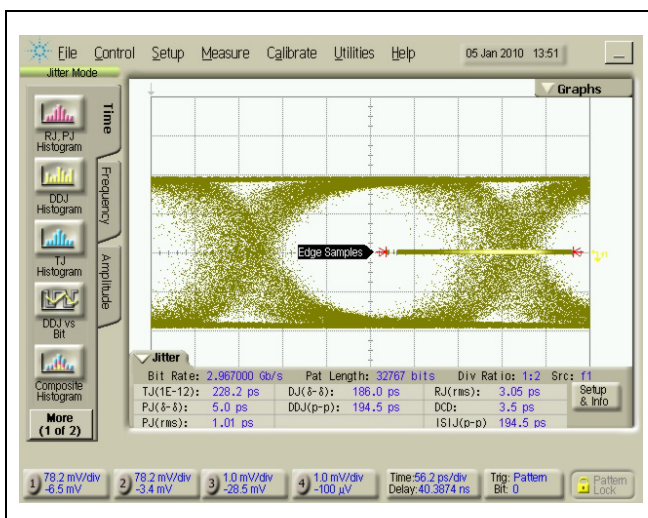
Symbol	Parameter	Note	Minimum	Typical	Maximum	Unit
$V_{OH}$	Output Logic High	1	$0.80 \times DV_{DDIO}$	$DV_{DDIO}$	—	V
$V_{OL}$	Output Logic Low	2	—	—	$0.2 \times DV_{DDIO}$	V
$V_{IH}$	Input Logic High	3, 5	$0.85 \times DV_{DDIO}$	—	$DV_{DDIO} + 0.5$	V
$V_{IF}$	Input Logic Floating	3, 5	$0.25 \times DV_{DDIO}$	—	$0.75 \times DV_{DDIO}$	V
$V_{IL}$	Input Logic Low	3, 5	0	—	$0.15 \times DV_{DDIO}$	V
$V_{IH}$	Input Logic High	4, 5	$0.75 \times DV_{DDIO}$	—	$DV_{DDIO} + 0.5$	V
$V_{IL}$	Input Logic Low	4, 5	0	—	$0.25 \times DV_{DDIO}$	V

**NOTE:**

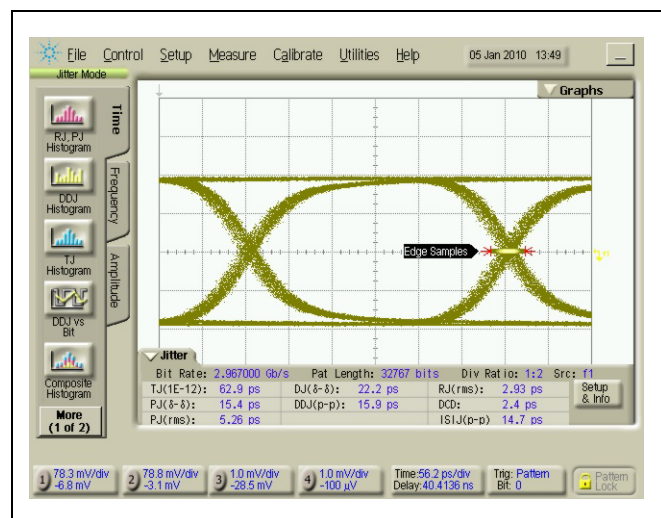
1.  $I_{OH} = -3 \text{ mA}$
2.  $I_{OL} = 3 \text{ mA}$
3. 3- state input
4. 2- state input
5. Some inputs can be 2 or 3 state. Depending on which mode is selected the threshold levels will change accordingly.

# 2.0 Typical Performance Characteristics

**Figure 2-1. Eye Diagram at Reclocker Input  
PRBS15 @ 3 Gbps**

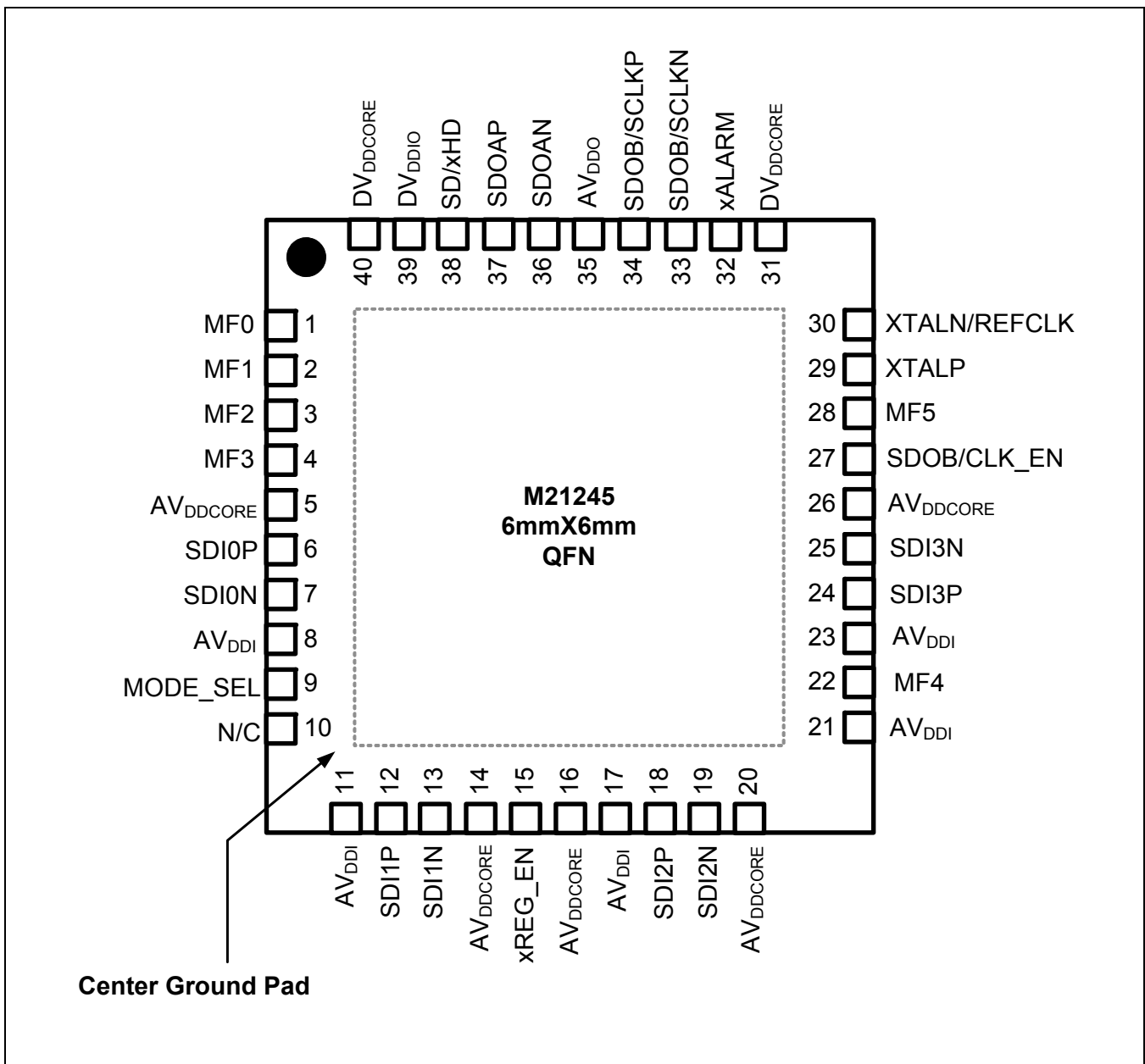


**Figure 2-2. Eye Diagram at Reclocker Output  
PRBS15 @ 3 Gbps**



### 3.0 Pinout Diagram, Pin Description, and Package Drawing

Figure 3-1. M21245 Pinout Diagram



**Table 3-1. M21245 Pin Description**

Pin Name	Pin Number(s)	Type	Description
AV <sub>DCCORE</sub>	5, 14, 16, 20, 26	Power	Analog positive supply
AV <sub>DDI</sub>	8, 11, 17, 21, 23	Power	Analog positive supply
AV <sub>DDO</sub>	35	Power	Analog positive supply
DV <sub>DCCORE</sub>	31, 40	Power	Digital core positive supply
DV <sub>DDIO</sub>	39	Power	Digital core positive supply
AV <sub>SS</sub>	Center Ground Pad	Power	Ground
SDI0P, SDI0N	6, 7	PCML input	Data input lane 0; true/complement
SDI1P, SDI1N	12, 13	PCML input	Data input lane 1; true/complement
SDI2P, SDI2N	18, 19	PCML input	Data input lane 2; true/complement
SDI3P, SDI3N	24, 25	PCML input	Data input lane 3; true/complement
SDOAP, SDOAN	37, 36	PCML output	Data output lane A; true/complement
SDOBP/SCLKP, SDOBN/SCLKN	34, 33	PCML output	Data output lane B; true/complement
XTALP	29	Reference Clock	27 MHz reference XTAL connection
XTALN/REFCLK	30	Reference Clock	27 MHz reference XTAL connection or 27 MHz reference clock input
MODE_SEL	9	CMOS Control Input	Sets the device control/configuration mode: L = Device is in register access mode with two-wire serial control (SIC2) F = Device is in hardware control mode (Hardware mode is not recommended) H = Device is in register access mode with four-wire serial control (SIC4) Termination - F
SDOB/SCLK_EN	27	CMOS Control Input	SDOB/SCLK output enable: L = SDOB/SCLK output disabled F = Serial data output enabled H = Serial clock output enabled Termination - L, 100 kΩ pull down to AV <sub>SS</sub>
xREG_EN	15	CMOS Control Input	Regulator enable control, as in Figure 3-6, but pull up resistor is to AV <sub>DDI</sub> . L = Integrated regulators enabled H = Integrated regulators disabled Termination - H, 100 kΩ pull up to AV <sub>DDI</sub>
SD/xHD	38	CMOS Output	CMOS SD/xHD rate indicator: L = HD/3G Data rate H = SD Rate

**Table 3-1. M21245 Pin Description**

Pin Name	Pin Number(s)	Type	Description
xALARM	32	Output (Open Drain)	Alarm indicator for all channels (Logical OR of all individual channel alarms). Termination - Open L = Alarm asserted H = Normal operation Serial control mode (two-wire/four-wire): xALARM in interrupt mode Hardware mode: Not supported
MF0	1	CMOS Control Input	Four-wire serial control mode: Serial clock input (SCLK) Two-wire serial control mode: Clock input from master host (SCL) Hardware mode: Unused
MF1	2	CMOS Control Input	Four-wire serial control mode: Serial data output (SO) Two-wire serial control mode: Serial data I/O (SDA) Hardware mode: Unused
MF2	3	CMOS Control Input	Four-wire serial control mode: Serial data in (SI) Two-wire serial control mode: Address bit 0 (ADD0) Hardware mode: Input trace equalization control for all SDI inputs (IE_CTRL) H = Large Input EQ F = Medium Input EQ L = Input EQ disabled
MF3	4	CMOS Control Input	Four-wire serial control mode: Active low chip select (xCS) Two-wire serial control mode: Address bit 1 (ADD1) Hardware mode: Output de-emphasis (DE) control for SDO outputs (DE_CTRL) H = Large Output DE F = Medium Output DE L = DE disabled
MF4	22	CMOS Control Input	Four-wire serial control mode: Not used. Tie to DV <sub>DDIO</sub> or leave floating Two-wire serial control mode: Address bit 2 (ADD2) Hardware mode: Reclocker bypass control (RC_BYPASS) L/F = Normal operation, reclocker not bypassed H = Reclocker bypassed
MF5	28	CMOS Control Input	Four-wire serial control mode: Not used. Tie to AVSS or leave floating Two-wire serial control mode: Address bit 3 (ADD3) Hardware mode: SDO disable control for all outputs (SDO_DIS) H = SDO disabled output logic high L/F = SDO enabled
NC	10	Reserved	Do not connect

Figure 3-2. I-Analog

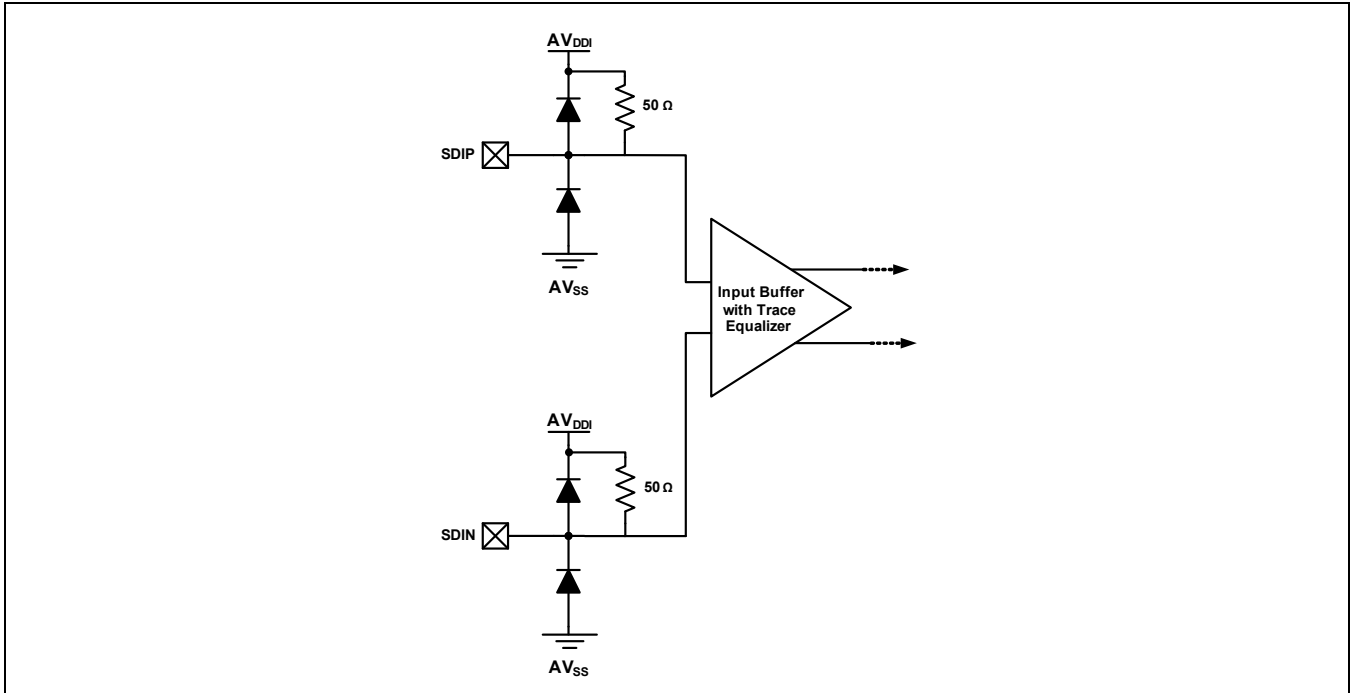


Figure 3-3. O-Analog

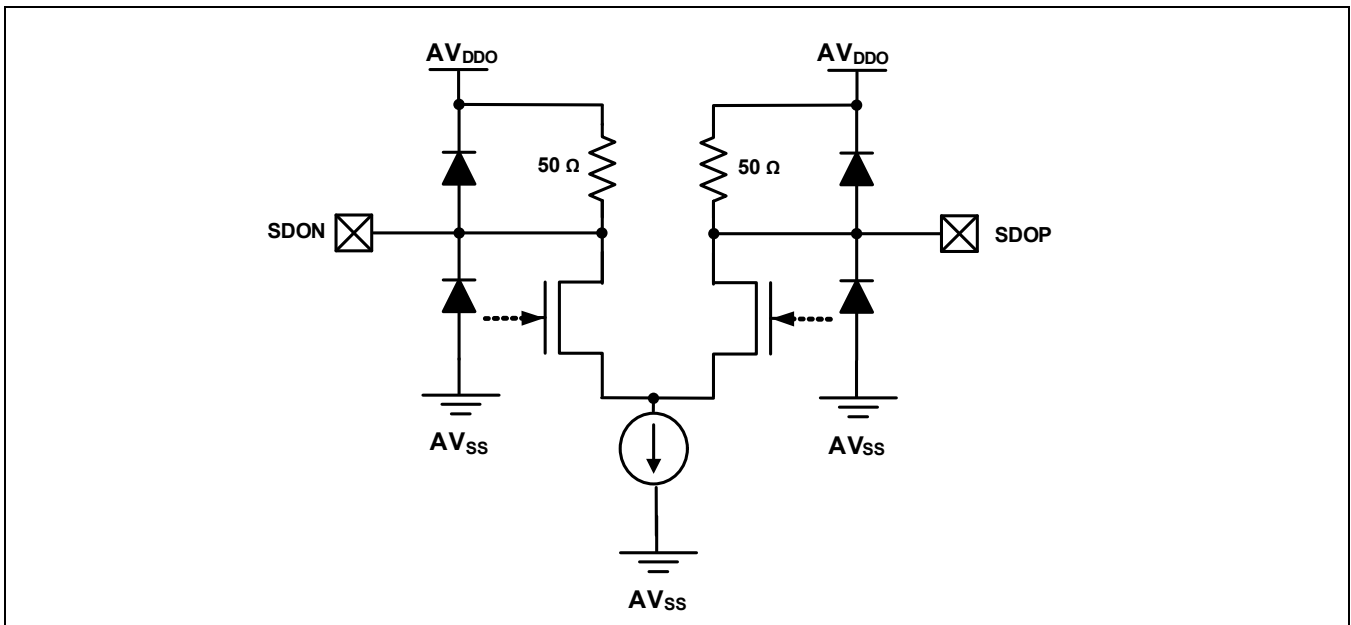


Figure 3-4. Ref Clock

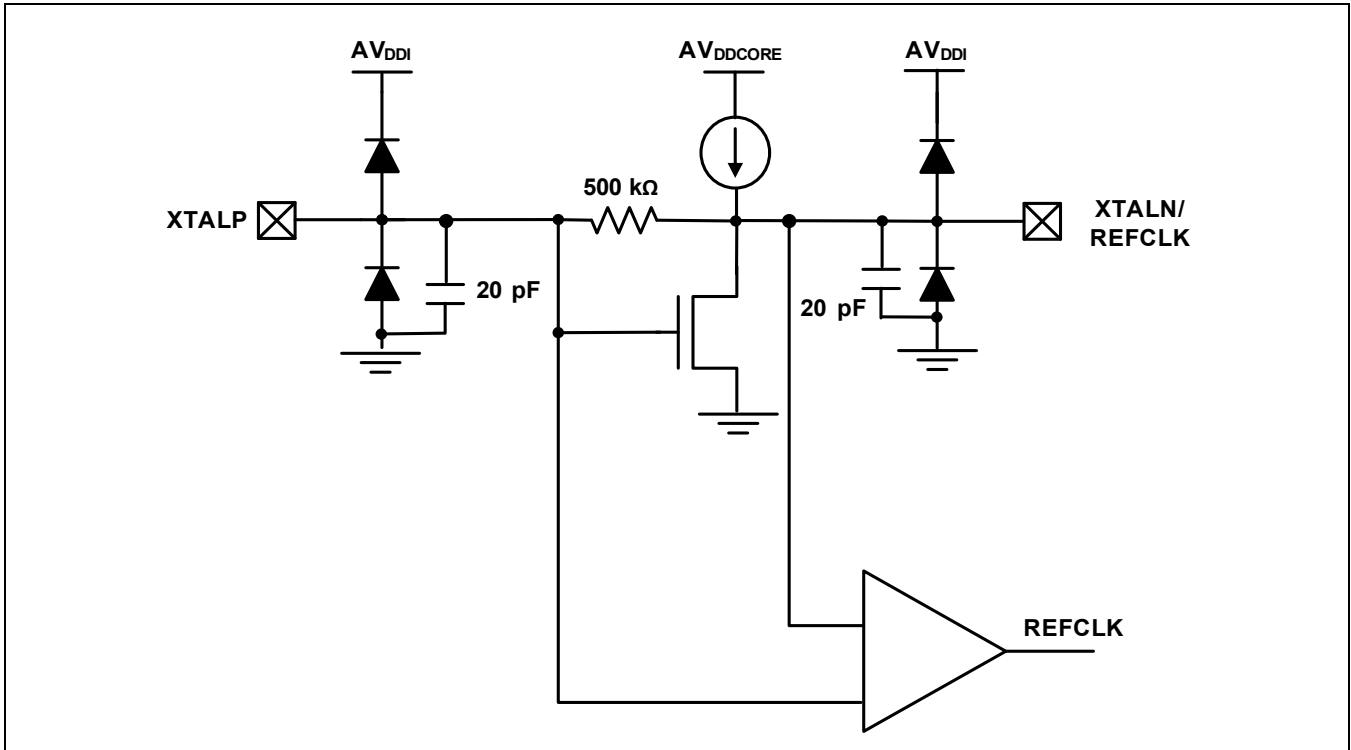


Figure 3-5. I-Digital With No Pull-up

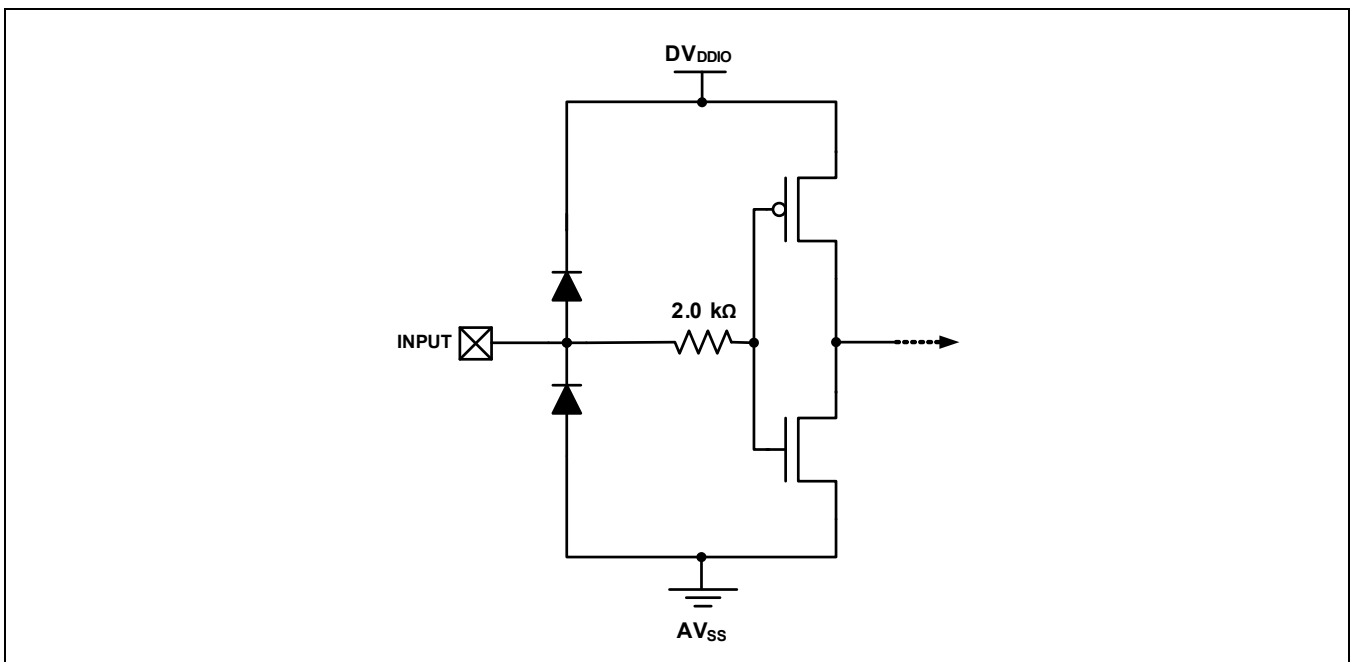


Figure 3-6. I-Digital With Pull-up

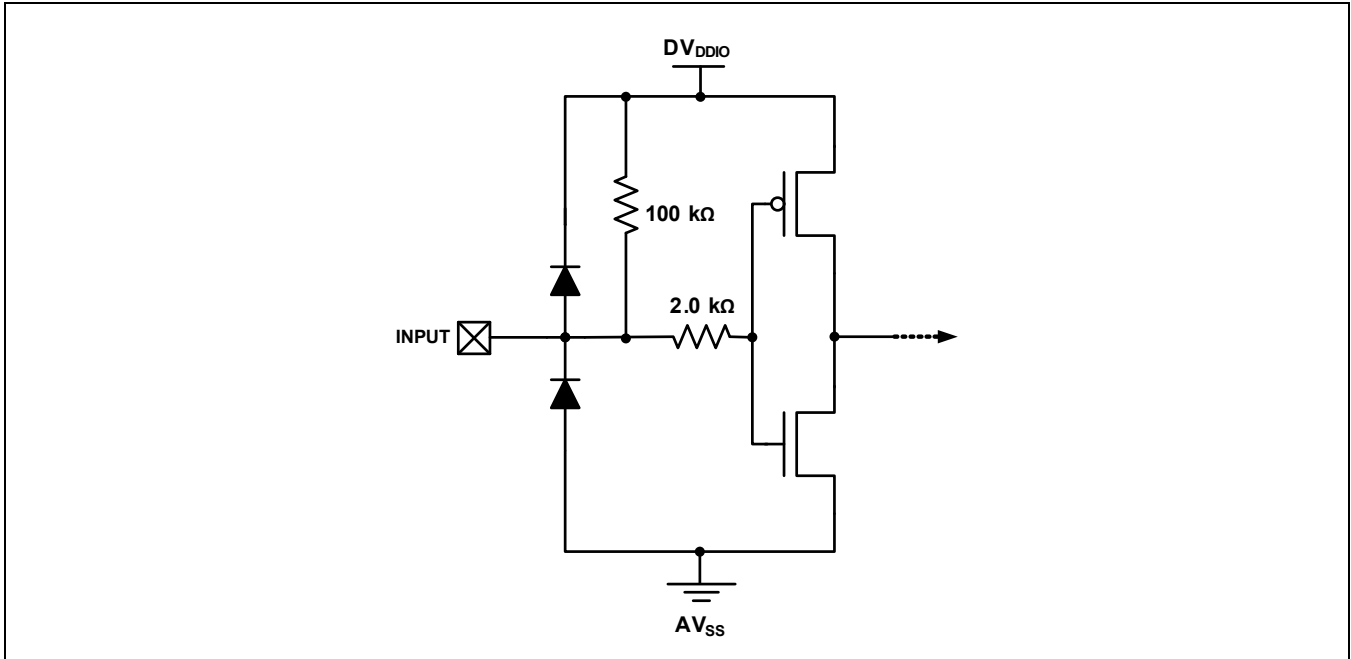


Figure 3-7. I-Digital With Pull-down

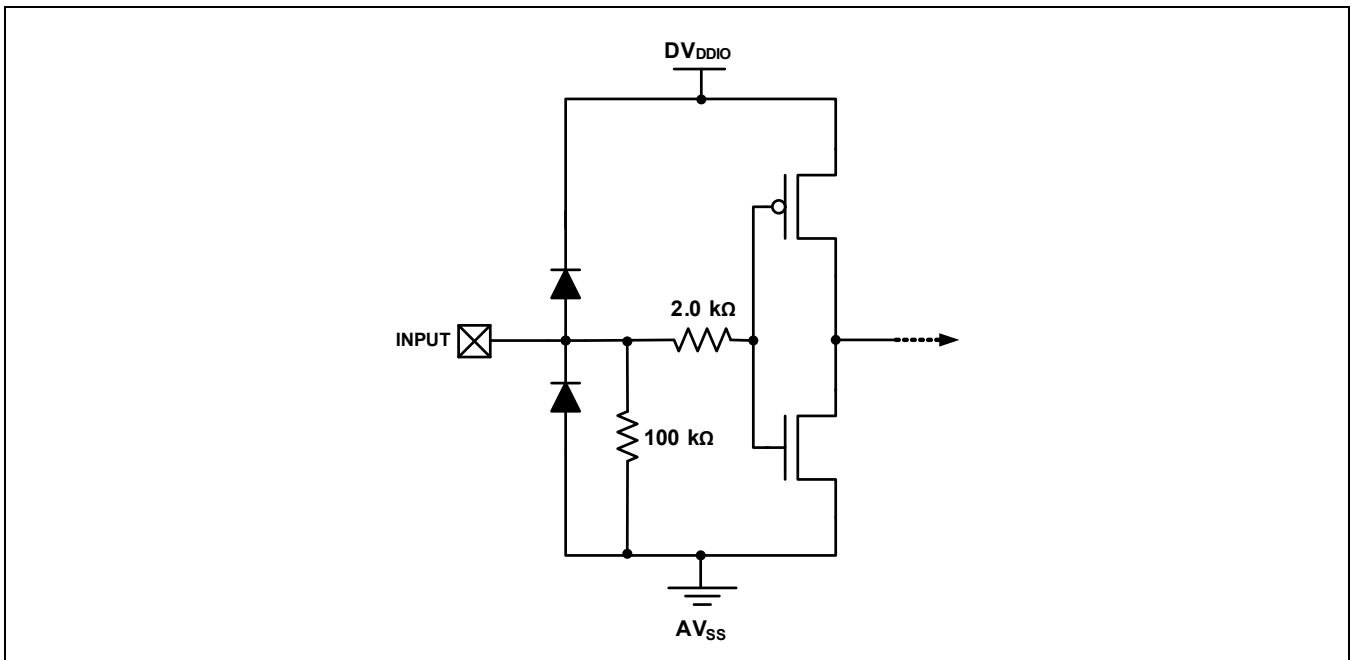




Figure 3-8. 3-State/I-Digital

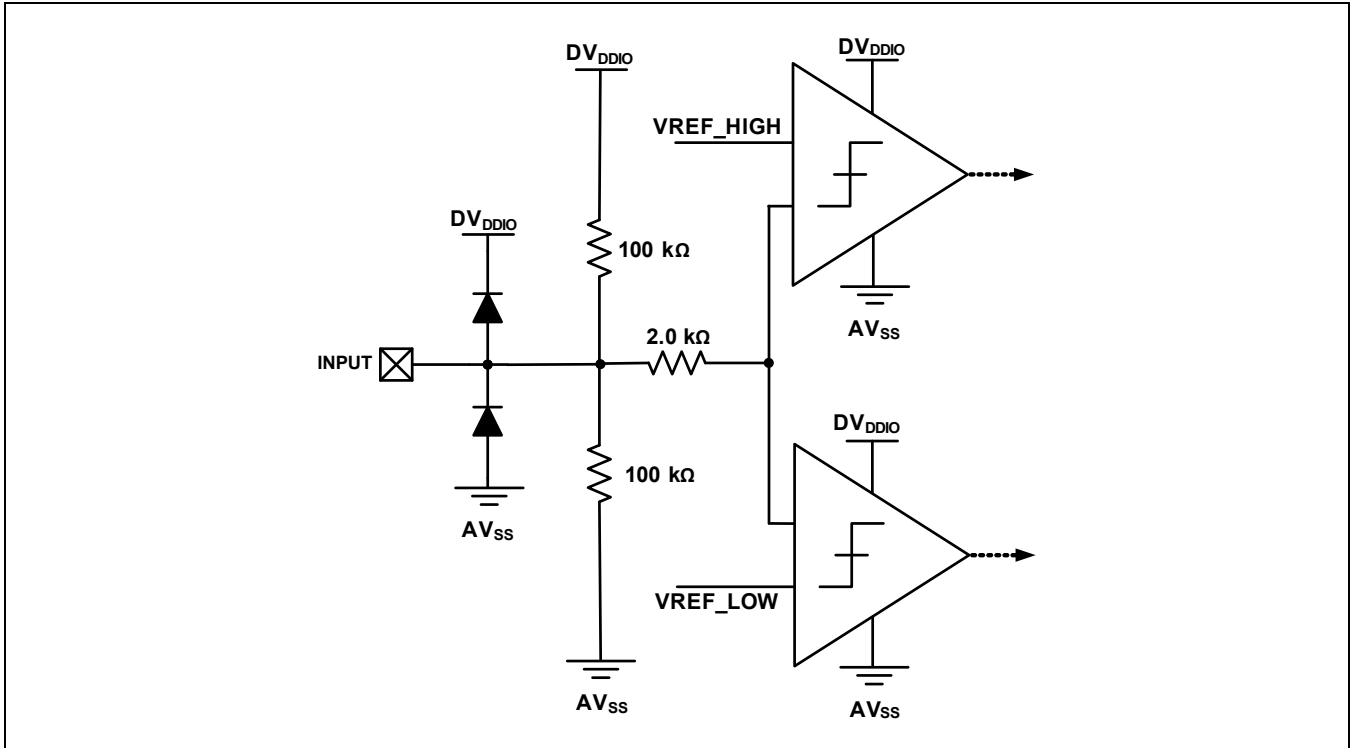


Figure 3-9. O-Digital

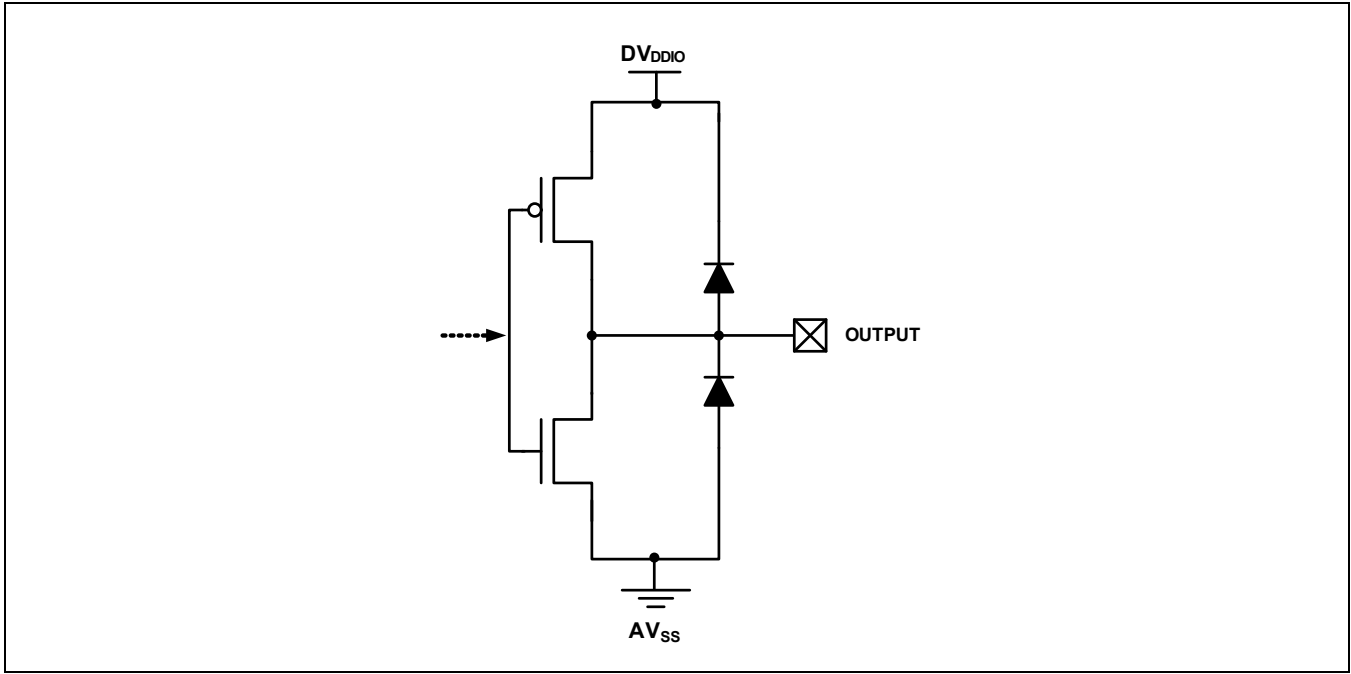
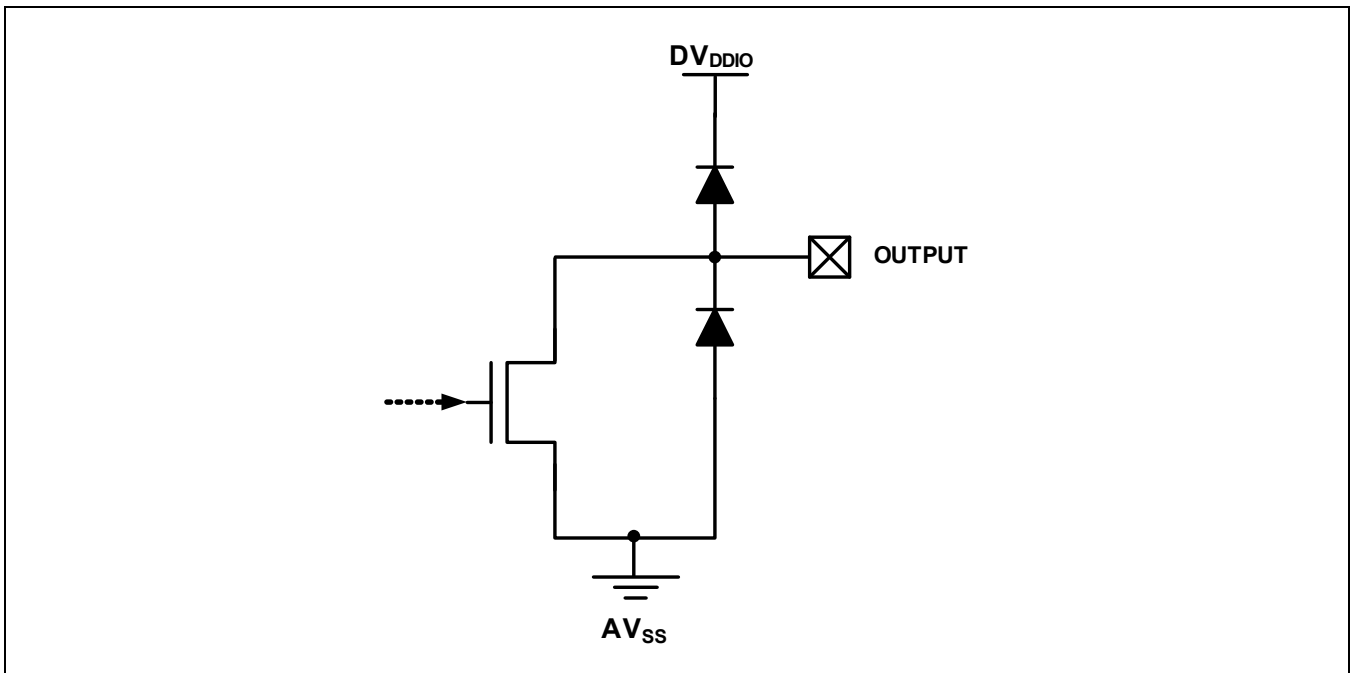


Figure 3-10. O-Open Drain



The M21245 is assembled in a 40-pin, 6 mm x 6 mm Quad Flat No-Lead (QFN) package. The exposed die paddle serves as the IC ground ( $AV_{SS}$ ), and the primary means of thermal dissipation. This die paddle should be soldered to the PCB. A cross-section of the QFN package is shown below.

**Figure 3-11. QFN Package Cross Section**

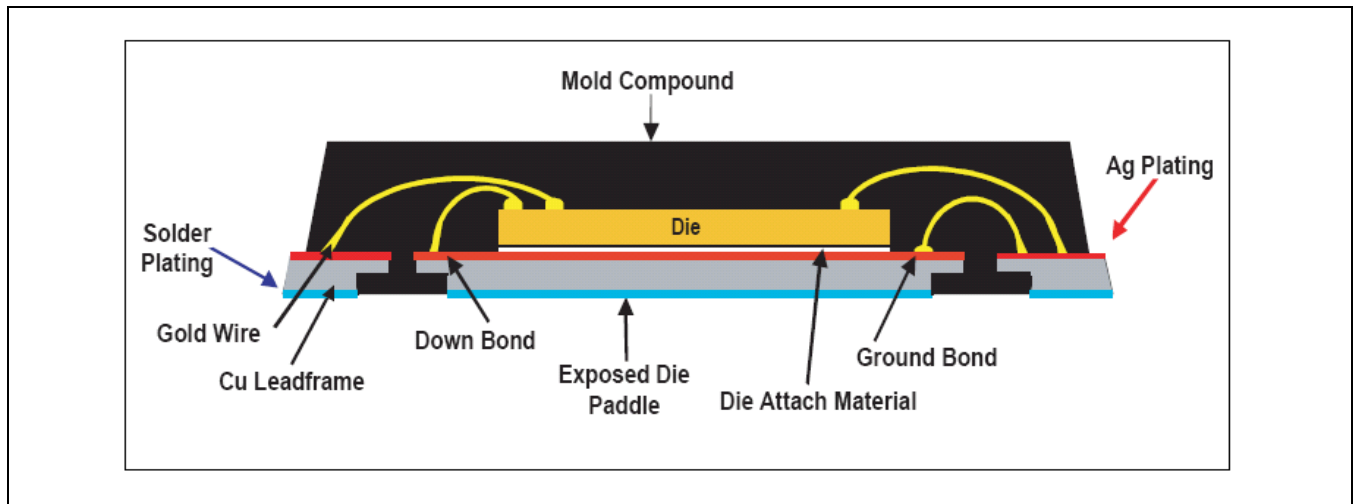


Figure 3-12. Package Outline Drawing

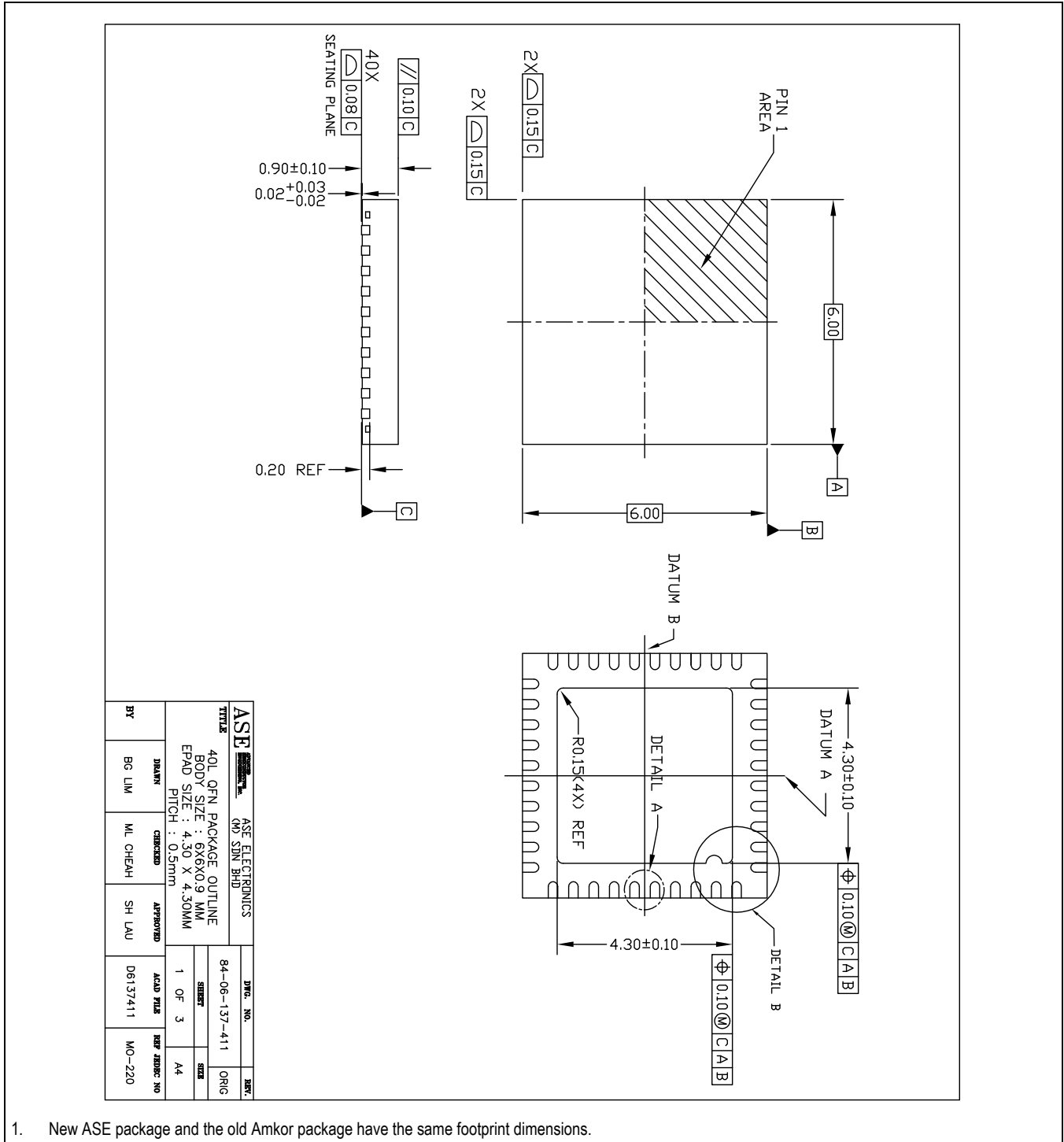
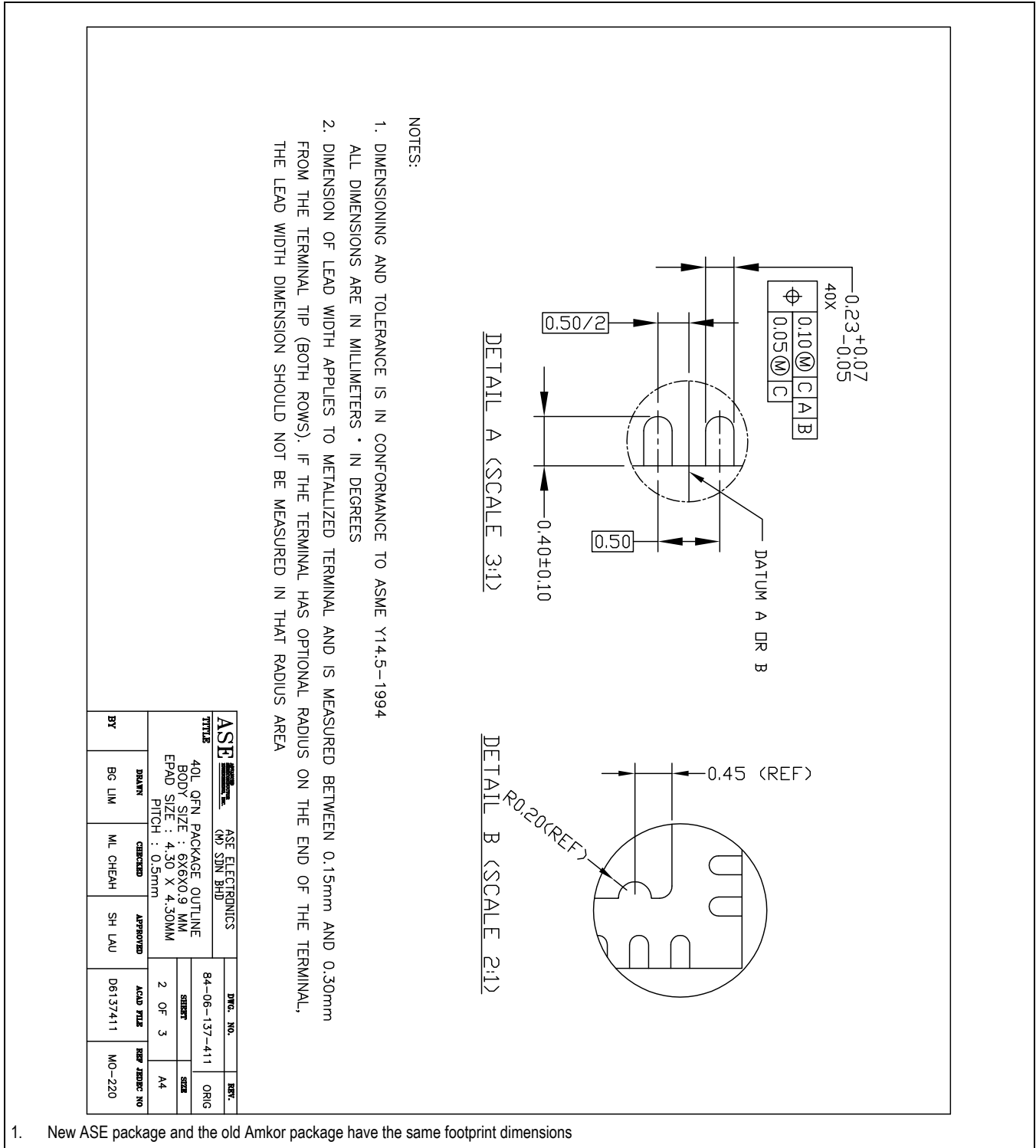


Figure 3-13. Package Dimensions



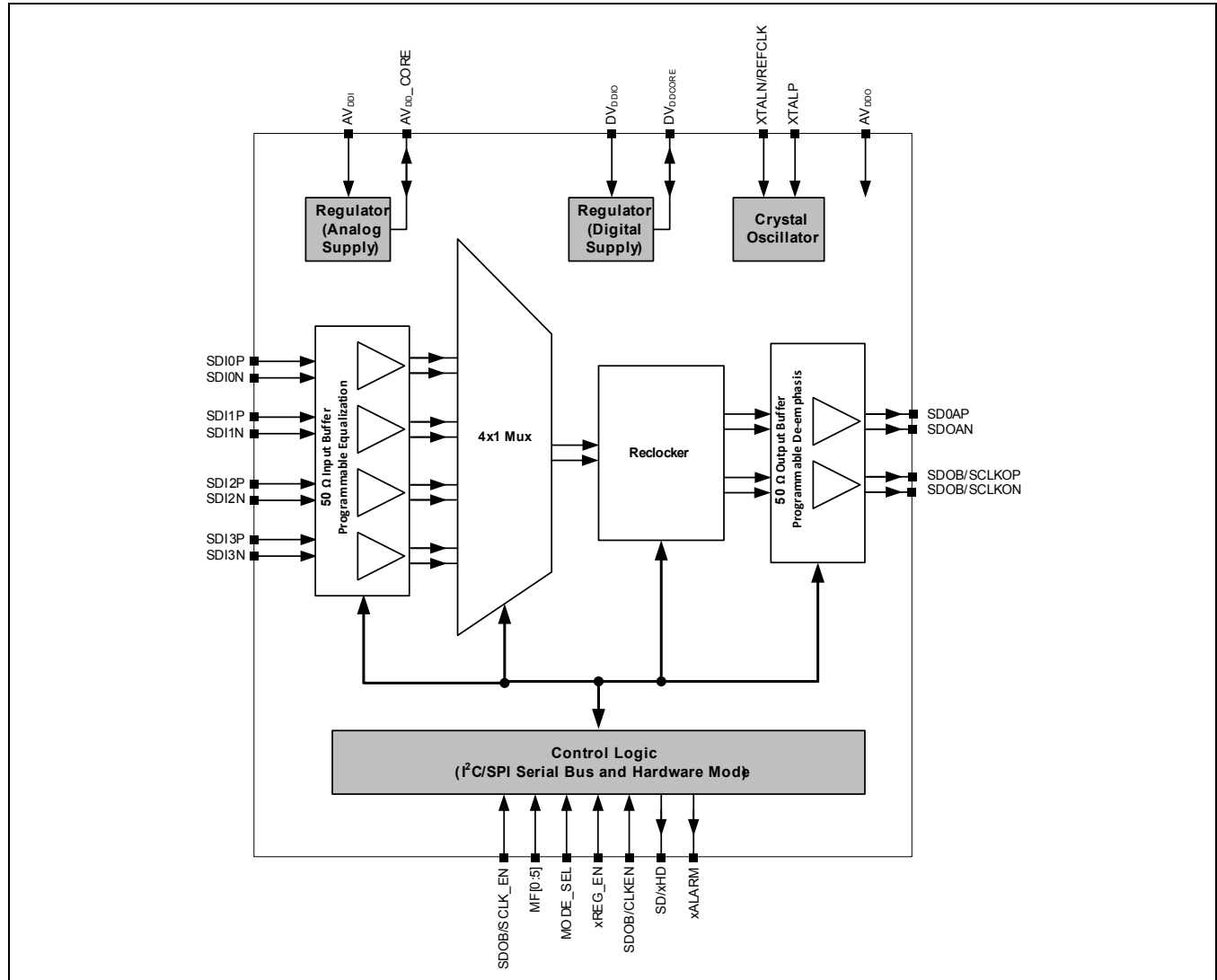
1. New ASE package and the old Amkor package have the same footprint dimensions

# 4.0 Functional Description

## 4.1 Functional Block Diagram

Figure 4-1 illustrates the M21245 block diagram. The subsequent sections provide additional detail on the operation of the device.

Figure 4-1. M21245 Block Diagram



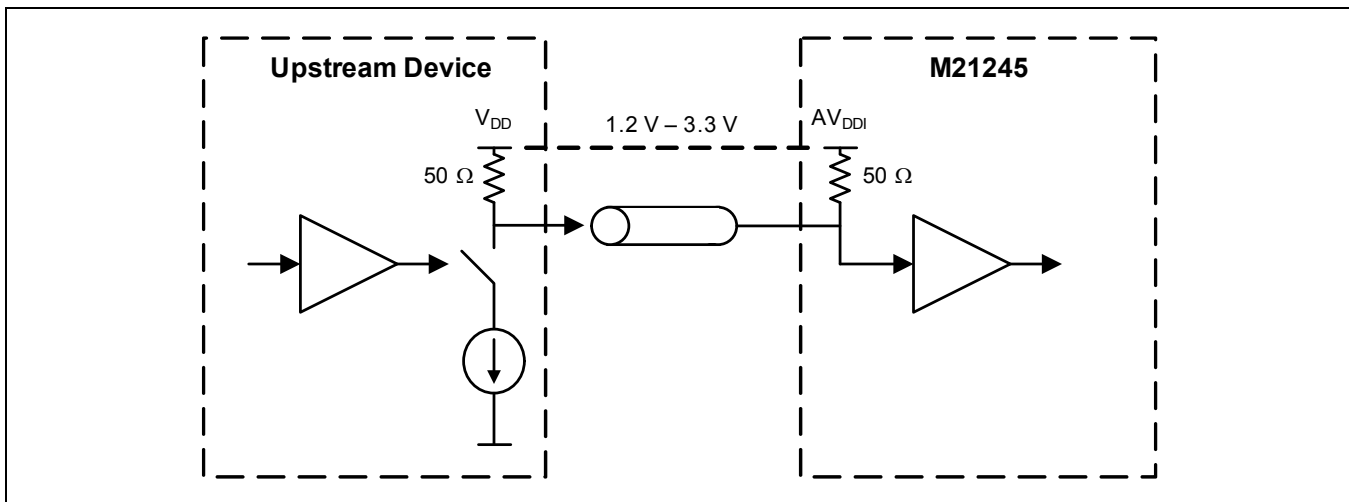
## 4.2 High-Speed Differential Inputs

The M21245 features four differential inputs; compatible with PCML, LVDS and LVPECL signal levels are also accommodated. Serial data to be retimed is presented to these four inputs. Each input is terminated with a  $50\ \Omega$  termination to  $AV_{DDI}$ .  $AV_{DDI}$  can be supplied from any voltage ranging from 1.2 V to 3.3 V.

In order to improve signal integrity when used in large systems, each input also comes equipped with programmable input equalization (IE) for FR4 trace. There are four settings for input equalization: 0 dB (or no equalization), 2 dB, 4 dB, and 6 dB. In serial control mode, the input equalization level for each input may be set by programming the desired value to register **Input EQ Config** (addresses 00h–03h). Alternatively, in hardware mode, the input equalization for all of the inputs may be set globally through pin **IE\_CTRL (MF2)**. In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC-coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC-coupling will result in more system jitter margin. In order to accommodate DC-coupling with the upstream device, the  $AV_{DDI}$  power domain of the M21245 is electrically independent from all other power domains therefore allowing it to be tied to the  $V_{DD}$  of the upstream device. This is demonstrated in Figure 4-2 below.

**Figure 4-2. M21245  $AV_{DDI}$  Connected to the  $V_{DD}$  of the Upstream Device**



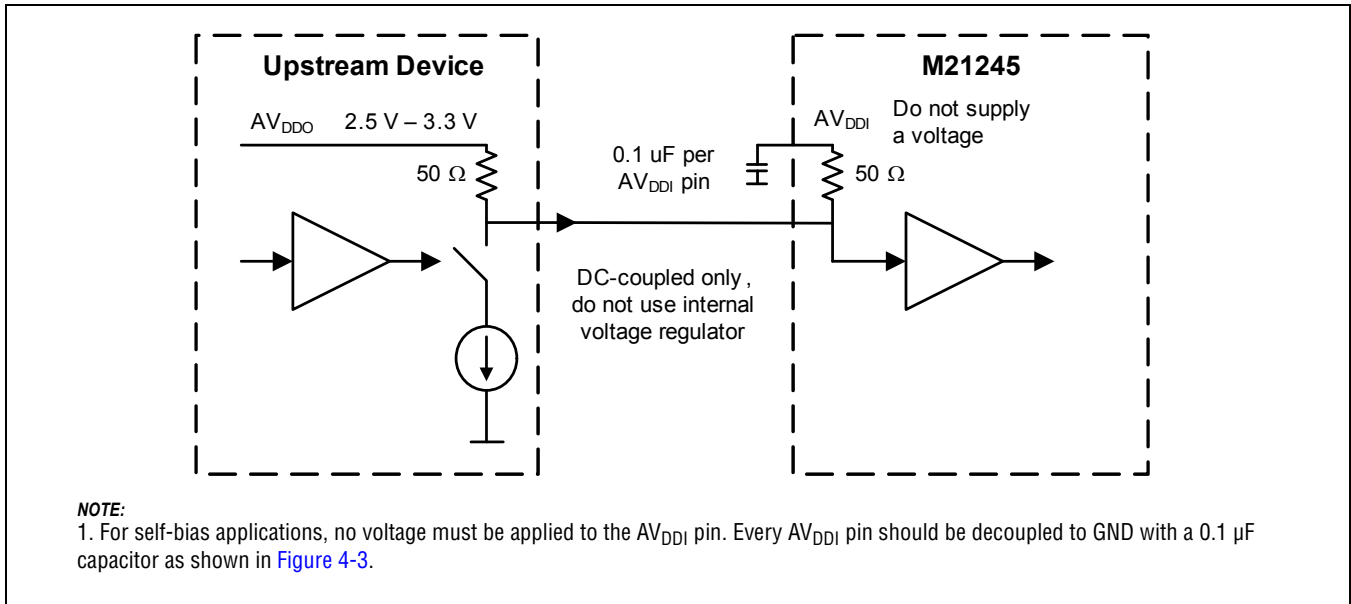
Alternatively and under certain conditions, the M21245 allows for the inputs to be self biased eliminating the need for an electrical connection between the supply voltages of the upstream device and M21245. This configuration offers the benefit of keeping the supply of the previous device and the power domain(s) of the M21245 completely isolated, while using DC-coupling. AC-coupling should not be used with the self bias interface. This self-biasing scheme is demonstrated in Figure 4-3 below.

When using the M21245 in self biased mode, specific conditions must be met:

1. The self biased inputs must be DC-coupled. No AC-coupling is supported in self biased mode.
2. The  $AV_{DDO}$  of the upstream device must be 2.5 V or greater.  $AV_{DDO}$  levels 1.2 V and 1.8 V are not supported in this mode.
3. The common mode of the upstream signals must be greater than 600 mV.

4. Internal voltage regulators are disabled.
5. All inputs are configured in self biased mode. Combination of self biased and non-self biased is not supported.

**Figure 4-3. Self Biasing the Input of M21245**



A Loss of Signal (LOS) detector monitors each input and issues an alarm when the input signal level dips below the detection threshold set in register **LOS Config** (address 06h). See Section 4.3 for more information on the LOS circuit.

In order to correct any duty cycle distortion (DCD) in the input signal, or any DC offset buildup in the internal signal path, a DC correction loop has been added. Programming register **GBL CTRL1.bit[1]** (address 0Dh) to a '1' will disable the DC correction loop for all inputs.

The M21245 includes a 4:1 multiplexer. This allows any one of the four input signals to be routed to the reclocker. By default, SDI0 is selected to be routed to SDO0. The selected input can be set using register **Input MUX CTRL** (address 07h).

By default, only the selected input is powered up, with all other inputs powered down. When an input is powered down, its associated LOS circuitry is disabled. If required, all the other inputs can also be powered up by setting register **GBL CTRL1.bit[3]** (address 0Dh). This will allow for a faster response if rapid input switching is required as there is no delay waiting for the circuitry to power-up and adjust to the input signal, but has the disadvantage of consuming more power.

With all inputs enabled, the power consumption increases by 100 mW.



## 4.3 LOS (Loss of Signal)

The M21245 has an integrated LOS circuit on each of its four high-speed inputs. This circuit monitors the input amplitude and if it falls below the detection threshold it asserts the LOS alarm bit by setting this to a logic high. These alarm bits are latched and will need to be reset with register **CLEAR ALARMS** (address 85h), by setting bit 0 to a high and back to a low. Hysteresis is built into the LOS circuit to avoid chattering. The LOS threshold can be set to a different level by using register **LOS Config.bits[7:5]** (address 06h), this changes the level on all four inputs.

By default, the LOS alarm mutes the signal from that particular input. Setting register **LOS Config.bit[3]** (address 06h) to a high will disable this feature.

## 4.4 High-Speed Output Description

There are two high-speed outputs available on the M21245. By default, only SDOA is powered up, setting register **SDOB CTRL.bit[2]** (address 0Ch) high will enable SDOB. The output signal will be a copy of SDOA. In hardware mode, SDOB is enabled with the SDOB/SCLK\_EN input pin in a floating (F) or high (H), see [Table 3-1](#).

A further function of this output is a serial clock source. By setting register **CLK EN.bit[0]** (address 06h) to high, the reclockers recovered clock is output to the SDOB/SCLK pins. In hardware mode this function is selected by setting SDOB/SCLK\_EN high, see [Table 3-1](#).

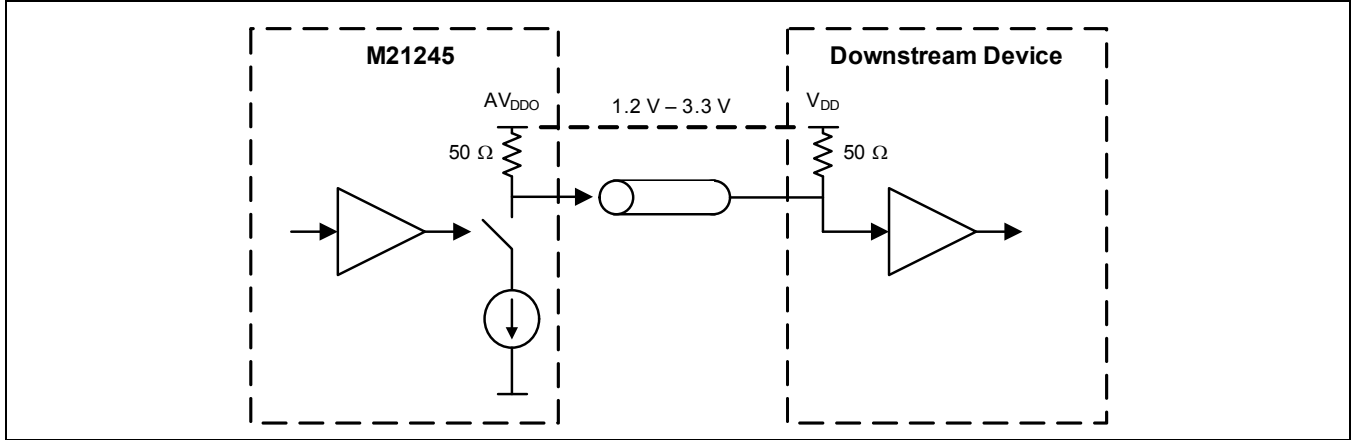
The M21245 features differential current mode logic (CML) drivers with integrated 50  $\Omega$  pull-ups to  $AV_{DDO}$  for the output of each reclocker channel.  $AV_{DDO}$  may be supplied from any voltage ranging from 1.2 V to 3.3 V.

The differential, peak-to-peak, output swing for each CML driver is programmable and may be set to 600 mV<sub>PPD</sub>, 800 mV<sub>PPD</sub>, or 1200 mV<sub>PPD</sub>. Please note that the 1200 mV<sub>PPD</sub> output swing setting is only available when  $AV_{DDO}$  is supplied from a voltage of 1.8 V or greater. The swing setting may be programmed by writing to register **SDOA CTRL.bits[3:2]** (address 09h) for SDOA, and register **Output CTRL.bits[3:2]** (address 0Bh) for SDOB.

In order to improve signal integrity when used in large systems, each output also comes equipped with programmable de-emphasis (DE) for FR4 trace. There are four settings for output de-emphasis: 0 dB (or no DE), 2 dB, 4 dB, and 6 dB. In serial control mode, the output de-emphasis level for each input may be set by programming the desired value to register **SDOA CTRL.bits[1:0]** for SDOA and register **SDOB CTRL DE.bits[5:4]** (address 0Ah) for SDOB. Alternatively, in hardware mode, the de-emphasis level for all of the outputs may be globally set through pin **DE\_CTRL** (MF3). In hardware mode only the three settings of 0 dB, 4 dB, and 6 dB are available.

In most SDI applications, it is important to avoid AC-coupled data interfaces between devices wherever possible. In addition to reducing the number of components, DC-coupling will result in more system jitter margin. In order to accommodate DC-coupling with the upstream device, the  $AV_{DDO}$  power domain of the M21245 is electrically independent from all other power domains therefore allowing it to be tied to the  $V_{DD}$  of the downstream device. This is demonstrated in [Figure 4-4](#) below.

**Figure 4-4. M21245 AV<sub>DDO</sub> Connected to the V<sub>DD</sub> of the Downstream Device**



If AC-coupling is desired or necessary, then the capacitor should be at least 10  $\mu$ F.

## 4.5 Logic Signals

To allow interfacing to logic levels other than the 1.2 V core voltage, or any of the analog input and output supplies, the digital interface signals are referenced to DV<sub>DDIO</sub> which is an isolated power domain. DV<sub>DDIO</sub> may be supplied from any voltage ranging from 1.2 V to 3.3 V. Many digital control pins have three states, high (H), low (L), or floating, (F). In order to assert the F or floating state, the pin must be left unconnected or undriven.

## 4.6 Control Modes

The M21245 may be configured in four separate control modes. The control mode is determined by the setting of pin. **MODE\_SEL** as shown in [Table 4-1](#) below.

**Table 4-1. Control Mode Setting**

MODE_SEL	Control Mode
MODE_SEL = F	Hardware control mode (HIC) This mode has limitations and is not recommended, see <a href="#">Section 4.6.1</a> .
MODE_SEL = H	Four-wire serial interface control mode (SIC4 or SPI)
MODE_SEL = L	Two-wire serial interface control mode (SIC2 or I <sup>2</sup> C)
	Memory interface configuration mode (MIC) When the reclocker is configured through an external EEPROM

The MIC mode is a subset of the two-wire Interface mode and is initiated by writing to special reserved address when the device is set in two-wire Interface mode.

### 4.6.1 HIC Mode

Configuring the M21245 in hardware mode avoids the complication of adding a microcontroller, but offers limited control options. When in hardware mode, the MF (Multi Function I/O) pins are configured as shown in [Table 4-2](#) below.

**Table 4-2. MF Pin Configuration in Hardware Mode**

MF	HIC Mode Pin Name	Function
MF2	IE_CTRL	Input trace equalization control for all SDI inputs H = 6 dB Input EQ F = 2 dB Input EQ L = 0 dB Input EQ
MF3	DE_CTRL	Output de-emphasis (DE) control for all SDO outputs H = 6 dB of output DE F = 4 dB of output DE L = 0 dB output DE
MF4	RC_BYPASS	Reclockers bypass control for all outputs L/H = Normal operation, reclocker not bypassed H = Reclocker bypassed
MF5	SDO_DIS	SDO disable control for all outputs H = SDO disabled output logic high L/F = SDO enabled

**NOTE:** In this mode, xALARM is not supported.

### 4.6.2 Four-wire Interface Mode (SIC4)

In this mode, a four-wire serial interface is used to program the device's internal registers, configuring the operation of the M21245. When in SIC4 mode, MF[0:3] pins comprise the four-wire bus as shown in [Table 4-3](#) below.

**Table 4-3. MF Pin Configuration in Four-wire Interface Mode**

MF	SIC4 Mode Pin Name	Function
MF0	SCLK	Serial clock input
MF1	SO	Serial data output
MF2	SI	Serial data input
MF3	xCS	Chip select (active low)

The interface shifts data in from the external controller on the rising edge of SCLK. The serial I/O operation is gated by xCS. Data is shifted in to M21245 from the Host (Master) to SI on the falling edge of SCLK, and shifted out through SO on the rising edge of SCLK. To write to a register, an 18-bit input needs to be shifted on SI, consisting

of the first bit (Start Bit, SB = 1), the second bit (Operation Bit, OP = 0 for write), the 8-bit address (MSB first) and the 8-bit data (MSB first).

**Figure 4-5. 4-wire Serial Digital Interface**

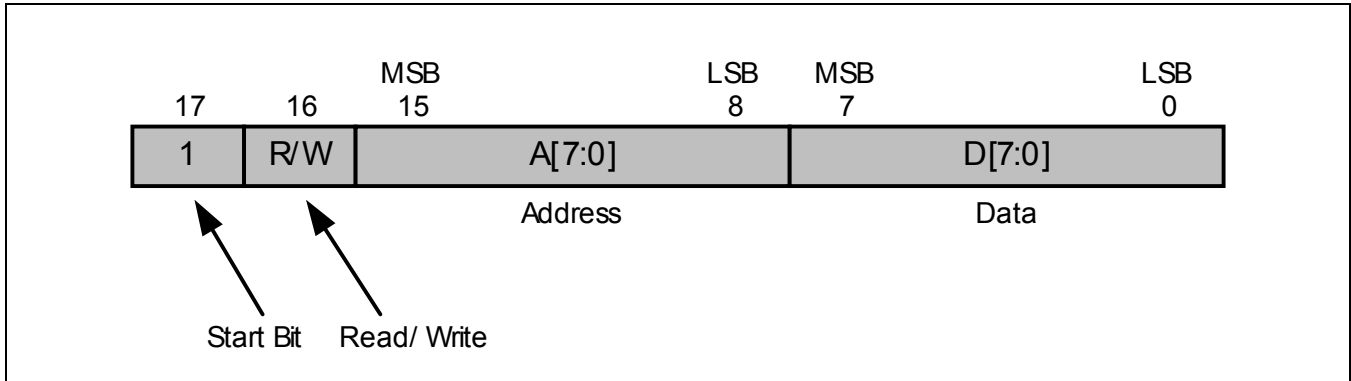
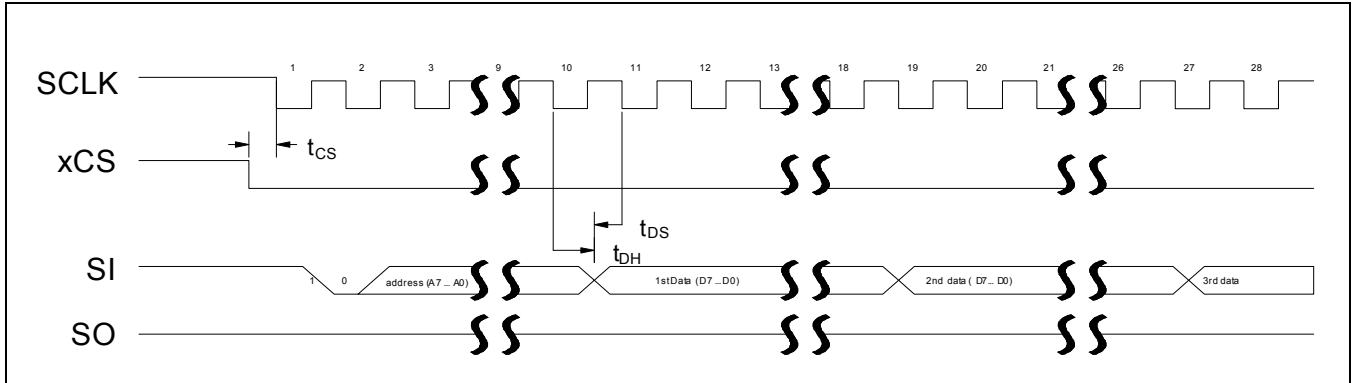


Figure 4-6 and Figure 4-7 illustrate the Serial Write Mode. To initiate a Write sequence, “xCS” goes low before the falling edge of “SCLK.” On each falling edge of the clock, the 18 bits consisting of the SB = 1, OP = 0, ADDR, and DATA, are latched into the input shift register through “SI.” The rising edge of “xCS” must occur before the falling edge of “SCLK” for the last bit. Upon receipt of the last bit, one additional cycle of “SCLK” is necessary before DATA transfers from the input shift register to the addressed register.

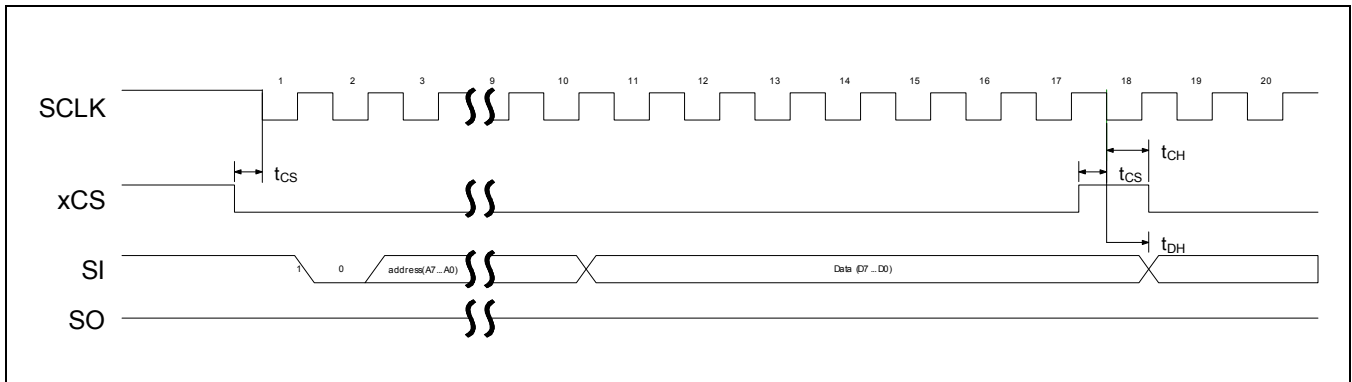
The 4-wire serial interface supports multiple consecutive writes. In this case, the address header is not needed and each additional 8 bits of data will be written into consecutive addresses. If consecutive read/write cycles are being performed, it is not necessary to insert an extra clock cycle between read/write cycles, however one extra clock cycle is needed after the last data bit of the last read/write cycle.

Figure 4-8 and Figure 4-9 illustrate the Serial Read mode to initiate a read sequence. “xCS” goes low before the falling edge of “SCLK.” On each falling edge of “SCLK”, the 10 bits consisting of SB = 1, OP = 1, and the 8-bit ADDR are written to the serial input shift register and copied to the serial output shift register. Data is then read back to the master, through pin SO on the next rising edge after the address LSB. SO is initially forced to 0 by the M21245, for one bit period, the 8 bits data are then shifted out. On a Write cycle, any bits that follow the expected number of bits are ignored, and only the first 16 bits following SB and OP are used. An invalid SB or OP renders the operation undefined. The falling edge of “xCS” always resets the serial operation for a new Read or Write cycle.

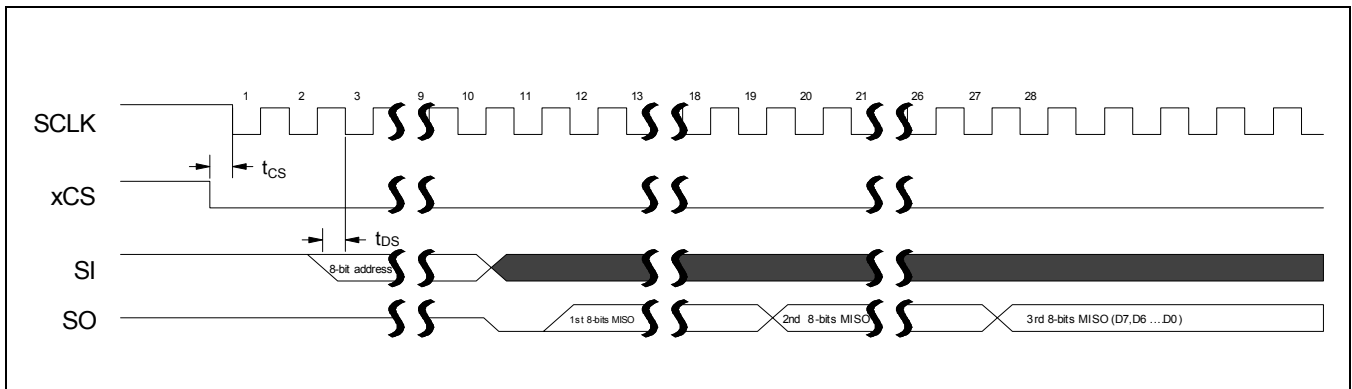
**Figure 4-6. 4-wire Serial Sequential WRITE Timing Diagram**



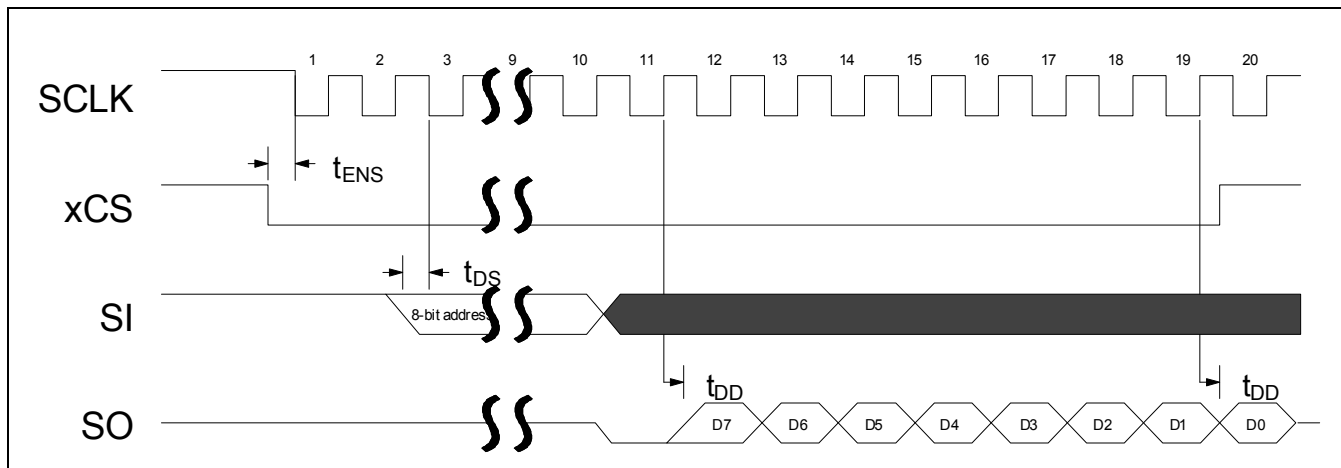
**Figure 4-7. 4-wire Random WRITE Timing Diagram**



**Figure 4-8. 4-wire Sequential READ Timing Diagram**



**Figure 4-9. 4-wire Random READ Timing Diagram**



**Table 4-4. Four-wire Interface Timing**

Timing Symbol	Description	Min	Max	Unit
Tds	Data set-up time	2.5	—	ns
Tdh	Data hold time	2.5	—	ns
Tcs	xCS set-up time	2.5	—	ns
Tch	xCS hold time	2.5	—	ns
Tfreq, write	Four-wire interface write clock frequency	—	100	MHz
Tfreq, read	Four-wire interface read clock frequency DV <sub>DDIO</sub> =1.2 V, 1.8 V Maximum load capacitance 10 pF	—	25	MHz
	Four-wire interface read clock frequency DV <sub>DDIO</sub> =2.5 V, 3.3 V Maximum load capacitance 30 pF	—	50	MHz
T <sub>DUTY</sub>	SCLK duty cycle	40	60	%
Tdd	Four-wire interface read data output delay DV <sub>DDIO</sub> =1.2 V, 1.8 V Maximum load capacitance 10 pF	2	17	ns
	Four-wire interface read data output delay DV <sub>DDIO</sub> =2.5 V, 3.3 V Maximum load capacitance 30 pF	2	9	ns

### 4.6.3 Two-wire Interface Mode (SIC2)

In this mode a two-wire serial interface is used to program the device's internal registers, configuring the operation of the M21245. When in SIC2 mode, MF[0:5] pins are configured as shown below.

**Table 4-5. MF Pin Configuration in Two-wire Interface Mode**

MF	SIC4 Mode Pin Name	Function
MF0	SCL	Clock input from master host
MF1	SDA	Serial data input/output
MF2	ADD0	Address bit 0
MF3	ADD1	Address bit 1
MF4	ADD2	Address bit 2
MF5	ADD3	Address bit 3

Each device has an individual address and is addressed using an address byte, which is latched upon Power-On-Reset (POR). In this mode, the M21245 is an I<sup>2</sup>C-compatible slave device that can operate at 100 kHz and 400 kHz for all allowed voltages seen at the DV<sub>DDIO</sub> pin.

The M21245 allows for forty different addresses to be programmed using the inputs ADD[3:0]; these inputs have three states, low (L), high (H) and floating (F). The slave addresses are from 21h to 48h.

**Table 4-6. M21245 2-Wire Interface Address Map**

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
32	20	010 0000b	L	L	L	L	EEPROM only, Address 50h
32	20	010 0000b	L	L	L	H	EEPROM only, Address 51h
32	20	010 0000b	L	L	H	L	EEPROM only, Address 52h
32	20	010 0000b	L	L	H	H	EEPROM only, Address 53h
33	21	010 0001b	L	H	L	L	Slave 1
34	22	010 0010b	L	H	L	H	Slave 2
35	23	010 0011b	L	H	L	F	Slave 3
36	24	010 0100 b	L	H	H	L	Slave 4
37	25	010 0101b	L	H	H	H	Slave 5
38	26	010 0110b	L	H	H	F	Slave 6
39	27	010 0111b	L	H	F	L	Slave 7
40	28	010 1000 b	L	H	F	H	Slave 8
41	29	010 1001b	L	H	F	F	Slave 9
42	2A	010 1010b	L	F	L	L	Slave 10

**Table 4-6. M21245 2-Wire Interface Address Map**

Dec Add	Hex Add	Bin Add	Pin Setting				Function
			ADD3	ADD2	ADD1	ADD0	
43	2B	010 1011b	L	F	L	H	Slave 11
44	2C	010 1100b	L	F	L	F	Slave 12
45	2D	010 1101b	L	F	H	L	Slave 13
46	2E	010 1110b	L	F	H	H	Slave 14
47	2F	010 1111b	L	F	H	F	Slave 15
48	30	011 0000 b	L	F	F	L	Slave 16
49	31	011 0001 b	L	F	F	H	Slave 17
50	32	011 0010 b	L	F	F	F	Slave 18
51	33	011 0011 b	F	L	L	L	Slave 19
52	34	011 0100 b	F	L	L	H	Slave 20
53	35	011 0101 b	F	L	L	F	Slave 21
54	36	011 0110 b	F	L	H	L	Slave 22
55	37	011 0111 b	F	L	H	H	Slave 23
56	38	011 1000 b	F	L	H	F	Slave 24
57	39	011 1001b	F	L	F	L	Slave 25
58	3A	011 1010b	F	L	F	H	Slave 26
59	3B	011 1011b	F	L	F	F	Slave 27
60	3C	011 1100b	F	H	L	L	Slave 28
61	3D	011 1101b	F	H	L	H	Slave 29
62	3E	011 1110b	F	H	L	F	Slave 30
63	3F	011 1111b	F	H	H	L	Slave 31
64	40	100 0000b	F	H	H	H	Slave 32
65	41	100 0001b	F	H	H	F	Slave 33
66	42	100 0010b	F	H	F	L	Slave 34
67	43	100 0011b	F	H	F	H	Slave 35
68	44	100 0100 b	F	H	F	F	Slave 36
69	45	100 0101b	F	F	L	L	Slave 37
70	46	100 0110b	F	F	L	H	Slave 38
71	47	100 0111b	F	F	L	F	Slave 39
72	48	100 1000 b	F	F	H	L	Slave 40

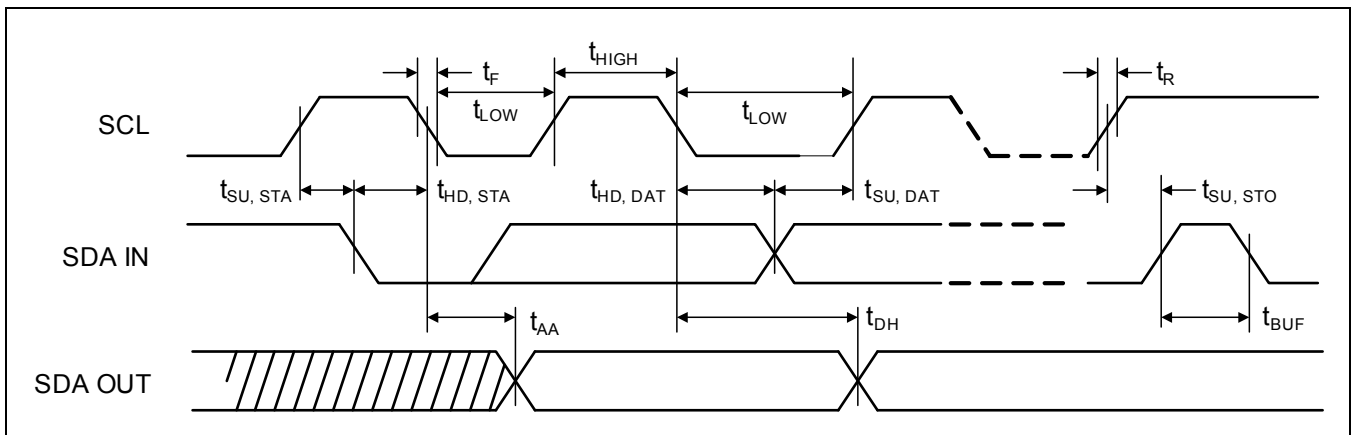


**Table 4-7. Supported AT24C01 EEPROM Addresses**

Dec Add	Hex Add	Bin Add	Fixed by EEPROM				Address Pin Setting		
			ADD6	ADD5	ADD4	ADD3	ADD2	ADD1	ADD0
80	50	010 0000b	H	L	H	L	L	L	L
81	51	010 0001b	H	L	H	L	L	L	H
82	52	010 0010b	H	L	H	L	L	H	L
83	53	010 0011b	H	L	H	L	L	H	H

Figure 4-10 illustrates typical waveforms and timing seen at SCL and SDA for a read and write operation.

**Figure 4-10. Two-wire Interface Timing Diagram**



**Table 4-8. Two-wire Interface Timing Specifications (Standard Mode or Fast Mode)**

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$f_{SCL}$	Clock frequency, SCL	—	—	400	kHz
$t_{LOW}$	Clock pulse width low	1.3	—	—	$\mu$ s
$t_{HIGH}$	Clock pulse width high	1	—	—	$\mu$ s
$t_{AA}$	Clock low to data out valid	0.05	—	0.9	$\mu$ s
$t_{HD, STA}$	Start hold time	200	—	—	ns
$t_{SU, STA}$	Start set-up time	200	—	—	ns
$t_{HD, DAT}$	Data in hold time	0	—	—	ns
$t_{SU, DAT}$	Data in set-up time	100	—	—	ns
$t_{SU, STO}$	Stop set-up time	200	—	—	ns
$t_{DH}$	Data out hold time	50	—	—	ns

**Notes:**

500 pF @ 100 kHz and 250 pF @ 400 kHz with 1k  $\Omega$  pull-up.

### 4.6.4 MIC Mode Operation

In this mode, the reclocker is initialized from an EEPROM. To use this mode, the EEPROM must be programmed with the register data required. The I<sup>2</sup>C address of the memory can be 50h, 51h, 52h or 53h; the reclocker loads its register contents from this address.

This mode is enabled when the I<sup>2</sup>C mode is set and address 20h has been hardwired on the address pins. When the reclocker locates the memory at one of the above addresses, it sets itself into I<sup>2</sup>C quasi-master mode. It will then load its registers from the EEPROM. Addresses 00h to 19h should be used when only one reclocker is used. Register **MicReg** (address 0Fh) contains the number of slave reclockers. If there are none this is set to 0.

Once the master has finished the task of downloading the registers, it will revert to slave mode at address 20h and can be accessed for debugging purposes.

Note that when using MIC power mode supply, ramp time is important. The EEPROM should be powered from the same supply as DV<sub>DDIO</sub> and the ramp up of the supply should be < 100 ms. If the ramp time is not met, the reclocker I<sup>2</sup>C will time-out before the EEPROM is ready to receive serial data.

The target EEPROM is the AT24C01 or equivalent.

If there is more than one reclocker to be programmed, a checksum is used to confirm that the data is correct. This works as follows:

1. The slave reclocker sums all registers from 00 to 1Ah, then truncates this to leave the 8 LSB bits. This is then compared with the value 2Eh. If it is not equal, then the registers are not loaded and it returns to the default value. It will then try up to 512 times before timing out. When the checksum is equal to 2Eh, the registers are loaded with the EEPROM settings.
2. To make the checksum = 2Eh, register **CHECKSUM** (address 1Ah) must be programmed with the 8 LSBs from the following calculation:

$$\text{Reg 1Ah} = 2\text{Eh} - (\text{sum of registers 0 to 19h})$$

## 4.7 Reclocker Operation

### 4.7.1 Clock Recovery

This block generates a serial clock signal at a frequency close to the data rate. The clock signal is generated by a phased locked loop (PLL) which uses the 27 MHz input clock as a reference.

The presence of the reference clock is monitored by the device. An alarm bit (NOREF) in register **RCLK ALARMS** (address 88h) is set to '1' when a suitable reference clock is not present. Once the PLL has locked to the reference clock, the REFLOL bit[4] in the same register will be set to '0'. A value of '1' in this bit indicates that the PLL has not locked to the input reference clock.

The frequency locked clock signal is supplied to the phase lock block. In this block, a bang-bang phase comparator is used to make fine adjustments to the phase and frequency of the clock, aligning it with the incoming serial data.

Once the clock signal is phase and frequency aligned with the serial data stream, it is used to re-time the data, producing a clean data signal that is provided at the output of the device. The phase lock block uses an integrated, programmable loop filter. The bandwidth of the phase lock block may be programmed using the BW[2:0] bits in register **RCLK BW CTRL** (address 16h). A wide bandwidth increases the jitter tolerance and reduces the lock time of the loop. However, a wide bandwidth also allows more jitter from the input serial data stream to be transferred to the output. Alternatively, a low bandwidth setting causes the loop to reject more of the incoming data stream's jitter, while increasing lock time, and reducing input jitter tolerance. The bandwidth setting can be optimized for each system.

Furthermore, since the phase lock block uses a non-linear, bang-bang loop, the bandwidth of the system is inversely proportional to the incoming data stream's jitter. This offers several advantages over linear PLLs. It achieves higher jitter attenuation with large input jitter, while it corrects for small variations quickly with low input jitter. With higher input jitter, the loop automatically reduces the bandwidth, causing more of the jitter to be rejected. Conversely, a data stream with lower jitter will cause the loop bandwidth to be widened. Note that bandwidth settings greater than 2x will increase output jitter.

When the recovered serial clock output is enabled, the clock alignment to the SDOA data output will be typically 60 ps, where the falling edge of the clock lags the transition edge of the SDOA signal.

### 4.7.2 Automatic Rate Detection

The reclocker features an Automatic Rate Detector (ARD) circuit that monitors the input signal rate and automatically sets the reclocker to the correct video rate. The data rate determined by the ARD block may be read from register **RCLK RATE DETECT.bits[1:0]** (address 89h) as shown in [Table 4-9](#).

**Table 4-9. Reclocker Rate Detection**

Address 89h Bits[1:0]	Function
00b	Reclocker unlocked
01b	SD rate detected
10b	HD rate detected
11b	3G rate detected

As an alternative to the ARD, the user may manually set the reclocker to the desired data rate by programming register **RCLK CTRL 0**.bits[3:2] (address 12h) to the desired values as shown in [Table 4-10](#).

**Table 4-10. Reclocker Data Rate Selection**

Address 12h Bits[3:2]	Function
00b	ARD enabled
01b	Manual SD rate programmed
10b	Manual HD rate programmed
11b	Manual 3G rate programmed

Please note that when configured in manual ARD mode, the reclocker is guaranteed to lock to the program data rate. However, it may also lock to the harmonics of that program data rate as well as. For example, if the reclocker is programmed to lock to HD data, it will also try to lock to 3G data as 2.97 Gbps is exactly twice 1.485 Gbps.

When in auto-bypass mode, if the ARD cannot determine the rate of the input data stream, it will switch the reclocker into bypass mode. This allows a data rate other than those specified to be passed through the reclocker. The auto-bypass mode may be disabled through register **RCLK CTRL 1** (address 14h).

### 4.7.3 Lock Detection

Several circuits monitor each reclocker for Loss of Lock. One in particular compares the recovered serial clock to one derived from the reference clock. If the clock frequency is within  $\pm 2000$  ppm of the serial data frequency, the Loss of Lock (LOL) alarm will be set to '0'. If the clock is outside of this window, then the LOL alarm will be asserted to '1'.

The LOL bit can be read from register **RCLK ALARMS**.bit[0] (address 88h).

### 4.7.4 Reference Clock

The M21245 can operate from a crystal or an external reference clock, but better jitter results are obtained with a crystal. If using an external reference clock then this should be a 27 MHz clock with a frequency accuracy of  $\pm 100$  ppm or better. Reference clock jitter is important and care must be taken to supply a low jitter reference clock to the reclocker of 1 ps RMS or less. The reference clock may either be from an external CMOS clock oscillator or an external parallel resonance crystal. If a low jitter 27 MHz signal is already available on the board then it may be used. Due to the higher jitter, a genlocked 27 MHz clock is likely not suitable for this device. When supplying an external clock signal, it is recommended to use AC-coupling, through a 0.1  $\mu$ F capacitor. Refer to [Table 1-6](#) for recommended input levels.

### 4.8 SD/xHD Output

When the reclocker is locked to the input data, the SD/xHD output indicates whether an SD or HD rate is detected. When a 3G rate is being received, the output will indicate HD. This output is designed to be connected to the slew rate control on a downstream cable driver.

The SD/xHD pin has two available modes as shown in [Table 4-11](#). These are controlled by the SDALG bit, register **SD xHD CTRL**.bit[5] (address 18h). By default this is a 0 and only goes high when the reclocker is locked to a 270 Mbps input signal. This mode sets the fast edge on the cable driver and allows for any signal in the reclockers data range to be bypassed. If the slow edge is set, any signal above 540 Mbps would be distorted by the slow edge on the cable driver.

When SDALG is high it also sets the SD/xHD pin high when the reclocker is unlocked. This is used when the user requires other SD rates such as 143 Mbps and 360 Mbps to be output from the cable driver with the slow SD edge when the reclocker is not locked.

**Table 4-11. SD/xHD Output Algorithm**

Rate (Gbps)	SD/xHD Pin	
	SDALG Bit = 0	SDALG Bit = 1
0.270	H	H
1.485/1.4835	L	L
2.97/2.967	L	L
unlocked	L	H

### 4.9 xALARM

The xALARM output pin is provided so the user can monitor alarm activity on the reclocker. The output is open drain as shown in [Figure 3-10](#). [Table 4-12](#) shows the reclocker alarms and their function. The assertion of any of the alarms in [Table 4-12](#) will trigger xALARM.

**NOTE:**

Please note that xAlarm is not supported in hardware control mode (HIC).

**Table 4-12. Reclocker Alarm Function**

Alarm	Function
LOS	Asserted when input signal goes below LOS threshold as set in register 06h
LOL	Asserted when reclocker cannot lock to the incoming data
NOREF	Asserted when no input reference is present at the reference clock inputs
REFLOL	Asserted when frequency lock block cannot lock to the reference clock input

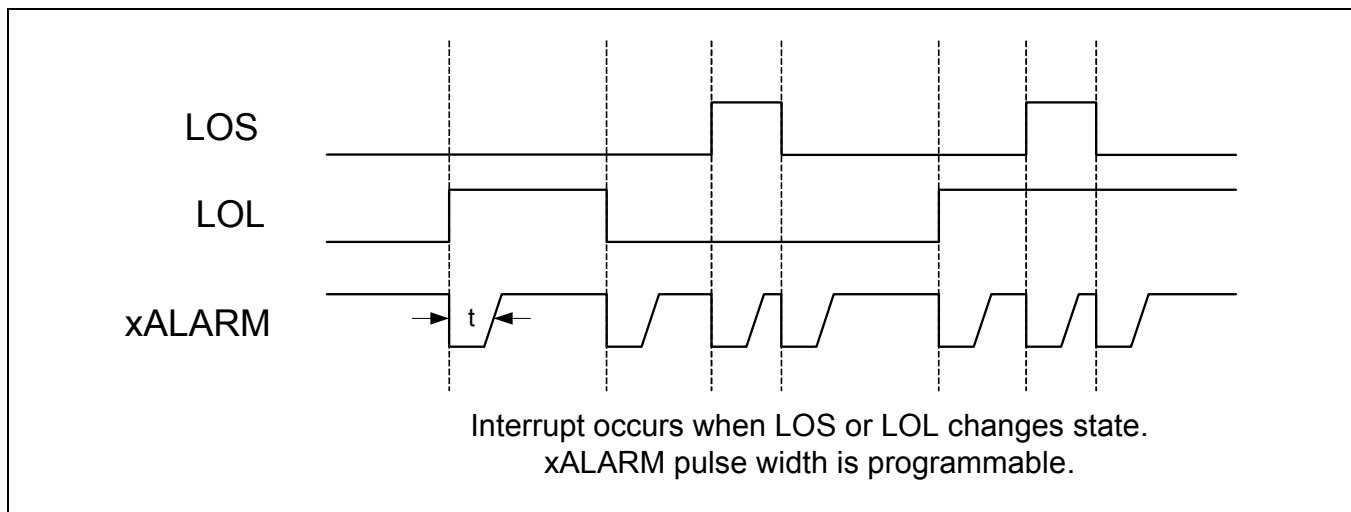
The xAlarm pin may be used when the M21245 is controlled using standard four-wire or two-wire serial interfaces (SIC4 and SIC2). The xAlarm pin operates in an interrupt mode. It goes low on the assertion of any of the internal

alarm flags and stays low for a fixed period of time before returning to high (see Figure 4-11). This period is set by the register **Interrupt CTRL** (address 0Eh). By default this is 0 and that corresponds to 20 ns, the maximum period is 2.560  $\mu$ s when INT[3:0] is set to Fh.

To achieve the correct pulse widths in “interrupt mode”, a 10 k $\Omega$  pull up to DV<sub>DDIO</sub> should be added to the xALARM output.

The xAlarm pin is designed to be connected to a microprocessor's interrupt pin. After the interrupt occurs, the microprocessor can read the reclocker's alarm registers to determine which alarm was asserted.

**Figure 4-11. xALARM-Output Interrupt Mode**



### 4.9.1 Reading Register Alarm Bits

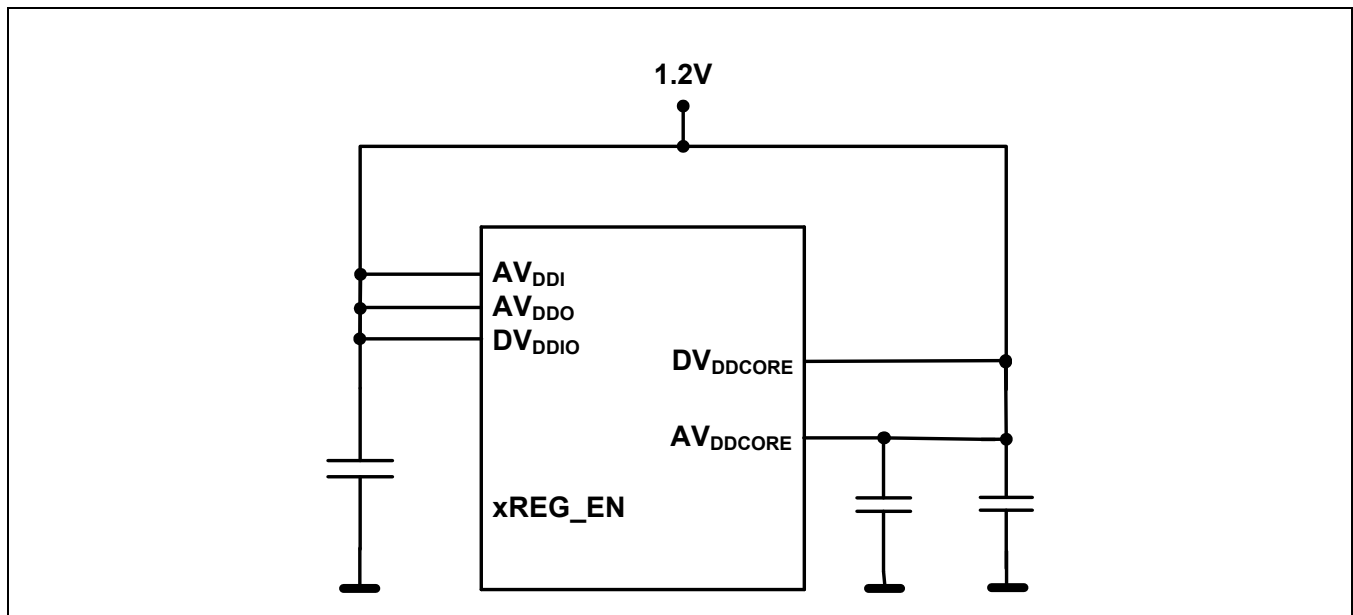
The LOS and LOL alarm bits are latched when asserted, after reading they should be cleared using register.CLEAR ALARMS.bit[0] (address 85h). This bit needs to be set to '1' to reset the alarms, it should then be reset to a '0' to re-enable normal alarm operation.

## 4.10 Internal Regulator

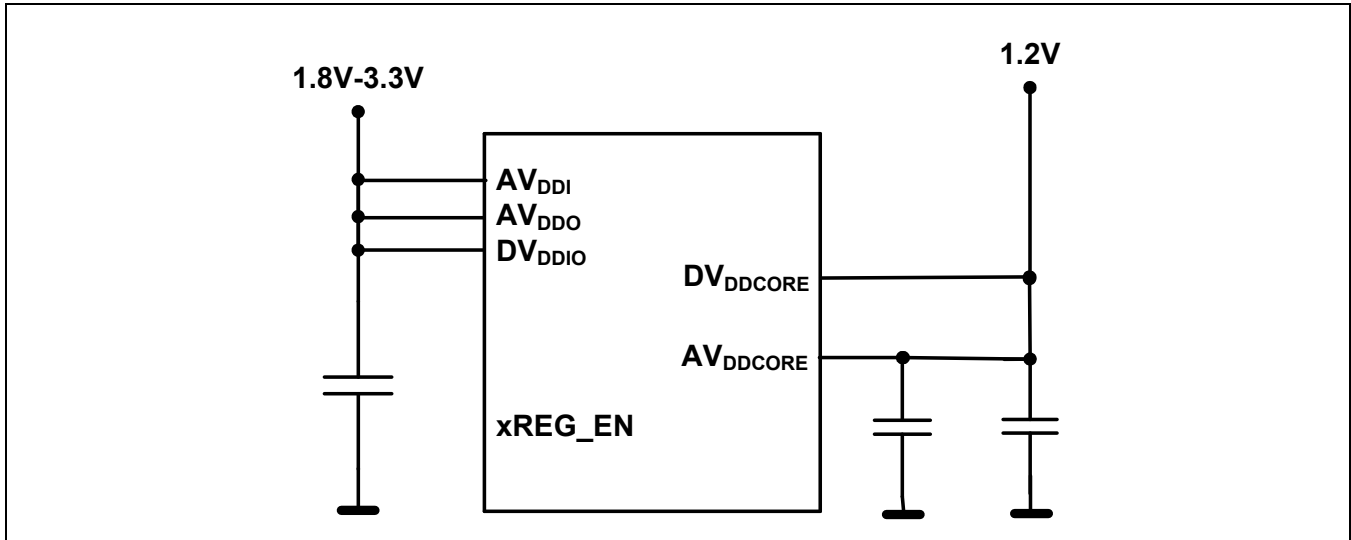
Both digital and analog cores of the M21245 are designed to run from a 1.2 V supply. If a 1.2 V supply is not available locally, then the internal regulator can be used to create this domain from  $AV_{DDI}/AV_{DDO}$  and  $DV_{DDIO}$ . Setting the  $xREG\_EN$  pin LOW, enables the internal regulator. This regulator generates a 1.2 V domain at pins  $AV_{DD}$  and  $DV_{DD}$ . See Figures [Figure 4-12](#) to [Figure 4-14](#) for the three different supply configurations. Note that the decoupling capacitors should be at least 100 nF.

When the internal regulator is used, all the current for the device is taken through the  $AV_{DDI}/AV_{DDO}$  and  $DV_{DDIO}$  pins. Because of this, care should be taken to ensure that the supplies to these pins are sufficient to handle the total current.

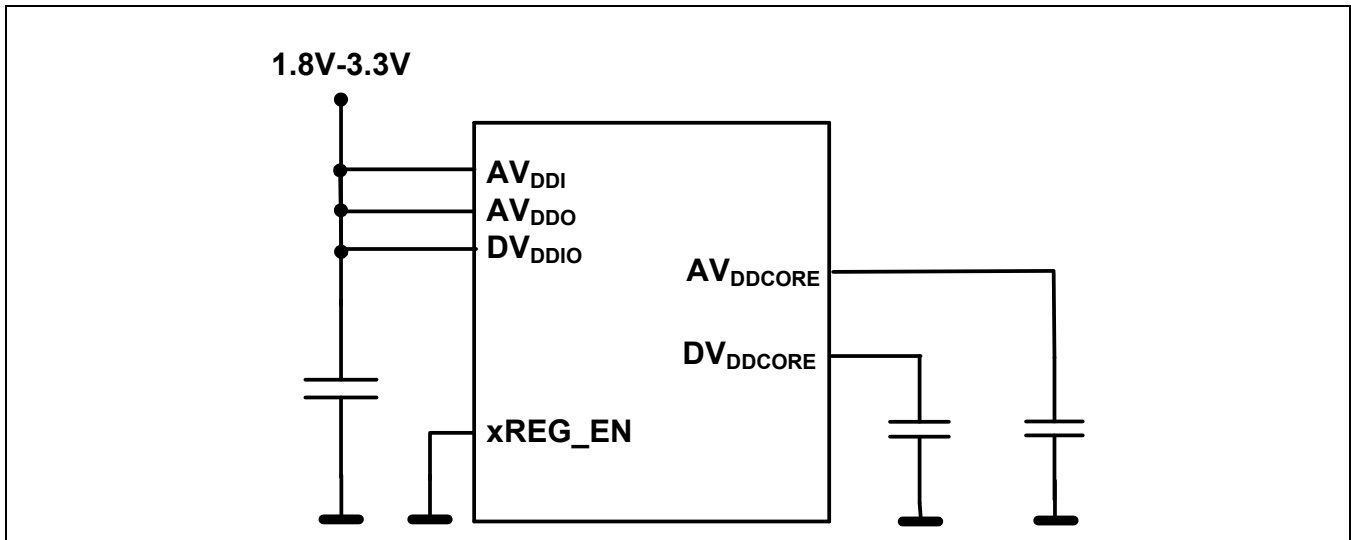
**Figure 4-12. All Power Pins Connected to 1.2 V, Internal Regulators Not Used**



**Figure 4-13.**  $AV_{DDI}$ ,  $AV_{DDO}$ , and  $DV_{DDIO}$  Connected to a Supply at 1.8 V or 3.3 V, 1.2 V is Supplied to  $AV_{DD}$  and  $DV_{DD}$ , Internal Regulator not Used



**Figure 4-14.**  $AV_{DDI}$ ,  $AV_{DDO}$ , and  $DV_{DDIO}$  Connected to a Supply at 1.8 V or 3.3 V. Internal Regulator Generates On-Chip 1.2 V



**Note:** In order to simplify the diagrams,  $AV_{DDI}$ ,  $AV_{DDO}$ , and  $DV_{DDIO}$  are shown to be shorted together. In practice, they may all be separated and connected to different supply domains if desired.

$AV_{DDO}$  is sensitive to noise and therefore should be filtered through a ferrite bead, with a 10 nF ceramic capacitor adjacent to each  $AV_{DDO}$  pin. Since this core can take a current in the order of 500 mA, the ferrite bead should be very low resistance to ensure the drop across it is minimal.



## 5.0 Control Registers Map and Descriptions

**Table 5-1. M21245 Register Map**

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
<b>Input/Output Configuration</b>											
00h	Input EQ Config 0	RSVD	RSVD	IE0[1]	IE0[0]	RSVD	RSVD	RSVD	RSVD	00h	R/W
01h	Input EQ Config 1	RSVD	RSVD	RSVD	RSVD	IE1[1]	IE1[0]	RSVD	RSVD	00h	R/W
02h	Input EQ Config 2	RSVD	RSVD	RSVD	RSVD	IE2[1]	IE2[0]	RSVD	RSVD	00h	R/W
03h	Input EQ Config 3	RSVD	RSVD	RSVD	RSVD	IE3[1]	IE3[0]	RSVD	RSVD	00h	R/W
04h	Input Polarity Flip 0	RSVD	RSVD	POL1	RSVD	RSVD	POL0	RSVD	RSVD	00h	R/W
05h	Input Polarity Flip 1	RSVD	RSVD	POL3	RSVD	RSVD	RSVD	POL2	RSVD	00h	R/W
06h	LOS Config/CLK EN	LVL[2]	LVL[1]	LVL[0]	F_LOS	NVRSQ	SQPOL	RSVD	SCLK_EN	20h	R/W
07h	Input MUX CTRL	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IN[1]	IN[0]	40h	R/W
08h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	C8h	R/W
09h	SDOA CTRL	RSVD	RSVD	RSVD	RSVD	LVL_A[1]	LVL_A[0]	DE_A[1]	DE_A[0]	88h	R/W
0Ah	SDOB CTRL DE	RSVD	RSVD	DE_B[1]	DE_B[0]	RSVD	RSVD	RSVD	RSVD	00h	R/W
0Bh	Output CTRL	RSVD	RSVD	RSVD	SDOA_MUTE	SCLK_LVL[1]	SCLK_LVL[0]	RSVD	RSVD	08h	R/W
0Ch	SDOB CTRL	RSVD	RSVD	RSVD	RSVD	RSVD	SDOB_EN	RSVD	RSVD	02h	R/W
0Dh	GBL CTRL1	RSVD	RSVD	RSVD	RSVD	FORCESDION	RSVD	OFFLOOP	PDALL	00h	R/W
0Eh	Interrupt CTRL	RSVD	RSVD	RSVD	RSVD	INT[3]	INT[2]	INT[1]	INT[0]	00h	R/W
0Fh	MicReg	RSVD	RSVD	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	MICDEV	00h	R/W
<b>Reclocker Configuration</b>											
10h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	30h	R/W
11h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
12h	RCLK CTRL 0	RSVD	RSVD	RSVD	RSVD	RATE[1]	RATE[0]	BYPASS	PDOWN	00h	R/W
13h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
14h	RCLK CTRL 1	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	BYPDIS	00h	R/W
15h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
16h	RCLK BW CTRL	RSVD	BW[2]	BW[1]	BW[0]	RSVD	RSVD	RSVD	RSVD	20h	R/W
17h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	C0h	R/W
18h	SD xHD CTRL	RSVD	RSVD	SDALG	RSVD	RSVD	RSVD	RSVD	RSVD	C8h	R/W

**Table 5-1. M21245 Register Map**

Addr	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
19h	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	03h	R/W
<b>Checksum for Memory Interface Configuration</b>											
1Ah	CHECKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	CHKSUM	55h	R/W
<b>Status/Monitoring Registers</b>											
80h	MASTER RESET	RST	RST	RST	RST	RST	RST	RST	RST	00h	R/W
81h	CHIP ID	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0Bh	R
82h	CHIP REV	REV[7]	REV [6]	REV [5]	REV [4]	REV [3]	REV [2]	REV [1]	REV [0]	04h	R
83h	LOS STATUS 0	RSVD	RSVD	LOS1	RSVD	RSVD	LOS0	RSVD	RSVD	00h	R
84h	LOS STATUS 1	RSVD	RSVD	LOS3	RSVD	RSVD	RSVD	LOS2	RSVD	00h	R
85h	CLEAR ALARMS	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SOFRST	CLRALARMS	00h	R/W
87h	CHECKSUM RESULT	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	CHKRES	00h	R/W
88h	RCLK ALARMS	RSVD	RSVD	NOREF	REFLOL	RSVD	RSVD	RSVD	LOL	00h	R
89h	RCLK RATE DETECT	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RATE[1]	RATE[0]	00h	R
96h	LOL CONFIG	RSVD	MASK[0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	00h	R/W
<b>NOTE:</b>											
1. RSVD are reserved bits that should never be changed from the default level.											

## 5.1 Register Descriptions

### 5.1.1 Input/Output Configuration

**Register Address:** 00h

**Default:** 00h

**Register Name:** Input EQ Config 0

**Description:** Select input equalization level, input 0

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R/W
5:4	IE0	00b: SDI0, Input equalization disabled 01b: SDI0, Small input equalization level 10b: SDI0, Medium input equalization level 11b: SDI0, Large input equalization level	00b	R/W
3:0	RSVD	Reserved (set to default)	0000b	R/W

**Register Address:** 01h

**Default:** 00h

**Register Name:** Input EQ Config 1

**Description:** Select input equalization level, input 1

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	0000b	R/W
3:2	IE1	00b: SDI1, Input equalization disabled 01b: SDI1, Small input equalization level 10b: SDI1, Medium input equalization level 11b: SDI1, Large input equalization level	00b	R/W
1:0	RSVD	Reserved (set to default)	00b	R/W

**Register Address:** 02h

**Default:** 00h

**Register Name:** Input EQ Config 2

**Description:** Select input equalization level, input 2

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	0000b	R/W
3:2	IE2	00b: SDI2, input equalization disabled 01b: SDI2, Small input equalization level 10b: SDI2, Medium input equalization level 11b: SDI2, Large input equalization level	00b	R/W
1:0	RSVD	Reserved (set to default)	00b	R/W

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**Register Address:** 03h

**Default:** 00h

**Register Name:** Input EQ Config 3

**Description:** Select input equalization level, input 3

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	0000b	R/W
3:2	IE3	00b: SDI3, input equalization disabled 01b: SDI3, Small input equalization level 10b: SDI3, Medium input equalization level 11b: SDI3, Large input equalization level	00b	R/W
1:0	RSVD	Reserved (set to default)	00b	R/W

**Register Address:** 04h

**Default:** 00h

**Register Name:** Input Polarity Flip 0

**Description:** Setting to a '1' inverts associated input, inputs 0 to 1

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R/W
5	POL1	0b: SDI1, Input normal 1b: SDI1, Input inverted	0b	R/W
4:3	RSVD	Reserved (set to default)	00b	R/W
2	POL0	0b: SDI0, Input normal 1b: SDI0, Input inverted	0b	R/W
1:0	RSVD	Reserved (set to default)	00b	R/W

**Register Address:** 05h

**Default:** 00h

**Register Name:** Input Polarity Flip 1

**Description:** Setting to a '1' inverts associated input, inputs 2 to 3

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R/W
5	POL3	0b: SDI3, Input normal 1b: SDI3, Input inverted	0b	R/W
4:2	RSVD	Reserved (set to default)	000b	R/W
1	POL2	0b: SDI2, Input normal 1b: SDI2, Input inverted	0b	R/W
0	RSVD	Reserved (set to default)	0b	R/W

**Register Address:** 06h

**Default:** 20h

**Register Name:** LOS Config/CLK EN

**Description:** Sets configuration for Loss of Signal alarm/Enables serial clock output buffer

Bit(s)	Name	Description	Default	Type
7:5	LVL	000b: 70 mV <sub>PPD</sub> assert, 80 mV <sub>PPD</sub> de-assert 001b: 80 mV <sub>PPD</sub> assert, 90 mV <sub>PPD</sub> de-assert [default] 010b: 90 mV <sub>PPD</sub> assert, 100 mV <sub>PPD</sub> de-assert 011b: 100 mV <sub>PPD</sub> assert, 110 mV <sub>PPD</sub> de-assert 100b: 110 mV <sub>PPD</sub> assert, 120 mV <sub>PPD</sub> de-assert 101b: 120 mV <sub>PPD</sub> assert, 130 mV <sub>PPD</sub> de-assert 110b: 130 mV <sub>PPD</sub> assert, 140 mV <sub>PPD</sub> de-assert 111b: LOS power down (globally applied for all input channels)	001b	R/W
4	F_LOS	0b: Normal LOS operation 1b: Force LOS to asserted	0b	R/W
3	NVRSQ	0b: Squelch input upon LOS assertion 1b: Never squelch input upon LOS assertion	0b	R/W
2	SQPOL	0b: Squelch to logic high state 1b: Squelch to logic low state	0b	R/W
1	RSVD	Reserved (set to default)	0b	R/W
0	SCLK_EN	0b: Serial clock output is disabled 1b: Serial clock output is enabled (output level controlled by reg0Bh[3:2])	0b	R/W

**Register Address:** 07h

**Default:** 40h

**Register Name:** Input Mux Control

**Description:** Selects the input that is selected for the serial data output

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved (set to default)	010000b	R/W
1:0	IN	00b: select input 0 to SDO 01b: select input 1 to SDO 10b: select input 2 to SDO 11b: select input 3 to SDO	00b	R/W

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**Register Address:** 09h

**Default:** 88h

**Register Name:** SDOA CTRL

**Description:** Sets output level and De-emphasis for SDO0

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	1000b	R/W
3:2	LVL_A	00b: SDO powered down 01b: SDO output swing = 600 mV p-p 10b: SDO output swing = 800 mV p-p 11b: SDO output swing = 1200 mV p-p	10b	R/W
1:0	DE_A	00b: SDO De-emphasis off 01b: SDO De-emphasis = small 10b: SDO De-emphasis = medium 11b: SDO De-emphasis = large	00b	R/W

**Register Address:** 0Ah

**Default:** 00h

**Register Name:** Data Output De-Emphasis Control

**Description:** Sets output level and de-emphasis for SDOB.

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	000b	R/W
5:4	DE_B	00b: SDOB de-emphasis off 01b: SDOB de-emphasis = small 10b: SDOB de-emphasis = medium 11b: SDOB de-emphasis = large	00b	R/W
3:0	RSVD	Reserved (set to default)	00b	R/W

**Register Address:** 0Bh

**Default:** 08h

**Register Name:** Output Control

**Description:** SDOA Mute and SDOB/SCLK swing control.

Bit(s)	Name	Description	Default	Type
7:5	RSVD	Reserved (set to default)	000b	R/W
4	SDOA_MUTE	0b: SDOA output in normal operation 1b: SDOA output muted	0b	R/W
3:2	SCLK_LVL	00b: SDOB/SCLK output powered down 01b: SDOB/SCLK output swing = 600 mV p-p 10b: SDOB/SCLK output swing = 800 mV p-p 11b: SDOB/SCLK output swing = 1200 mV p-p	10b	R/W
1:0	RSVD	Reserved (set to default)	00b	R/W

**Register Address:** 0Ch

**Default:** 02h

**Register Name:** SDOB Control

**Description:** Enable for second data output.

Bit(s)	Name	Description	Default	Type
7:3	RSVD	Reserved (set to default)	00000b	R/W
2	SDOB_EN	0b: SDOB output disabled 1b: SDOB output enabled	0b	R/W
1:0	RSVD	Reserved (set to default)	10b	R/W

**Register Address:** 0Dh

**Default:** 00h

**Register Name:** Global Control1

**Description:** Controls Global Configuration

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	0000b	R/W
3	FORCESDION	0b: Inputs that are not used are powered down 1b: All inputs are forced on	0b	R/W
2	RSVD	Reserved (set to default)	0b	R/W
1	OFFLOOP	0b: Input offset correction loop On (all inputs) 1b: Input offset correction loop Off (all inputs)	0b	R/W
0	PDALL	0b: Normal Operation 1b: Global Power Down	0b	R/W

**Register Address:** 0Eh

**Default:** 00h

**Register Name:** Interrupt Control

**Description:** Sets configuration for xALARM Output pin

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	00000b	R/W
3	INT[3]	0b: xALARM output is used in Interrupt mode 1b: Not supported	0b	R/W
2:0	INT[2:0]	000b: xALARM pulse width = 140 ns 001b: xALARM pulse width = 180 ns 010b: xALARM pulse width = 200 ns 011b: xALARM pulse width = 300 ns 100b: xALARM pulse width = 450 ns 101b: xALARM pulse width = 800 ns 110b: xALARM pulse width = 1.5 $\mu$ s 111b: xALARM pulse width = 2.8 $\mu$ s Measured with a 10 k $\Omega$ pull up resistor. Actual pulse width varies with the value of the pullup resistor.	000b	R/W

**Register Address:** 0Fh

**Default:** 00h

**Register Name:** Memory Interface Configuration Control

**Description:** Defines the number of slave RCLK devices, controlled by quasi master/EEPROM

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R/W
5:0	MICDEV	000000b: no slave RCLKs 000001b: 1 slave RCLK 000010b: 2 slave RCLKs	000000b	R/W



## 5.1.2 Reclocker Configuration

**Register Address:** 12h

**Default:** 00h

**Register Name:** Reclocker Control 0

**Description:** Controls Reclocker

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved (set to default)	0000b	R/W
3:2	RATE	00b: ARD enabled 01b: SD data rate selected for reclocker. 10b: HD data rate selected for reclocker. 11b: 3G data rate selected for reclocker.	00b	R/W
1	BYPASS	0b: Normal operation (reclocker not bypassed) 1b: Reclocker bypassed	0b	R/W
0	PDOWN	0b: Normal operation 1b: Reclocker powered down	0b	R/W

**Register Address:** 14h

**Default:** 00h

**Register Name:** Reclocker Control 1

**Description:** Controls Reclocker

Bit(s)	Name	Description	Default	Type
7:1	RSVD	Reserved (set to default)	0000b	R/W
0	BYPDIS	0b: Normal operation 1b: Reclocker auto-bypass feature disabled	0b	R/W

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**Register Address:** 16h**Default:** 20h**Register Name:** Reclocker BW Control**Description:** Controls bandwidth of Reclocker

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved (set to default)	0b	R/W
6:4	BW	000b: Reserved (do not use) 001b: 0.5 x Nominal LBW 010b: 1 x Nominal LBW 011b: 4 x Nominal LBW 100b: 2 x Nominal LBW 101b: 3 x Nominal LBW 110b: 1.5 x Nominal LBW 111b: 0.875 x Nominal LBW	010b	R/W
3:0	RSVD	Reserved (set to default)	0000b	R/W

**Register Address:** 18h**Default:** 00h**Register Name:** SD/xHD Algorithm Control**Description:** Controls SD/xHD output of Reclocker

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R/W
5	SDALG	0b: SD/xHD output conforms to case 1, <a href="#">Table 4-11</a> 1b SD/xHD output conforms to case 2, <a href="#">Table 4-11</a>	0b	R/W
4:0	RSVD	Reserved (set to default)	00000b	R/W

### 5.1.3 Checksum for Memory Interface Configuration

**Register Address:** 1Ah**Default:** 55h**Register Name:** Checksum**Description:** Checksum value to be added to sum of reg 00h to 19h contents

Bit(s)	Name	Description	Default	Type
7:0	CHKSUM	Checksum value	01010101b	R/W

### 5.1.4 Status/Monitoring

**Register Address:** 80h

**Default:** 00h

**Register Name:** Reset

**Description:** Does Master Reset on Device

Bit(s)	Name	Description	Default	Type
7:0	RST	00h: Normal Operation AAh: Master Reset	00000000b	R/W

**Register Address:** 81h

**Default:** 0Bh

**Register Name:** Chip ID

**Description:** Chip Identification Number

Bit(s)	Name	Description	Default	Type
7:0	ID	M21245	00001011b	R

**Register Address:** 82h

**Default:** 04h

**Register Name:** Chip Rev

**Description:** Chip Revision

Bit(s)	Name	Description	Default	Type
7:0	REV	Chip revision	00000100b	R

**Register Address:** 83h

**Default:** 00h

**Register Name:** LOS Status 0

**Description:** Inputs 0-1, Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R
5	LOS1	0b: SDI1, Input present 1b: SDI1, LOS Asserted	0b	R
4:3	RSVD	Reserved (set to default)	00b	R
2	LOS0	0b: SDI0, Input present 1b: SDI0, LOS Asserted	0b	R
1:0	RSVD	Reserved (set to default)	00b	R

**Register Address:** 84h

**Default:** 00h

**Register Name:** LOS Status 1

**Description:** Inputs 2-3, Set to a '1' when LOS asserted (single-event latched operation). Proper status is obtained after clearing all latched alarms by using Register 85h bit 0.

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R
5	LOS3	0b: SDI3, Input present 1b: SDI3, LOS Asserted	0b	R
4:2	RSVD	Reserved (set to default)	000b	R
1	LOS2	0b: SDI2, Input present 1b: SDI2, LOS Asserted	0b	R
0	RSVD	Reserved (set to default)	0b	R

**Register Address:** 85h

**Default:** 00h

**Register Name:** Alarm Clear

**Description:** Clears Latched Alarms. To properly clear all alarm bits, write "1" followed by a "0" to bit 0.

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved (set to default)	000000b	R/W
1	SOFTRST	0b: Normal operation 1b: Soft reset for CDR block (for master reset use reg 80h)	0b	R/W
0	CLRALARMS	0b: Normal operation 1b: Clears all alarm bits in registers 83h, 84h and 88h	0b	R/W

**Register Address:** 87h

**Default:** 00h

**Register Name:** Checksum result

**Description:** Shows the result of the checksum calculation

Bit(s)	Name	Description	Default	Type
7:0	CHKRES	Checksum result	00000000b	R/W

## 3G/HD/SD-SDI Multi-rate Reclocker

Rev V6

**Register Address:** 88h

**Default:** 00h

**Register Name:** Reclocker Status Register

**Description:** Reads status of the Reclocker

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved (set to default)	00b	R
5	NOREF	0b: Reference clock is present 1b: Reference clock is not present	0b	R
4	REFLOL	0b: PLL locked 1b: PLL unlocked	0b	R
3:1	RSVD	Reserved (set to default)	XXXb	R
0	LOL	0b: Reclocker, locked 1b: Reclocker, un-locked	0b	R

**Register Address:** 89h

**Default:** 00h

**Register Name:** Reclocker Rate Detect

**Description:** Reads data rate for Reclocker

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved (set to default)	XXXXXXb	R
1:0	RATE	00b: Reclocker: un-locked 01b: Reclocker: SD data rate detected 10b: Reclocker: HD data rate detected 11b: Reclocker: 3G data rate detected	00b	R

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