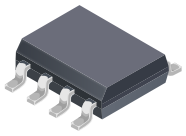
True Zero-Speed, High Accuracy, Ring Magnet Sensor IC

FEATURES AND BENEFITS

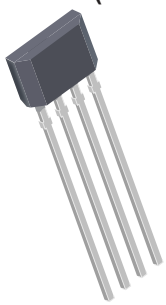
- Optimized robustness to magnetic offset variation
- Small signal lockout for immunity against vibration
- Tight duty cycle and timing accuracy over full operating temperature range
- True zero-speed operation
- Air gap independent switch points
- Large operating air gaps achieved through use of gain adjust and offset adjust circuitry
- Defined power-on state (POS)
- Wide operating voltage range
- Digital output representing target profile
- Single chip sensing IC for high reliability
- Small mechanical size
- Fast startup
- Undervoltage lockout (UVLO)

PACKAGES:

8-Pin SOIC (suffix L)



4-Pin SIP (suffix K)



Not to scale

DESCRIPTION

The A1667 is a true zero-speed ring magnet sensor integrated circuit (IC) consisting of an optimized Hall IC available in two package options that provides a user-friendly solution for digital ring magnet sensing applications.

The sensor incorporates a dual element Hall IC that switches in response to differential magnetic signals created by a ring magnet. The IC contains a sophisticated compensating circuit designed to eliminate the detrimental effects of magnet and system offsets. Digital processing of the analog signal provides zero-speed performance independent of air gap and also dynamic adaptation of device performance to the typical operating conditions found in automotive applications (reduced vibration sensitivity). High-resolution peak detecting DACs are used to set the adaptive switching thresholds of the device. Hysteresis in the thresholds reduces the negative effects of any anomalies in the magnetic signal associated with the targets used in many automotive applications.

The open-drain output is configured for three-wire applications. This sensor is ideal for obtaining speed and duty cycle

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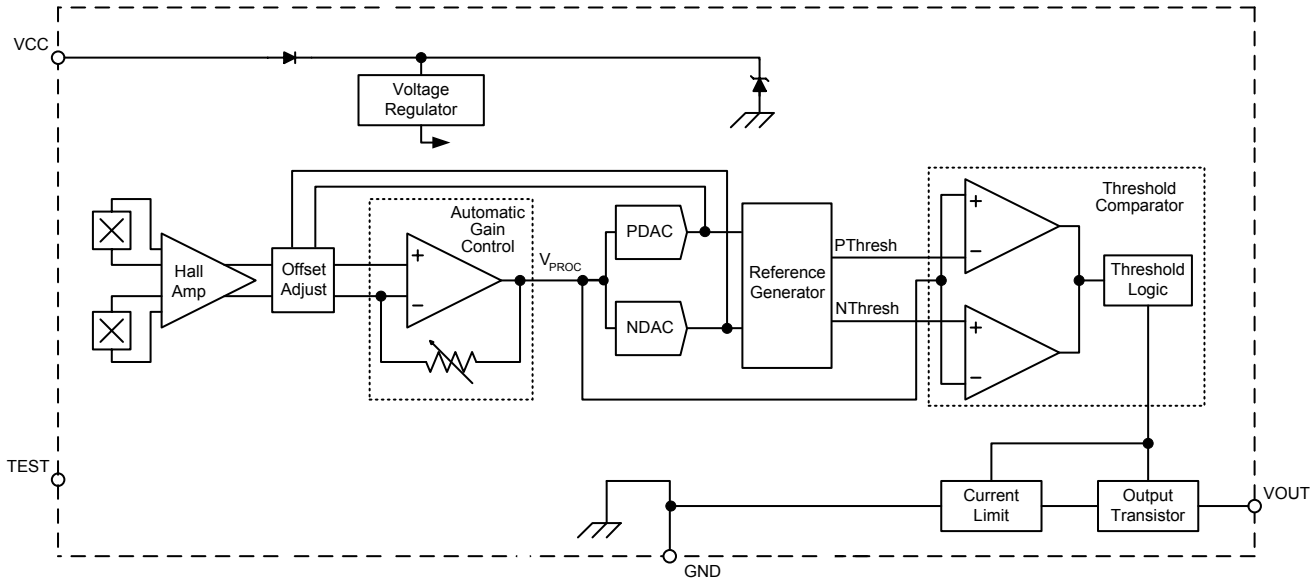
KEY APPLICATIONS

- Automotive – Transmissions Applications
- 2- and 3-Wheeler Speed Applications
- White Goods – Drum Speed Applications

Functional Block Diagram



DESCRIPTION (continued)

information using ring magnet based systems in applications such as automotive transmissions and industrial equipment.

The A1667 is available in a 4-pin SIP through-hole package (suffix K) and an 8-pin SOIC surface-mount package (suffix L). Both packages are lead (Pb) free with 100% matte-tin-plated leadframes.

SELECTION GUIDE

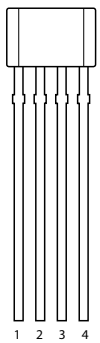
Part Number	Packaging	Packing*
A1667LK-T	4-pin SIP through hole	Bulk, 500 pieces per bag
A1667LLTR-T	8-pin SOIC surface mount	3000 pieces per 13-in. reel

*Contact Allegro™ for additional packing options

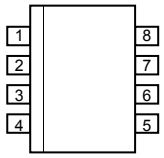
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	See Power Derating section	26.5	V
Reverse Supply Voltage	V_{RCC}		–18	V
Reverse Supply Current	I_{RCC}		–50	mA
Reverse Output Voltage	V_{ROUT}		–0.5	V
Output Sink Current	I_{OUT}		25	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

PINOUT DIAGRAMS AND TERMINAL LIST TABLE



Package K, 4-Pin SIP



Package L, 8-Pin SOIC

Terminal List

Number		Name	Function
K	L		
1	1	VCC	Supply voltage
2	2	VOUT	Device output
3	3	TEST	Test pin (float or tie to GND)
4	4	GND	Ground
–	5,6,7,8	NC	No connect*

* Pins 5, 6, 7, and 8 should be externally connected to Ground.

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OPERATING CHARACTERISTICS: Valid over operating voltage and temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	Operating, $T_J < T_J$(max)	4	–	24	V
Undervoltage Lockout (UVLO)	$V_{CC(UV)}$		2.7	3.5	3.95	V
Reverse Supply Current	I_{RCC}	V_{CC} = –18 V	–	–	–10	mA
Supply Zener Clamp Voltage	V_Z	I_{CC} = 15 mA, T_A = 25 °C	26.5	–	–	V
Supply Zener Current	I_Z	T_A = 25°C, $T_J < T_J$(max), continuous, V_Z = 26.5 V	–	–	15	mA
Supply Current	I_{CC}	Output off	4	7	12	mA
		Output on	4	7	12	mA
Test Pin Zener Clamp Voltage [2]	V_{TESTZ}		–	6	–	V
POWER-ON STATE CHARACTERISTICS						
Power-On State	POS	Connected as in figure 6	–	High	–	–
Power-On Time [3]	t_{PO}	f_{OP} < 200 Hz; $V_{CC} > V_{CC}$(min)	–	–	2	ms
OUTPUT STAGE						
Low Output Voltage	$V_{OUT(SAT)}$	I_{SINK} = 10 mA, Output = on	–	100	250	mV
Output Zener Clamp Voltage	V_{ZOUT}		26.5	–	–	V
Output Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 12 V, $T_J < T_J$(max)	25	45	70	mA
Output Leakage Current	$I_{OUT(OFF)}$	Output = off, V_{OUT} = 24 V	–	–	10	µA
Output Rise Time	t_r	R_L = 1 kΩ, C_L = 4.7 nF, V_{PULLUP} = 12 V, 10% to 90%, connected as in figure 6	–	10	–	µs
Output Fall Time	t_f	R_L = 1 kΩ, C_L = 4.7 nF, V_{PULLUP} = 12 V, 10% to 90%, connected as in figure 6	–	0.6	2	µs
DIGITAL-TO-ANALOG CONVERTER (DAC) CHARACTERISTICS						
Allowable User-Induced Differential Offset [4][5]	$B_{DIFFEXT}$	User induced differential offset	–150	–	150	G
SWITCHPOINT CHARACTERISTICS						
Operational Switching Frequency	f_{OP}		0	–	12	kHz
Bandwidth	f_{-3dB}	Cutoff frequency for low-pass filter	15	20	–	kHz
Operate Point	B_{OP}	% of peak-to-peak V_{PROC} referenced from PDAC to NDAC, $B_{SIG} > B_{SIG(MIN)}$, V_{OUT} high to low	65	70	75	%
Release Point	B_{RP}	% of peak-to-peak V_{PROC} referenced from PDAC to NDAC, $B_{SIG} > B_{SIG(MIN)}$, V_{OUT} low to high	25	30	35	%
Running Mode Lockout Enable (LOE)	$V_{LOE(RM)}$	$V_{PROC(PK-PK)} < V_{LOE(RM)}$ = output switching disabled	–	100	–	mV
Running Mode Lockout Release (LOR)	$V_{LOR(RM)}$	$V_{PROC(PK-PK)} < V_{LOR(RM)}$ = output switching enabled	–	220	–	mV

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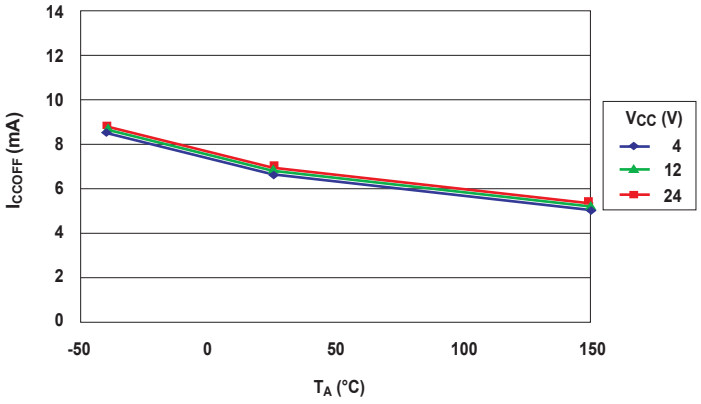
OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
CALIBRATION						
Initial Calibration [6]	CAL_I	Possible reduced edge detection accuracy, duty cycle not guaranteed	–	1	6	electrical edge
Update Method		Running mode operation, bounded for decreasing B_{SIG}, unlimited for increasing B_{SIG}	–	Continuous	–	–
OPERATING CHARACTERISTICS						
Operating Signal Range	B_{SIG}	Differential magnetic signal operation within specification	30	–	1400	G
Relative Repeatability [7]	$T_{\theta E}$	60 pole-pair target, using 100 G_{PK-PK} ideal sinusoidal signal, T_A = 150°C, and f_{OP} = 1000 Hz	–	0.12	–	degrees
Maximum Single Outward Sudden Air Gap Change [8]	ΔAG_{MAX}	Single instantaneous air gap peak-to-peak amplitude change, f_{OP} < 500 Hz, $V_{PROC(pk-pk)}$ > V_{LOE} after sudden AG change	–	40	–	$\%_{PK-PK}$

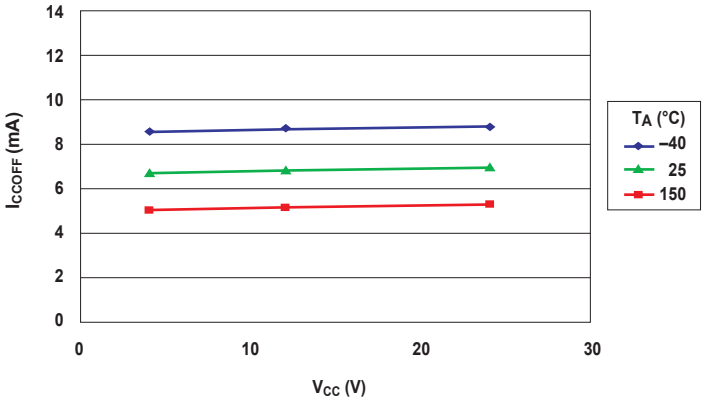
[1] Typical data is at V_{CC} = 12 V and T_A = 25°C, unless otherwise noted. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Sustained voltages beyond the clamp voltage may cause permanent damage to the IC.
[3] Power-On Time is the time required to complete the internal Automatic Offset Adjust; the DACs are then ready for peak acquisition.
[4] The device compensates for magnetic and installation offsets. Offsets greater than specification in gauss may cause inaccuracies in the output.
[5] 1 G (gauss) = 0.1 mT (millitesla).
[6] For power-on frequency, f_{OP} < 200 Hz. Higher power-on frequencies may result in more input magnetic cycles until full output edge accuracy is achieved, including the possibility of missed output edges.
[7] The repeatability specification is based on statistical evaluation of a sample population, evaluated at 1000 Hz.
[8] Single maximum allowable air gap change in outward direction (increase in air gap).

CHARACTERISTIC PERFORMANCE

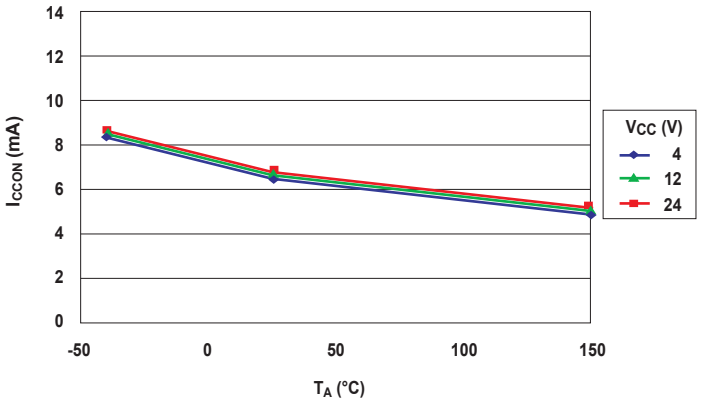
Supply Current (Off) versus Ambient Temperature



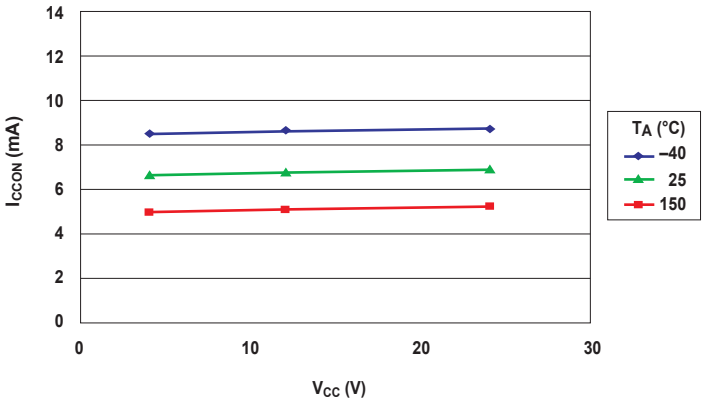
Supply Current (Off) versus Supply Voltage



Supply Current (On) versus Ambient Temperature

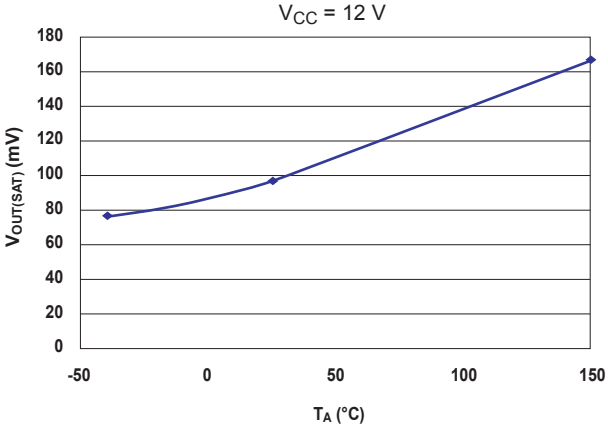


Supply Current (On) versus Supply Voltage

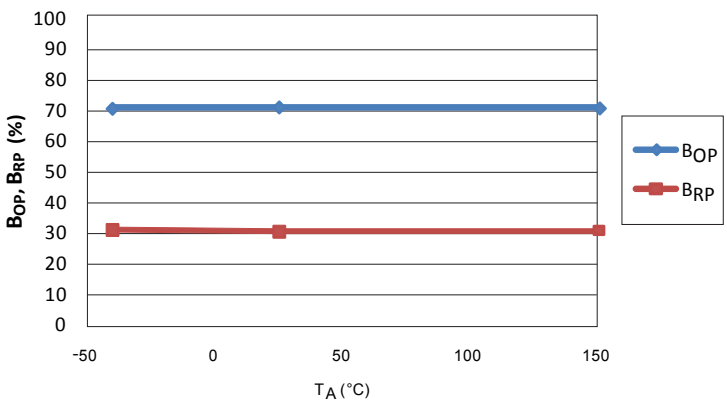


Output Saturation Voltage versus Ambient Temperature

V_{CC} = 12 V



Switchpoints versus Ambient Temperature

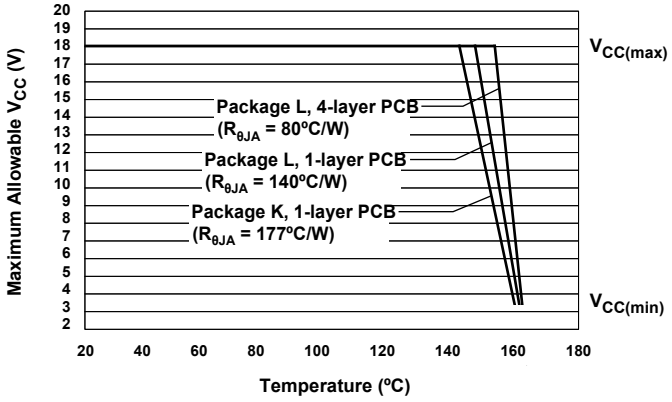


THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

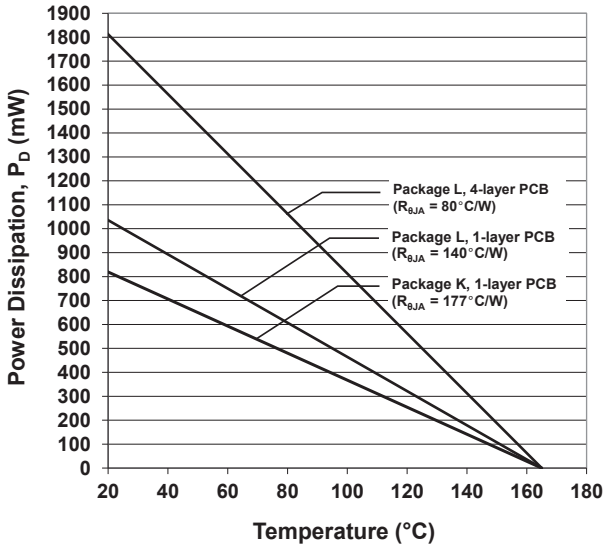
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package K, 1-layer PCB with copper limited to solder pads	177	°C/W
		Package L, 1-layer PCB with copper limited to solder pads	140	°C/W
		Package L, 4-layer PCB based on JEDEC standard	80	°C/W

*Additional thermal data available on the Allegro Website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

HALL TECHNOLOGY

The single-chip differential Hall-effect sensor IC contains two Hall elements as shown in figure 1, which simultaneously sense the magnetic profile of the ring magnet. The magnetic fields are sensed at different points (spaced at a 2.2 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature-compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

TARGET PROFILING DURING OPERATION

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in figure 3 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the A1667. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

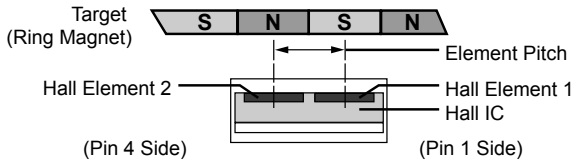

Figure 1. Relative motion of the target is detected by the dual Hall elements mounted on the Hall IC.

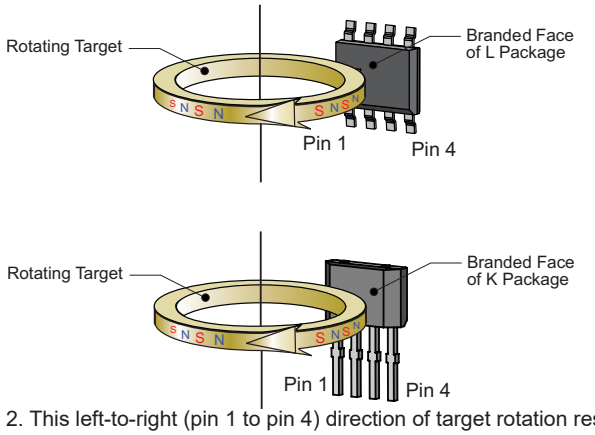

Figure 2. This left-to-right (pin 1 to pin 4) direction of target rotation results in a high output state when a north magnetic pole of the target is nearest the face of the device (see figure 3). A right-to-left (pin 4 to pin 1) rotation inverts the output signal polarity.

DETERMINING OUTPUT SIGNAL POLARITY

In figure 3, the top panel, labeled *Mechanical Position*, represents the mechanical features of the target ring magnet and orientation to the device. The bottom panel, labeled *Device Output Signal*, displays the square waveform corresponding to the digital output signal that results from a rotating ring magnet configured as shown in figure 2. That direction of rotation (of the target side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 4 side. This results in the device output switching from low to high output state as the leading edge of a north magnetic pole passes the device face. In this configuration, the device output voltage switches to its high polarity when a north pole is the target feature nearest to the device. If the direction of rotation is reversed, then the output polarity inverts.

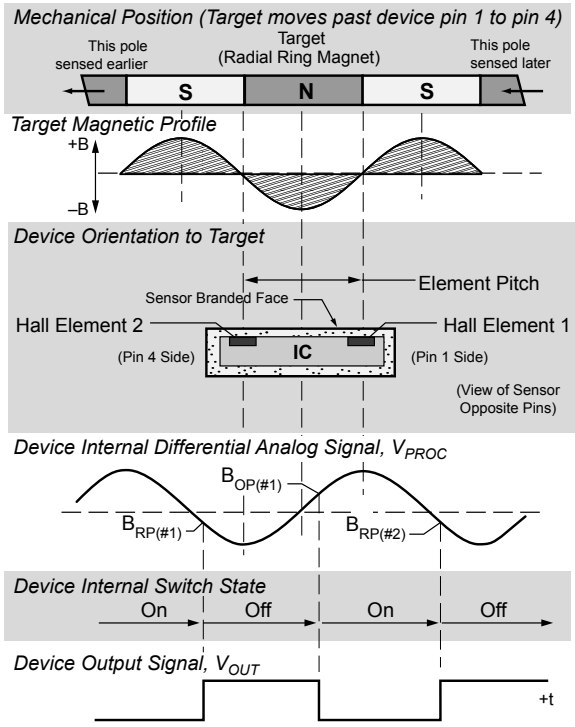

Figure 3. The magnetic profile reflects the geometry of the target, allowing the A1667 to present an accurate digital output response.

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CONTINUOUS UPDATE OF SWITCHPOINTS

Switchpoints are the threshold levels of the differential internal analog signal, V_{PROC}, at which the device changes output signal state. The value of V_{PROC} is directly proportional to the magnetic flux density, B, induced by the target and sensed by the Hall elements. As V_{PROC} rises through a certain limit, referred to as the *operate point*, B_{OP}, the output state changes from high to low. As V_{PROC} falls below B_{OP} to a certain limit, the *release point*, B_{RP}, the output state changes from low to high.

As shown in figure 5, threshold levels for the A1667 switchpoints are established as a function of the peak input signal levels. The A1667 incorporates an algorithm that continuously monitors the input signal and updates the switching thresholds accordingly with limited inward movement of V_{PROC}. The switchpoint for each edge is determined by the detection of the previous two signal edges. In this manner, variations are tracked in real time.

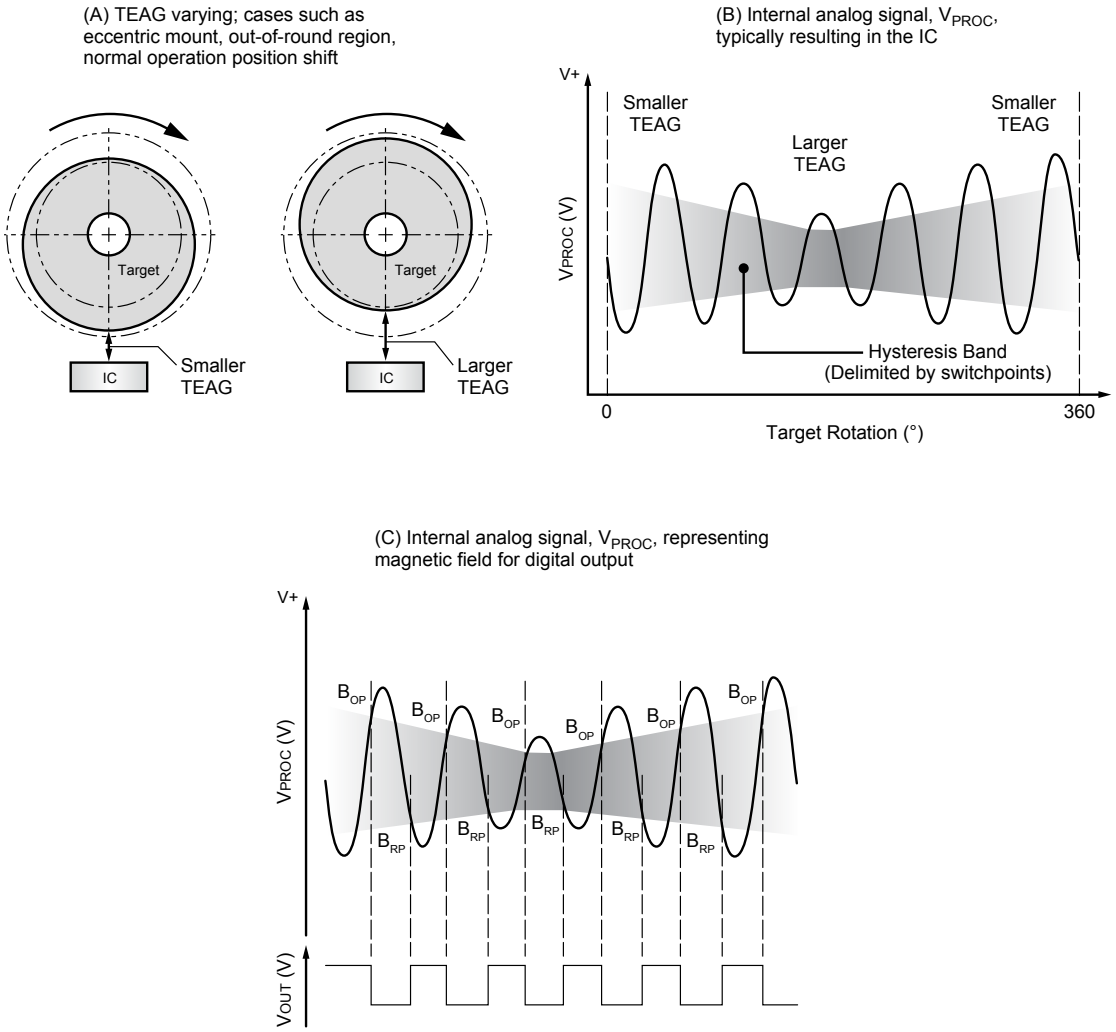

Figure 4. The Continuous Update algorithm allows the Allegro IC to interpret and adapt to variances in the magnetic field generated by the target as a result of eccentric mounting of the target, out-of-round target shape, and similar dynamic application problems that affect the TEAG (Total Effective Air Gap). As shown in panel A, the variance in the target position results in a change in the TEAG. This affects the IC as a varying magnetic field, which results in proportional changes in the internal analog signal, V_{PROC}, shown in panel B. The Continuous Update algorithm is used to establish switchpoints based on the fluctuation of V_{PROC}, as shown in panel C.

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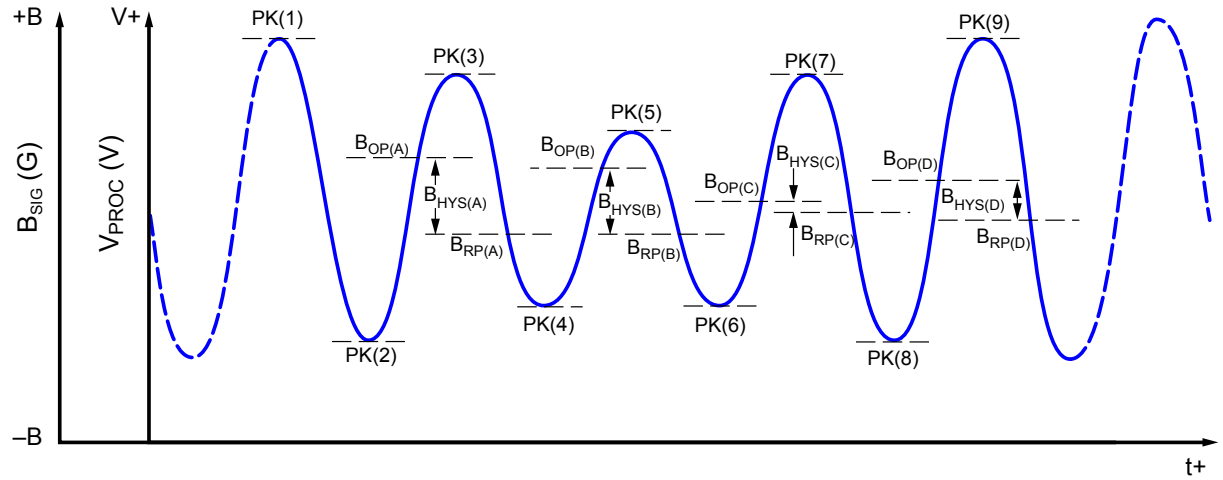

Figure 5. The Continuous Update algorithm operation. Not detailed in the figure are the boundaries for peak capture DAC movement which intentionally limit the amount of inward signal variation the IC is able to react to over a single transition. The algorithm is used to establish and subsequently update the device switchpoints (B_{OP} and B_{RP}). The hysteresis, $B_{HYS(\#x)}$, at each target feature configuration results from this recalibration, ensuring that it remains properly proportioned and centered within the peak-to-peak range of the internal analog signal, V_{PROC}.

Chart Index	Magnetic Field		Peak V_{PROC} Amplitude	Centered Calculated Range, B_{HYS}		
	Target Behavior (Example only)	Peak Magnetic Signal, B_{PK}		Operate Point. B_{OP} (70% $B_{(PKPK)}$ ∝ 70% $V_{PROC(PKPK)}$)	Release Point. B_{RP} (30% $B_{(PKPK)}$ ∝ 30% $V_{PROC(PKPK)}$)	B_{HYS}
PK(1)	TEAG small	+B_{PK} (South Polarity)	$V_{PROCPK(1)}$	$B_{OP(A)}$	(Previous state)	A
PK(2)	TEAG small	–B_{PK} (North Polarity)	$V_{PROCPK(2)}$		$B_{RP(A)}$	
PK(3)	TEAG mid	+B_{PK} (South Polarity)	$V_{PROCPK(3)}$			B
PK(4)	TEAG mid	–B_{PK} (North Polarity)	$V_{PROCPK(4)}$	$B_{OP(B)}$	$B_{RP(B)}$	
PK(5)	TEAG large	+B_{PK} (South Polarity)	$V_{PROCPK(5)}$			C
PK(6)	TEAG large	–B_{PK} (North Polarity)	$V_{PROCPK(6)}$	$B_{OP(C)}$	$B_{RP(C)}$	
PK(7)	TEAG mid	+B_{PK} (South Polarity)	$V_{PROCPK(7)}$			D
PK(8)	TEAG mid	–B_{PK} (North Polarity)	$V_{PROCPK(8)}$	$B_{OP(D)}$	$B_{RP(D)}$	
PK(9)	TEAG small	+B_{PK} (South Polarity)	$V_{PROCPK(9)}$			
				(Next state)		

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START MODE HYSTERESIS

This feature helps to ensure optimal self-calibration by rejecting electrical noise and low-amplitude target vibration during initialization. This prevents AGC from calibrating the IC on such spurious signals. Calibration can be performed using the actual target features.

A typical scenario is shown in figure 6. The Start Mode Hysteresis, PO_{HYS}, is a minimum level of the peak-to-peak amplitude of the internal analog electrical signal, V_{PROC}, that must be exceeded before the A1667 starts to compute switchpoints.

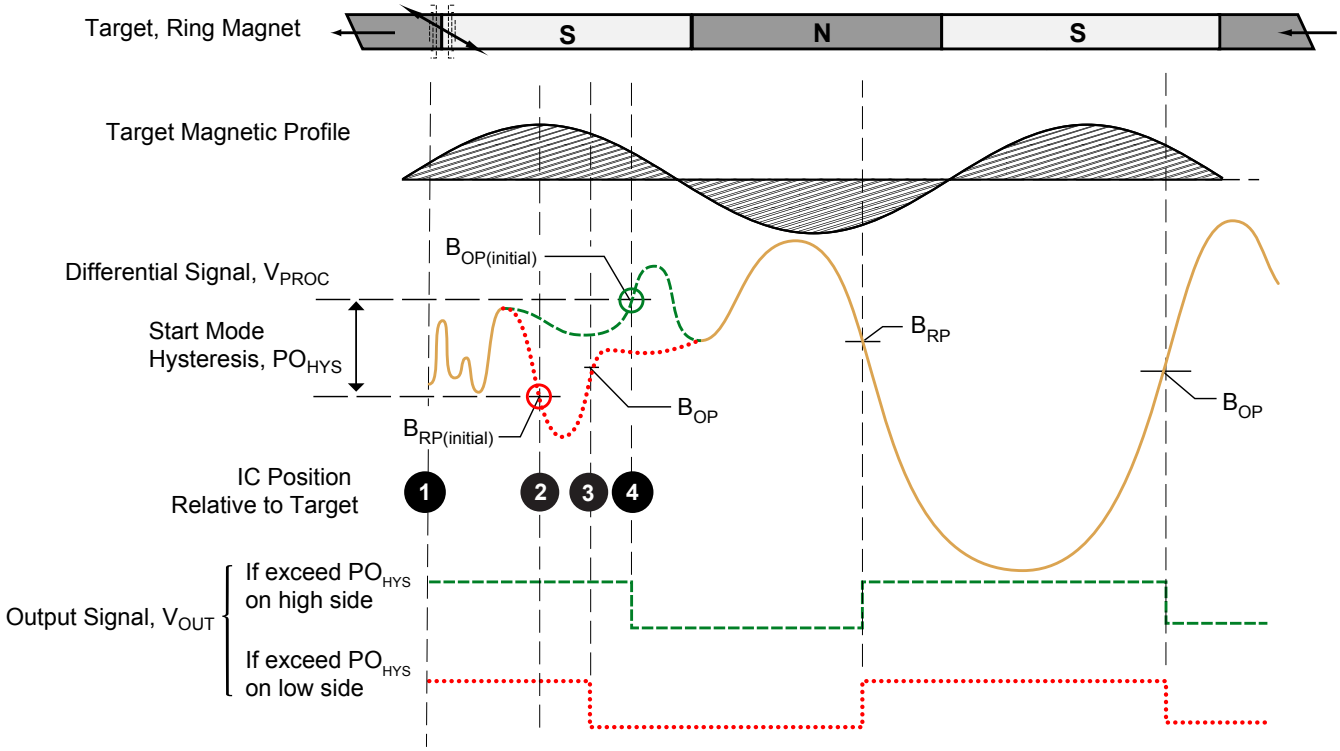

Figure 6. Operation of Start Mode Hysteresis

- At power-on (position 1), the A1667 begins sampling V_{PROC}.
- At the point where the Start Mode Hysteresis, PO_{HYS}, is exceeded, the device establishes an initial switching threshold, by using the Continuous Update algorithm. If V_{PROC} is falling through the limit on the low side (position 2), the switchpoint is B_{RP}, and if V_{PROC} is rising through the limit on the high side (position 4), it is B_{OP}. After this point, Start Mode Hysteresis is no longer a consideration. Note that a valid V_{PROC} value exceeding the Start Mode Hysteresis can be generated either by a legitimate target feature or by excessive vibration.
- In either case, because the switchpoint is immediately passed as soon as it is established, the A1667 enables switching:
  --If on the low side, at B_{RP} (position 2) the output would switch from low to high. However, because output is already high, no output switching occurs. At the next switchpoint, where B_{OP} is passed (position 3), the output switches from high to low.
  --If on the high side, at B_{OP} (position 4) the output switches from high to low.

As this example demonstrates, initial output switching occurs with the same polarity, regardless of whether the Start Mode Hysteresis is exceeded on the high side or on the low side.

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UNDERVOLTAGE LOCKOUT

When the supply voltage falls below the undervoltage lockout voltage, $V_{CC(UV)}$, the device enters Reset, where the output state returns to the Power-On State (POS) until sufficient V_{CC} is supplied. I_{CC} levels may not meet datasheet limits when $V_{CC} < V_{CC}(min)$. This lockout feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the IC.

POWER SUPPLY PROTECTION

The device contains an on-chip regulator and can operate over a wide V_{CC} range. For devices that must operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, EMI/RFI protection may still be required. Contact Allegro for information on the circuitry needed for compliance with various EMC specifications. Refer to figure 7 for an example of a basic application circuit.

AUTOMATIC GAIN CONTROL (AGC)

This feature allows the device to operate with an optimal internal electrical signal, regardless of the air gap (within the AG specification). At power-on, the device determines the peak-to-peak amplitude of the signal generated by the target. The gain of the IC is then automatically adjusted. Figure 8 illustrates the effect of this feature.

AUTOMATIC OFFSET ADJUST (AOA)

The AOA circuitry automatically compensates for the effects of chip, magnet, and installation offsets. This circuitry is continuously active, including during both power-on mode and running mode, compensating for any offset drift (within the Allowable User Induced Differential Offset). Continuous operation also allows it to compensate for offsets induced by temperature variations over time.

RUNNING MODE LOCKOUT

The A1667 has a running mode lockout feature to prevent switching in response to small signals that are characteristic of vibration signals. The internal logic of the chip considers small signal amplitudes below a certain level to be vibration. The output is held to the state prior to lockout until the amplitude of the signal returns to normal operational levels.

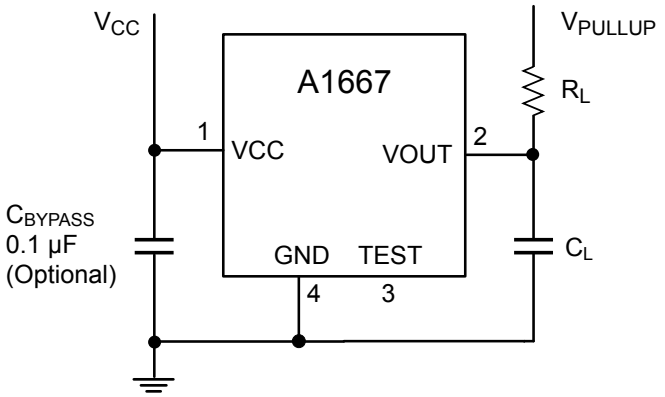

Figure 7. Typical circuit for proper device operation.

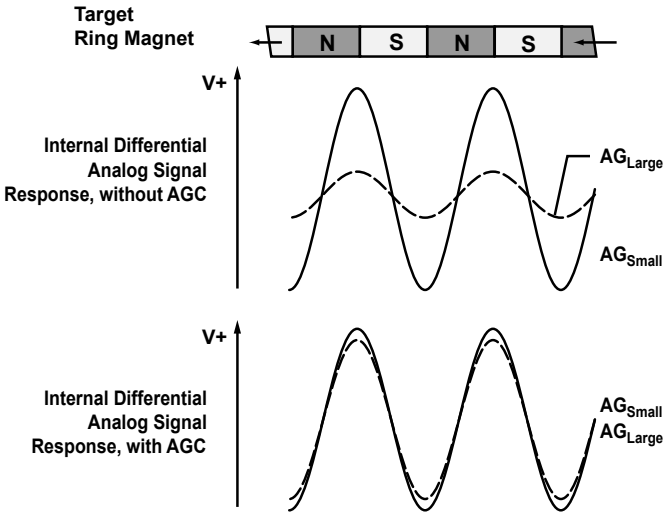

Figure 8. Automatic Gain Control (AGC). The AGC function corrects for variances in the air gap. Differences in the air gap cause differences in the magnetic field at the device, but AGC prevents that from affecting device performance, as shown in the lowest panel.

POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 7.5 mA, and $R_{\theta JA}$ = 177°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 7.5\ mA = 90\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 90\ mW \times 177°C/W = 11.3°C$$

$$T_J = T_A + \Delta T = 25°C + 11.3°C = 36.3°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package K, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=177°C/W, $T_{J(max)}$ =165°C, $V_{CC(max)}$ =24 V, and $I_{CC(max)}$ = 12 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 177°C/W = 84.7\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 119\ mW \div 12\ mA = 7.1\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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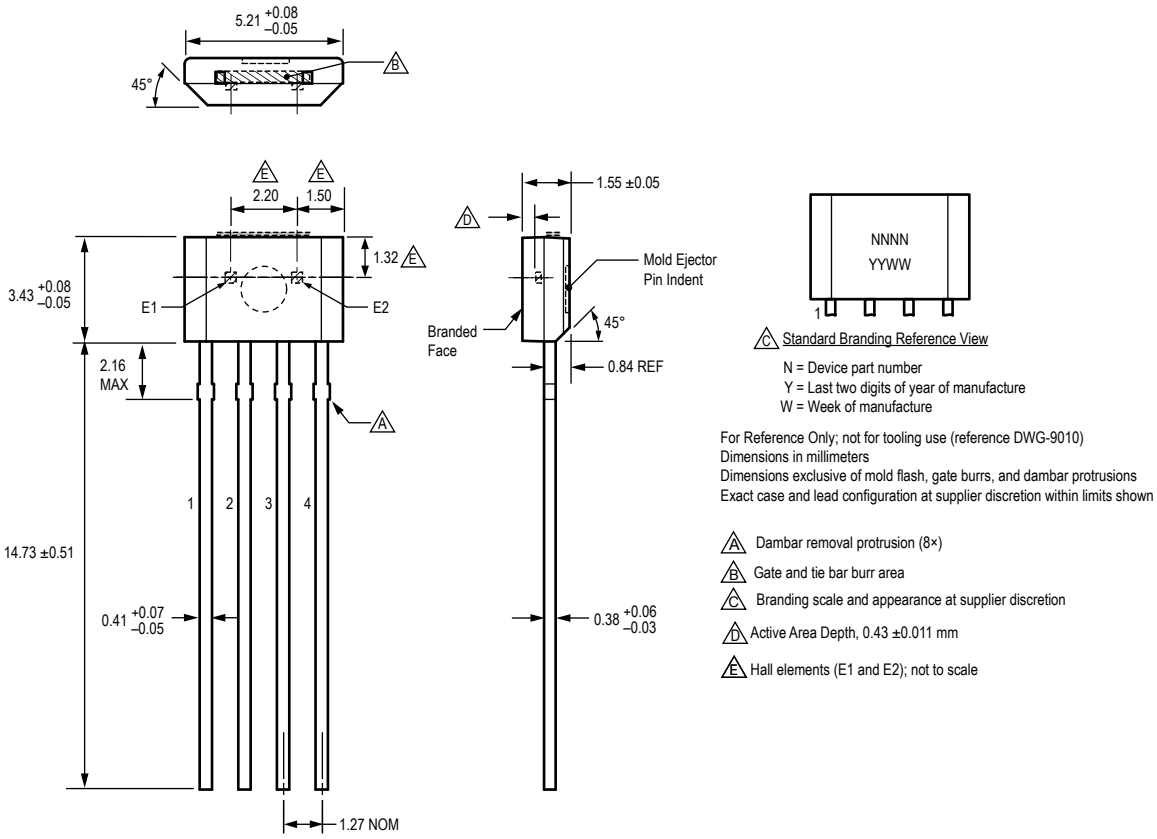
Package K, 4-Pin SIP



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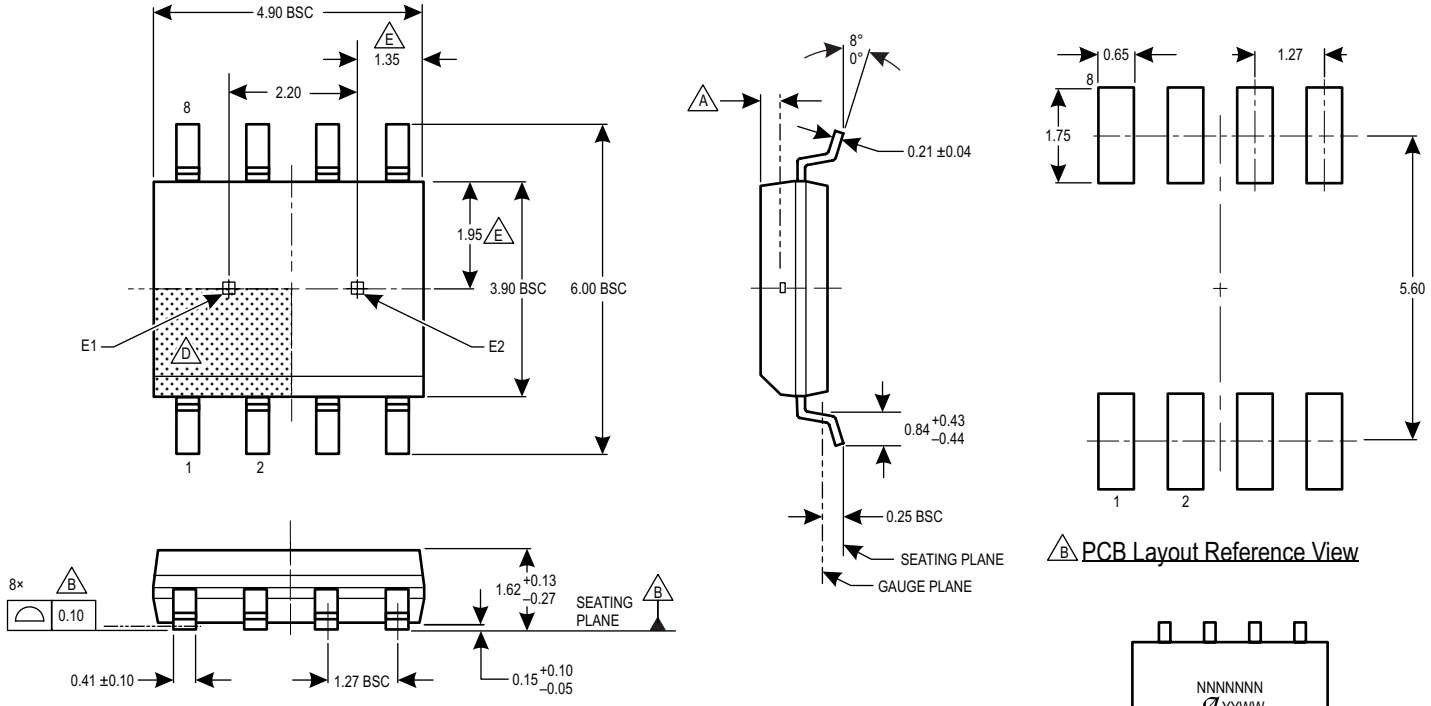
Package L, 8-Pin SOIC

For Reference Only – Not for Tooling Use

(Reference DWG-0000385)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.40 mm NOM

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Terminal #1 mark area

E Hall elements (E1 and E2); not to scale

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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Revision History

Number	Date	Description
1	May 13, 2016	Added L package option
2	April 4, 2017	Corrected K package active area depth
3	October 4, 2018	Corrected L package Hall element spacing; minor editorial updates

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