CHANGE NOTIFICATION

Analog Devices, Inc.
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June 20, 2017

Dear Sir/Madam:

PCN# 062017

Subject: Notification of Change to LTC3884 Die and Datasheet

Please be advised that Linear Technology Corporation has made enhancements to the LTC3884 product die to improve performance in the following areas:

1) Fix errata
2) Reduce power up times
3) Reduce the ADC update period
4) Improve on-chip EEPROM robustness
5) Support I^2C PMBus thresholds compatible with bus power supplies as low as 1.8 volts
6) Reduced TON_MIN

The documented errata in the LTC3884 are eliminated. Refer to the following link for the current errata documents http://cds.linear.com/docs/en/spec-notice/er3884f.pdf.

T_{INIT}, the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 65ms to 35ms. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner. The ADC update period, $T_{CONVERT}$, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters. The above changes are shown on the attached pages of the marked up datasheet.

Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth events are a repeat of the fourth event if the part is reset. However, when reading the fault log from RAM, all 6 events of cyclical data are available.

I^2C thresholds are reduced in order to support PMBus communication with other ICs using I/O interface supplies as low as 1.8 volts. TON_MIN will be reduced from nominally 90ns to 60ns in to support large step down rations at relatively high switching frequencies. The new silicon can be identified by the MFR_SPECIAL_ID, PMBus command code 0xE7, with a value of 0x460* where * is a value of 8-F.

The die changes were qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. The revised product will have successfully completed 1000 hours burn-in before production release. Product built using the revised die will be shipped after August 20, 2017.

Linear Technology will accept requests for revised samples within 30 days of the date of this notification. If we don't hear back from your company within this 30 day period, we will assume acceptance of this Change Notice by August 20, 2017.

Should you have any further questions, please feel free to contact your local Analog Devices Inc. sales person or you may contact me at 408-432-1900 ext. 2077, or by E-mail JASON.HU@ANALOG.COM.

Sincerely,

Jason Hu
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Notes 2, 3). V_{IN} = 12V, $EXTV_{CC}$ = 0V, $V_{RUN0,1}$ = 3.3V, f_{SYNC} = 500kHz (externally driven) and all programmable parameters at factory default, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Input Voltage							
V_{IN}	Input Voltage Range	(Note 11)	●	4.5		38	V
I_Q	Input Voltage Supply Current	$V_{RUN0,1}$ = 3.3V (Note 16) $V_{RUN0,1}$ = 0V (Note 16)			25 23		mA mA
V_{UVLO}	Undervoltage Lockout Threshold When V_{IN} > 4.3V	V_{INTVCC} Falling V_{INTVCC} Rising			3.55 3.90		V V
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			~~65~~ 35		ms
$t_{OFF(MIN)}$	Short Cycle Retry Time				120		ms
Control Loop							
V_{OUTRL}	Full-Scale Voltage Range Set Point Accuracy (0.6V ~ 2.5V) Resolution LSB Step Size	VOUT_COMMAND = 2.75V, MFR_PWM_MODE[1] = 1 (Notes 9, 10, 13)	● ●	2.7 –0.5	 12 0.688	2.8 0.5	V % Bits mV
V_{OUTRH}	Full-Scale Voltage Range Set Point Accuracy (0.6V ~ 5.0V) Resolution LSB Step Size	VOUT_COMMAND = 5.5V, MFR_PWM_MODE[1] = 0 (Notes 9, 10, 13)	● ●	5.40 –0.5	 12 1.375	5.60 0.5	V % Bits mV
$V_{LINEREG}$	Line Regulation	6V < V_{IN} < 38V	●			±0.02	%/V
$V_{LOADREG}$	Load Regulation	ΔV_{ITH} = 1.35V ~ 0.7V ΔV_{ITH} = 1.35V ~ 2V	● ●		0.01 –0.01	0.1 –0.1	% %
$I_{ISENSE0,1}$	Input Pin Bias Current	0V ≤ V_{PIN} ≤ 5.5V	●		±1	±3	µA
$V_{SENSERIN0,1}$	V_{SENSE} Input Resistance to GND	0V ≤ V_{PIN} ≤ 5.5V			50		kΩ
V_{ILIMIT}	N				12		Steps
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7],[2]=0, 1, I_{LIM}[3:0]=1100, V_{OUT} ≤ 3.5V (Note 15) MFR_PWM_MODE[7],[2]=0, 1, I_{LIM}[3:0]=0001, V_{OUT} ≤ 3.5V MFR_PWM_MODE[7],[2]=0, 1, V_{OUT} ≥ V_{OV}	●	14.5	16.5 9.5 –7.5	18.5	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=1, 1, I_{LIM}[3:0]=1100,V_{OUT} ≤ 3.5V MFR_PWM_MODE[7][2]=1, 1, I_{LIM}[3:0]=0001,V_{OUT} ≤ 3.5V MFR_PWM_MODE[7][2]=1, 1, V_{OUT} ≥ V_{OV}	●	27.0	29.5 17.0 –15	31.0	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=0, 0, I_{LIM}[3:0]=1100 MFR_PWM_MODE[7][2]=0, 0, I_{LIM}[3:0]=0001 MFR_PWM_MODE[7][2]=0, 0, V_{OUT} ≥ V_{OV}	●	35	42 25 –18.8	49	mV mV mV
	V_{ILIM_HIGH} V_{ILIM_LOW} V_{REV}	MFR_PWM_MODE[7][2]=1, 0, I_{LIM}[3:0]=1100 MFR_PWM_MODE[7][2]=1, 0, I_{LIM}[3:0]=0001 MFR_PWM_MODE[7][2]=1, 0, V_{OUT} ≥ V_{OV}	●	67.5	74.5 43.5 –37.5	81.5	mV mV mV
$g_{m0,1}$	Resolution Error Amplifier $g_{m(MAX)}$ Error Amplifier $g_{m(MIN)}$ LSB Step Size	$I_{TH0,1}$ = 1.35V, MFR_PWM_CONFIG[7:5] = 0 to 7			3 5.76 1 0.68		Bits mmho mmho mmho
$R_{TH0,1}$	Resolution Compensation Resistor $R_{TH(MAX)}$ Compensation Resistor $R_{TH(MIN)}$	MFR_PWM_CONFIG[4:0] = 0 to 31 (See Figure 1)			5 70 0.5		Bits kΩ kΩ
Gate Drivers							
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω

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SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω
TG t_r t_f	TG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
BG t_r t_f	BG Transition Time: Rise Time Fall Time	(Note 4) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 30 30		 ns ns
TG/BG, t_{1D}	Top Gate Off to Bottom Gate on Delay Time	(Note 4) C_{LOAD} = 3300pF at Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate on Delay Time	(Note 4) C_{LOAD} = 3300pF at Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time				~~90~~60		ns
OV/UV Output Voltage Supervisor Channel 0/1							
N	Resolution				9		Bits
$V_{OUSTPSP\_RL}$	LSB Step Size	MFR_PWM_MODE[1] = 1 (Note 13)			5.6		mV
$V_{OUSTPSP\_RH}$	LSB Step Size	MFR_PWM_MODE[1] = 0 (Note 13)			11.2		mV
V_{RANGE_RL}	Voltage Monitoring Range	MFR_PWM_MODE[1] = 1		0.5		2.7	V
V_{RANGE_RH}	Voltage Monitoring Range	MFR_PWM_MODE[1] = 0		1		5.6	V
V_{THAC0_RL}	Threshold Accuracy 1V < V_{OUT} < 2.5V	MFR_PWM_MODE[1] = 1	●			±1.5	%
V_{THAC1_RH}	Threshold Accuracy 2V < V_{OUT} < 5.5V	MFR_PWM_MODE[1] = 0	●			±1.5	%
t_{PROPOV}	OV Comparator Response Time	V_{OD} = 10% of Threshold				100	µs
t_{PROPUV}	UV Comparator Response Time	V_{OD} = 10% of Threshold				100	µs
V_{IN} Voltage Supervisor							
N	Resolution				9		Bits
V_{INSTP}	LSB Step Size				76		mV
V_{IN}	Full-Scale Voltage			4.5		38	V
$V_{INTHACCM}$	Threshold Accuracy 9V < V_{IN} < 38V Threshold Accuracy 4.5V < V_{IN} ≤ 9V					±3 ±6.0	% %
$t_{PROPVIN}$	Comparator Response Time (VIN_ON and VIN_OFF)	V_{OD} = 10% of threshold				100	µs
Output Voltage Readback							
N	Resolution				16		Bits
V_{OUTSTP}	LSB Step Size				244		µV
$V_{F/S}$	Full-Scale Sense Voltage	V_{RUNn} = 0 (Note 8)			8		V
V_{OUT_TUE}	Total Unadjusted Error	V_{OUT} > 0.6V (Note 8)	●	–0.5		0.5	%
V_{OS}	Zero-Code Offset Voltage					±500	µV
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~90		ms
V_{IN} Voltage Readback							
N	Resolution	(Note 5)			10		Bits
$V_{F/S}$	Full-Scale Input Voltage	(Note 11)			43		V
V_{INTUE}	Total Unadjusted Error	V_{VIN} > 4.5V (Note 8)	●			0.5 2	% %
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~90		ms

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SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Output Current Readback							
N	Resolution	(Note 5)			10		Bits
$V_{IOUTSTP}$	LSB Step Size	0V ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 16mV 16mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 32mV 32mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 64mV 64mV ≤ $\lvert V_{ISENSE}^+ - V_{ISENSE}^- \rvert$ < 128mV			15.63 31.25 62.5 125		µV µV µV µV
$I_{F/S}$	Full-Scale Input Current	(Note 7) DCR or R_{ISENSE} = 1mΩ			±128		A
I_{OUT_TUE}	Total Unadjusted Error	$V_{ISENSE}^+ - V_{ISENSE}^-$ > 6mV (Note 8)	●			±1.25	%
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~ 90		ms
Input Current Readback							
N	Resolution	(Note 5)			10		Bits
V_{IINSTP}	LSB Step Size Full-Scale Range = 16mV LSB Step Size Full-Scale Range = 32mV LSB Step Size Full-Scale Range = 64mV	Gain = 8, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 5mV Gain = 4, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 20mV Gain = 2, 0V ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ ≤ 50mV			15.26 30.52 61		µV µV µV
I_{IN_TUE}	Total Unadjusted Error	Gain = 8, 2.5mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ V_{IN} = 8V (Note 8) Gain = 4, 4mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ V_{IN} = 8V (Note 8) Gain = 2, 6mV ≤ $\lvert V_{IIN}^+ - V_{IIN}^- \rvert$ V_{IN} = 8V (Note 8)	● ● ●			±2 ±1.3 ±1.2	% % %
V_{OS}	Zero-Code Offset Voltage					±50	µV
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~ 90		ms
Supply Current Readback							
N	Resolution	(Note 5)			10		Bits
$V_{ICHIPSTP}$	LSB Step Size Full-Scale Range = 256mV				244		µV
$I_{CHIPTUE}$	Total Unadjusted Error	$\lvert V_{IIN}^+ - V_{IN} \rvert$ ≤ 150mV (Note 19)	●			±3	%
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~ 90		ms
Temperature Readback (T0, T1)							
T_{RES_T}	Resolution				0.25		°C
T0_TUE	External Temperature Total Unadjusted Readback Error	TSNS0, TSNS1 ≤ 1.85V (Note 8) MFR_PWM_MODE_[6] = 0 MFR_PWM_MODE_[6] = 1 (Note 14)		 –3 –10		 3 10	 °C °C
T1_TUE	Internal TSNS TUE	$V_{RUN0,1}$ = 0.0, f_{SYNC} = 0kHz (Note 8)			±1		°C
$t_{CONVERT}$	Update Rate	(Note 6)			~~100~~ 90		ms
$INTV_{CC}$ Regulator/$EXTV_{CC}$							
V_{INTVCC}	Internal V_{CC} Voltage No Load	6V ≤ V_{IN} ≤ 38V		5.25	5.5	5.75	V
V_{LDO_INT}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA, 6V ≤ V_{IN} ≤ 38V			0.5	±2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	V_{IN} ≥ 7V, $EXTV_{CC}$ Rising		4.5	4.7		V
V_{LDO_HYS}	$EXTV_{CC}$ Hysteresis				290		mV
V_{LDO_EXT}	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5.5V			50	100	mV
V_{IN_THR}	V_{IN} Threshold to Enable $EXTV_{CC}$ Switchover	V_{IN} Rising			7		V

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SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
V_{IN_THF}	V_{IN} Threshold to Disable $EXTV_{CC}$ Switchover	V_{IN} Falling			6.5		V
V_{DD33} Regulator							
V_{DD33}	Internal V_{DD33} Voltage	4.5V < V_{INTVCC} or 4.8V < V_{EXTVCC}		3.2	3.3	3.4	V
I_{LIM}	V_{DD33} Current Limit	V_{DD33} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			100		mA
V_{DD33_OV}	V_{DD33} Overvoltage Threshold				3.5		V
V_{DD33_UV}	V_{DD33} Undervoltage Threshold				3.1		V
V_{DD25} Regulator							
V_{DD25}	Internal V_{DD25} Voltage				2.5		V
I_{LIM}	V_{DD25} Current Limit	V_{DD25} = GND, V_{IN} = $INTV_{CC}$ = 4.5V			80		mA
Oscillator and Phase-Locked Loop							
f_{RANGE}	PLL SYNC Range	Syncronized with Falling Edge of SYNC	●	200		1000	kHz
f_{OSC}	Oscillator Frequency Accuracy	Frequency Switch = 250.0 to 1000.0 kHz	●			±7.5	%
$V_{TH(SYNC)}$	SYNC Input Threshold	V_{SYNC} Falling V_{SYNC} Rising			1 1.5		V V
$V_{OL(SYNC)}$	SYNC Low Output Voltage	I_{LOAD} = 3mA			0.2	0.4	V
$I_{LEAK(SYNC)}$	SYNC Leakage Current in Slave Mode	0V ≤ V_{PIN} ≤ 3.6V				±5	µA
θSYNC-θ0	SYNC to Ch0 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG0	MFR_PWM_CONFIG[2:0] = 0,2,3 MFR_PWM_CONFIG[2:0] = 5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0]= 4,6			0 60 90 120		Deg Deg Deg Deg
θSYNC-θ1	SYNC to Ch1 Phase Relationship Based on the Falling Edge of Sync and Rising Edge of TG1	MFR_PWM_CONFIG[2:0] = 3 MFR_PWM_CONFIG[2:0] = 0 MFR_PWM_CONFIG[2:0] = 2,4,5 MFR_PWM_CONFIG[2:0] = 1 MFR_PWM_CONFIG[2:0] = 6			120 180 240 270 300		Deg Deg Deg Deg Deg
EEPROM Characteristics							
Endurance	(Note 12)	0°C < T_J < 85°C EEPROM Write Operations	●	10,000			Cycles
Retention	(Note 12)	T_J < 125°C	●	10			Years
Mass_Write	Mass Write Operation Time	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operation	●		440	4100	ms
Leakage Current SDA, SCL, $\overline{ALERT}$, RUN							
I_{OL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V	●			±5	µA
Leakage Current $\overline{FAULT}n$, PGOOD*n*							
I_{GL}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
Digital Inputs SCL, SDA, RUN*n*, $\overline{GPIO}n$							
V_{IH}	Input High Threshold Voltage		●			~~2~~ 1.35	V
V_{IL}	Input Low Threshold Voltage		●	~~1.4~~		0.8	V
V_{HYST}	Input Hysteresis	SCL, SDA			0.08		V
C_{PIN}	Input Capacitance					10	pF
Digital Input WP							
I_{PUWP}	Input Pull-Up Current	WP			10		µA
Open-Drain Outputs SCL, SDA, $\overline{FAULT}n$, $\overline{ALERT}$, RUN*n*, SHARE_CLK, PGOOD*n*							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA				0.4	V