CY91590 Series

FR Family FR81S 32-Bit Microcontroller

This series is Cypress 32-bit microcontroller designed for automotive and industrial control applications. It contains the FR81S CPU that is compatible with the FR family. The FR81S has a high level performance among the Cypress FR family by enhancing CPU instruction pipeline and load store processing, and improving internal bus transfer.
It is best suited for application control for automotive.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency:

  128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))

  It shows maximum CPU frequency of series. The specification of each part number can be referred in “Product Lineup” and “Electrical Characteristics.”
- General-purpose register: 32 bits ×16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift instruction etc.
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions
  - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  - Reduced overhead during branch process
- Register interlock function
  - Easy assembler writing
- The support at the built-in / instruction level of the multiplier
  - Signed 32-bit multiplication: 5 cycles
  - Signed 16-bit multiplication: 3 cycles
- Interrupt (PC/PS saving)
  - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
  - Main oscillation (4 MHz)
  - Sub oscillation (32 kHz) or none sub oscillation
  - PLL multiplication rate: 1 to 32 times
- Built-in Program flash memory capacity 2048 + 64KB (series maximum)
- Built-in Data flash memory capacity(WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM 192 KB (Series maximum)
  - Sub RAM (on AHB) 64 KB (Series maximum)
  - Backup RAM 8 KB
- General-purpose ports (5V Pin): 63 (dual clock products: 61)
  - Included I^2C pseudo open drain support ports: 4
- General-purpose ports (3V Pin): 93
  - Included 48 combined external bus interface (For GDC external memory I/F)
- External bus interface
  - GDC external memory for I/F use
  - 25-bit address, 16-bit data
  - Power supply voltage fixed to 3.3 V
- DMA Controller
  - Up to 16 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
  - 8/10-bit resolution: 32 channels
  - Conversion time: 3 µs
- External interrupt input: 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- LIN-UART
  - 6 channels, ch.2 to ch.7
  - UART, synchronous mode, LIN-UART mode is selectable.
  - LIN protocol Revision 2.1 is supported
  - SPI (Serial Peripheral Interface) supported (synchronous mode)
  - Full-duplex double buffering system
  - LIN synch break detection (linked to the input capture)
  - Built-in dedicated baud rate generator
  - DMA transfer support

- Multi-function serial communication (built-in transmission/reception FIFO memory):
  - 2 channels for CY91F591/2/4/6/7/9
  - 6 channels for CY91F59A/B

  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detect functions provided
  - DMA transfer support

  <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 9-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detect function is provided
  - DMA transfer support

  <LIN-UART (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - LIN protocol Revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support

  < I^2C >
  - ch.0 and ch.1 only supported
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (C-CAN): 3 channels
  - Transfer speed: Up to 1 Mbps
  - 64-transmission/reception message buffering: 1 channel, 32-transmission/reception message buffering: 2 channels
- Up/down counter: 16-bit × 3 channels for CY91F59A/B
- PPG: 16-bit × 24 channels
- Reload timer:
  - 16-bit × 4 channels for CY91F591/2/4/6/7/9
  - 16-bit × 8 channels for CY91F59A/B
- Free-run timer:
  - 32-bit × 2 channels (Can select each channel for input capture, output compare) for CY91F591/2/4/6/7/9
  - 32-bit × 2 channels (LSYN (LIN synch field detection) for exclusive input capture) for CY91F591/2/4/6/7/9
  - 32-bit × 8 channels (Can select ch.0, 1, 2, and 3 for input capture, output compare) for CY91F59A/B
- Input capture:
  - 32-bit × 6 channels (linked to the free-run timer) for CY91F591/2/4/6/7/9
  - 32-bit × 2 channels (linked to the free-run timer) LSYN (LIN synch field detected) Exclusive for CY91F591/2/4/6/7/9
  - 32-bit × 12 channels (linked to the free-run timer) LSYN (LIN synch field detected) for CY91F59A/B
- Output compare: 32-bit × 4 channels (linked to the free-run timer)
- Sound generator: 5 channels
  - Frequency and amplitude sequencers provided
- Stepping motor controller: 6 channels
  - 8/10-bit PWM
  - High current output supported (4 lines × 6 channels)
  - Can refer back electromotive force using pin-shared A/D converter
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main/sub oscillation frequency can be selected for the operation clock (dual product only)
- Calibration: The hardware watchdog for CR oscillation drive and real-time clock (RTC) for sub clock drive (dual product only)
  - The CR oscillation frequency can be trimmed
  - The main clock to sub clock (dual product only) ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32kHz) (two system clock kinds) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
- Base timer: 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.

- I/O relocation
  - Peripheral function pins can be reassigned.
- Low-power consumption mode
  - Sleep / Stop / Watch / Sub RUN mode
  - Stop (power shutdown) / Watch (power shutdown) mode
  - GDC part self-support power supply
- Power on reset
- Low-voltage detection reset (external low-voltage detection)
- Low-voltage detection reset (internal low-voltage detection)
- GDC
  - Internal/memory frequency: 81 MHz
  - The resolution of the display which can support: 800 × 480 at the maximum
    Screen overlay of five simultaneous layers at the maximum (window)
    Size of the resolution which can be supported varies depending on color format.
  - Analog video input (NTSC)
  - Digital video input (RGB666/555)
  - YUV input (BT.656)
  - Video image expansion/reduction /invert function is supported
  - RGB Digital output (6-bit × 3)
  - Built-in 2D rendering engine
    The line drawing is supported.
    The blt function is supported.
    Display list operation is supported
    8bpp indirect color
    ARGB-1555 direct color
    Alpha blending, anti-aliasing
  - Built-in Sprite engine
    Equipped with automatic display function when booted
    Maximum of 512 sprites are supported
    32 special sprites capable of automatic animation are supported.
    The command list execution is supported.
    1bpp, 2bpp, 4bpp, 8bpp indirect color
    ARGB-1555, RGB-565, ARGB-8888 direct color
    The color format for each sprite can be set.
    Horizontal invert, Vertical invert
    Alpha blending
  - Built-in memory
    - 800 KB(CY91F591/2/4/6/7/9)
    - 1792 KB(CY91F59A/B)
  - HS-SPI(CY91F59A/B)
- Device Package: LQFP-208, HQFP-208*, BGA320, TEQFP-208*
- CMOS 90 nm Technology
- Power supplies
  - 5V/3.3V Power supply
  - The internal 1.2 V is generated from 5 V/3.3 V with the voltage step-down circuit.
  - I/O of an external bus and GDC, 3.3 V power supply used.
  - For other I/O, 5 V power supply used.
  - If 2 power supplies are used, they must turn on in the specified sequence (5 V → 3.3 V).

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

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1. Product Lineup

Item \ Product		CY91F591B/BS	CY91F591BH/BHS
CPU core		FR81S	
Technology		90 nm	
Package		LQFP208	
Sub clock		Yes (Non-S series) No (S series)	
Maximum CPU operating frequency		80 MHz	
Maximum GDC operating frequency		81 MHz	
Built-in CR oscillator		100 kHz	
System clock		On chip PLL	
Flash	Main	576 KB	
	Work	64 KB	
RAM	Main	40 KB	
	Backup	8 KB	
VRAM		260 KB	
Watchdog timer		1 ch Hardware 1 ch Software	
Clock supervisor		Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes	
Low-voltage detection reset (Internal low-voltage detection)		Yes	
NMI function		Yes	
DMA Controller		16 ch	
CAN		1 ch (64 msg) 2 ch (32 msg)	
LIN-UART		6 ch	
Multi-function Serial Interface		2 ch	
A/D converter (8-bit/10-bit)		1 unit/32 ch	
Reload timer(16-bit)		4 ch	
Base timer(16-bit)		2 ch	
Free-run timer(32-bit)		2 ch	
Input capture(32-bit)		6 ch	
Output compare(32-bit)		4 ch	
PPG timer(16-bit)		24 ch	
Sound generator		5 ch	
Real-time clock		Yes	
External interrupt		16 ch	
CR/SUB compensation function		Yes	
CRC generation		Yes	
Stepping motor control		6 ch	
Stop mode (including power shut-off)		Supported	
Power supply voltage		MICOM: 4.5 V to 5.5 V GDC: 3.0 V to 3.6 V	
Operating temperature		-40 °C to +105 °C	
Allowable power [mW]		1250	
Others		Flash product	
On chip debugger		Yes	

Item \ Product		CY91F592B /BS	CY91F592BH /BHS	CY91F594B /BS	CY91F594BH /BHS
CPU core		FR81S			
Technology		90 nm			
Package		LQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		80 MHz			
Maximum GDC operating frequency		81 MHz			
Built-in CR oscillator		100 kHz			
System clock		On chip PLL			
Flash	Main	576 KB		1088 KB	
	Work	64 KB			
RAM	Main	40 KB		64 KB	
	Backup	8 KB			
VRAM		800 KB			
Watchdog timer		1 ch Hardware 1 ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16 ch			
CAN		1 ch (64 msg) 2 ch (32 msg)			
LIN-UART		6 ch			
Multi-function Serial Interface		2 ch			
A/D converter (8-bit/10-bit)		1 unit/32 ch			
Reload timer(16-bit)		4 ch			
Base timer(16-bit)		2 ch			
Free-run timer(32-bit)		2 ch			
Input capture(32-bit)		6 ch			
Output compare(32-bit)		4 ch			
PPG timer(16-bit)		24 ch			
Sound generator		5 ch			
Real-time clock		Yes			
External interrupt		16 ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6 ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM: 4.5 V to 5.5 V GDC: 3.0 V to 3.6 V			
Operating temperature		-40 °C to +105 °C			
Allowable power [mW]		1250			
Others		Flash product			
On chip debugger		Yes			

Item \ Product		CY91F596B /BS*	CY91F596BH /BHS*	CY91F597B /BS*	CY91F597BH /BHS*
CPU core		FR81S			
Technology		90 nm			
Package		HQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		128 MHz			
Maximum GDC operating frequency		81 MHz			
Built-in CR oscillator		100 kHz			
System clock		On chip PLL			
Flash	Main	576 KB			
	Work	64 KB			
RAM	Main	40 KB			
	Backup	8 KB			
VRAM		260 KB		800 KB	
Watchdog timer		1 ch Hardware 1 ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16 ch			
CAN		1 ch (64 msg) 2 ch (32 msg)			
LIN-UART		6 ch			
Multi-function Serial Interface		2 ch			
A/D converter (8-bit/10-bit)		1 unit/32 ch			
Reload timer(16-bit)		4 ch			
Base timer(16-bit)		2 ch			
Free-run timer(32-bit)		2 ch			
Input capture(32-bit)		6 ch			
Output compare(32-bit)		4 ch			
PPG timer(16-bit)		24 ch			
Sound generator		5 ch			
Real-time clock		Yes			
External interrupt		16 ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6 ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature		-40°C to +105°C			
Allowable power [mW]		2500			
Others		Flash product			
On chip debugger		Yes			

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

Item \ Product		CY91F599B/BS*	CY91F599BH/BHS*
CPU core		FR81S	
Technology		90 nm	
Package		HQFP208	
Sub clock		Yes (Non-S series) No (S series)	
Maximum CPU operating frequency		128 MHz	
Maximum GDC operating frequency		81 MHz	
Built-in CR oscillator		100 kHz	
System clock		On chip PLL	
Flash	Main	1088 KB	
	Work	64 KB	
RAM	Main	64 KB	
	Backup	8 KB	
VRAM		800 KB	
Watchdog timer		1 ch Hardware 1 ch Software	
Clock supervisor		Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes	
Low-voltage detection reset (Internal low-voltage detection)		Yes	
NMI function		Yes	
DMA Controller		16 ch	
CAN		1 ch (64 msg) 2 ch (32 msg)	
LIN-UART		6 ch	
Multi-function Serial Interface		2 ch	
A/D Converter (8-bit/10-bit)		1 unit/32 ch	
Reload timer(16-bit)		4 ch	
Base timer(16-bit)		2 ch	
Free-run timer(32-bit)		2 ch	
Input capture(32-bit)		6 ch	
Output compare(32-bit)		4 ch	
PPG timer(16-bit)		24 ch	
Sound generator		5 ch	
Real-time clock		Yes	
External interrupt		16 ch	
CR/SUB compensation function		Yes	
CRC generation		Yes	
Stepping motor control		6 ch	
Stop mode (including power shut-off)		Supported	
Power supply voltage		MICOM: 4.5 V to 5.5 V GDC: 3.0 V to 3.6 V	
Operating temperature		-40 °C to +105 °C	
Allowable power [mW]		2500	
Others		Flash product	
On chip debugger		Yes	

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

Item \ Product		CY91F59AC /F59ACS	CY91F59ACH /F59ACHS	CY91F59BC /F59BCS	CY91F59BCH /F59BCHS
CPU core		FR81S			
Technology		90 nm			
Package		BGA320/TEQFP-208*1			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		128 MHz			
Maximum GDC operating frequency		81 MHz			
Built-in CR oscillator		100 kHz			
System clock		On chip PLL			
Flash	Main	1600 KB		2112 KB	
	Work*2	64 KB			
RAM	Main	192 KB			
	Sub on AHB	64 KB			
	Backup	8 KB			
VRAM		1792 KB			
Watchdog timer		1 ch Hardware 1 ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16 ch			
CAN		1 ch (64 msg) 2 ch (32 msg)			
LIN-UART		6 ch			
Multi-function Serial Interface		6 ch*3			
High Speed SPI (GDC)		Yes			
A/D converter (8-bit/10-bit)		1 unit/32 ch			
Up/down counter(16-bit)		3 ch			
Reload timer(16-bit)		8 ch			
Base timer(16-bit)		2 ch			
Free-run timer(32-bit)		8 ch			
Input capture(32-bit)		12 ch			
Output compare(32-bit)		4 ch			
PPG timer(16-bit)		24 ch			
Sound generator		5 ch			
Real-time clock		Yes			
External interrupt		16 ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6 ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM: 4.5 V to 5.5 V GDC: 3.0 V to 3.6 V			
Operating temperature		-40 °C to +105 °C			
Allowable power [mW]		2500			
Others		Flash product			
JTAG Boundary Scan Test		Yes (Only support BGA package products)			
On chip debugger		Yes			

*1: Under consideration.

*2: Start address of Work Flash memory is different between CY91F591/2/4/6/7/9 and CY91F59A/B.

*3: I^2C is supported with ch.0 and ch.1 only.

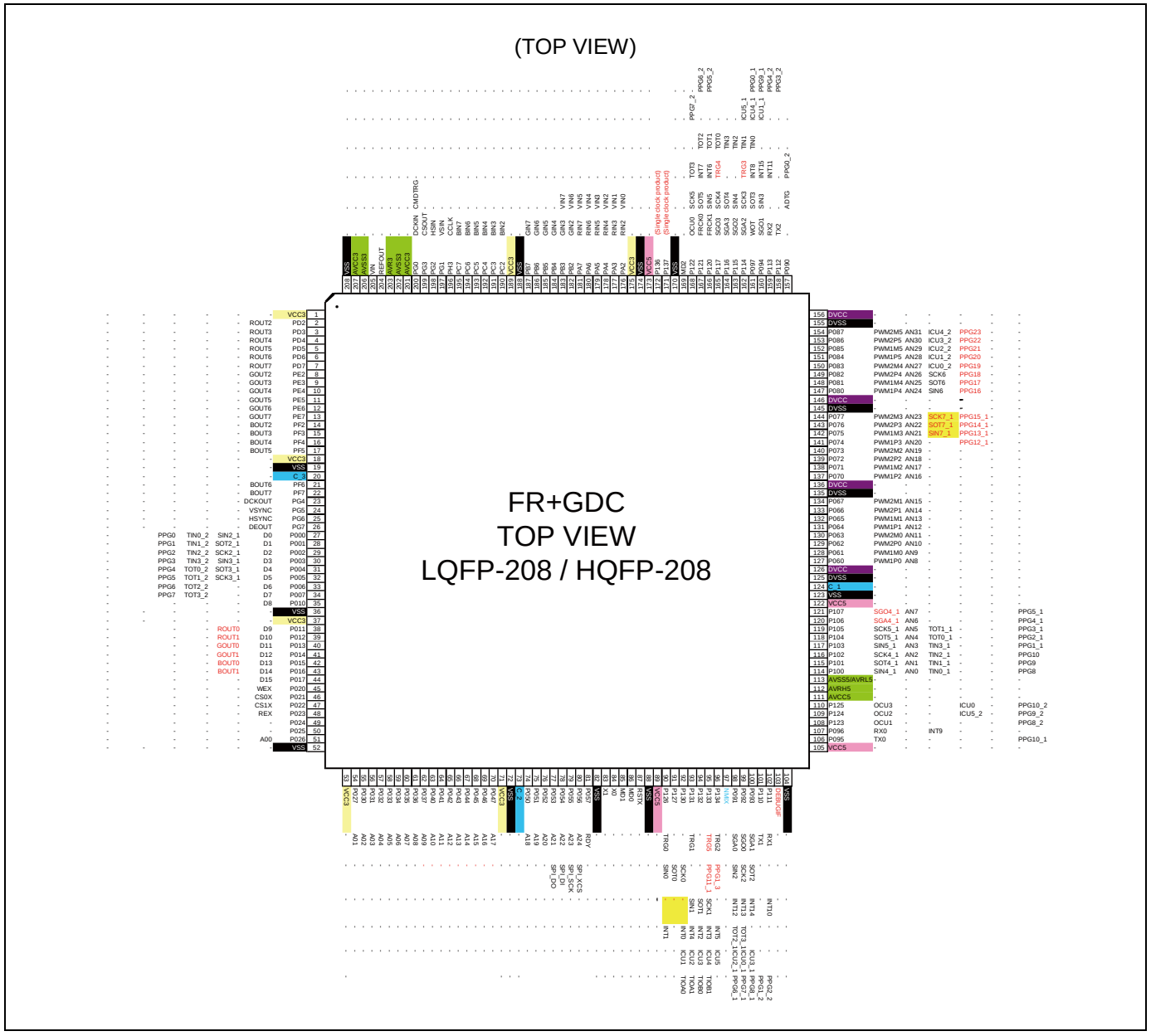
Main difference of functionality between CY91F594 and CY91F59B

Part	Item	CY91F594	CY91F59B
MCU part	FLASH (main)	1088 KB	2112 KB
	RAM (Main)	64 KB	192 KB
	RAM (Sub on AHB)	-	64 KB
	Multi-function Serial Interface	2 ch	6 ch
	Free-run timer	2 ch	8 ch
	Input Capture	6 ch	12 ch
	Reload timer	4 ch	8 ch
	Up/down counter	-	3 ch
	Package	LQFP208	BGA320/TEQPF-208*
	JTAG Boundary Scan Test	-	Yes (Only support BGA package products)
GDC part	VRAM	800 KB	1792 KB
	High Speed SPI	-	Yes

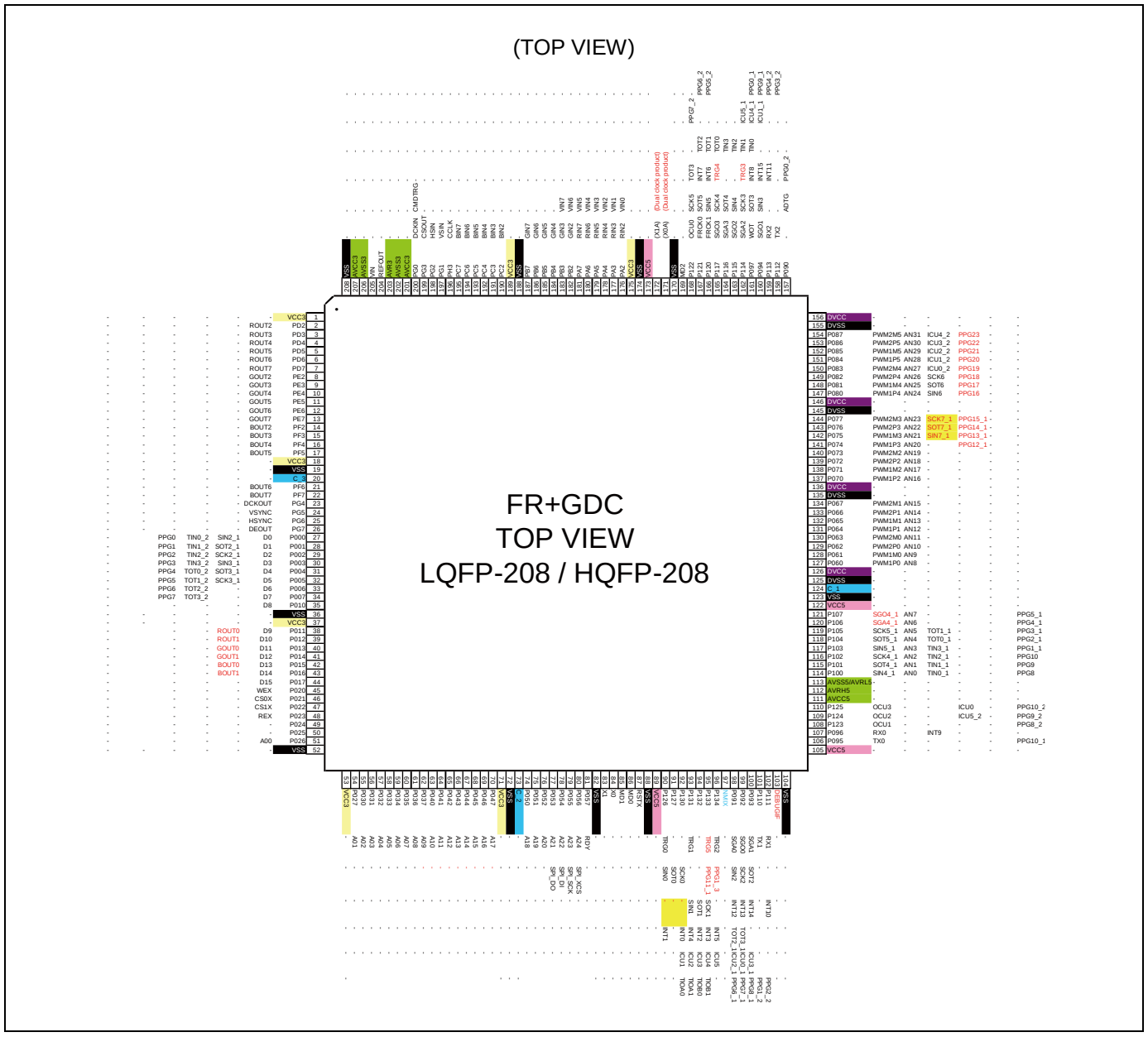
*: Under consideration.

2. Pin Assignment

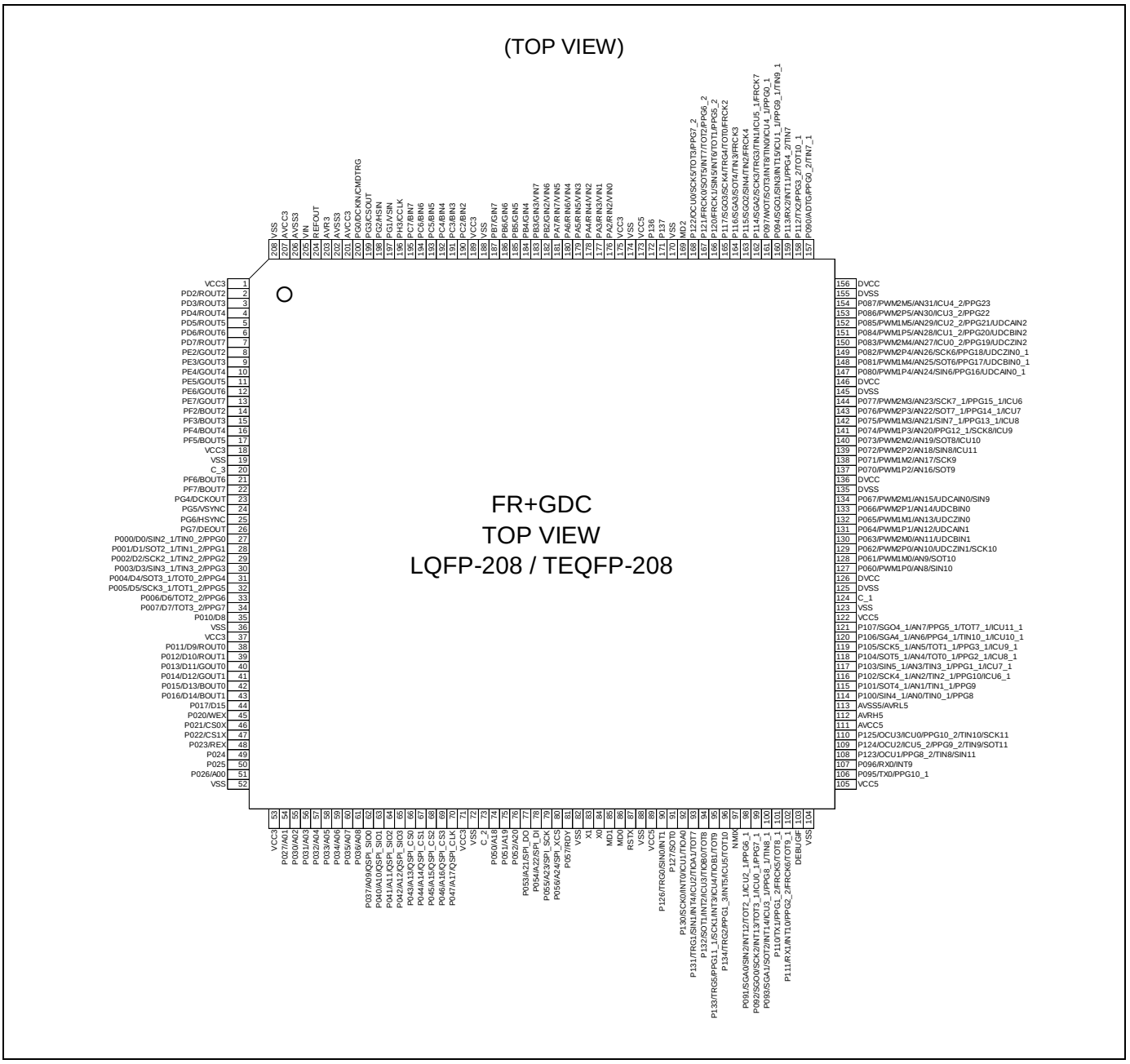
2.1 Pin Assignment (CY91F591/2/4/6/7/9 Single Clock Product)



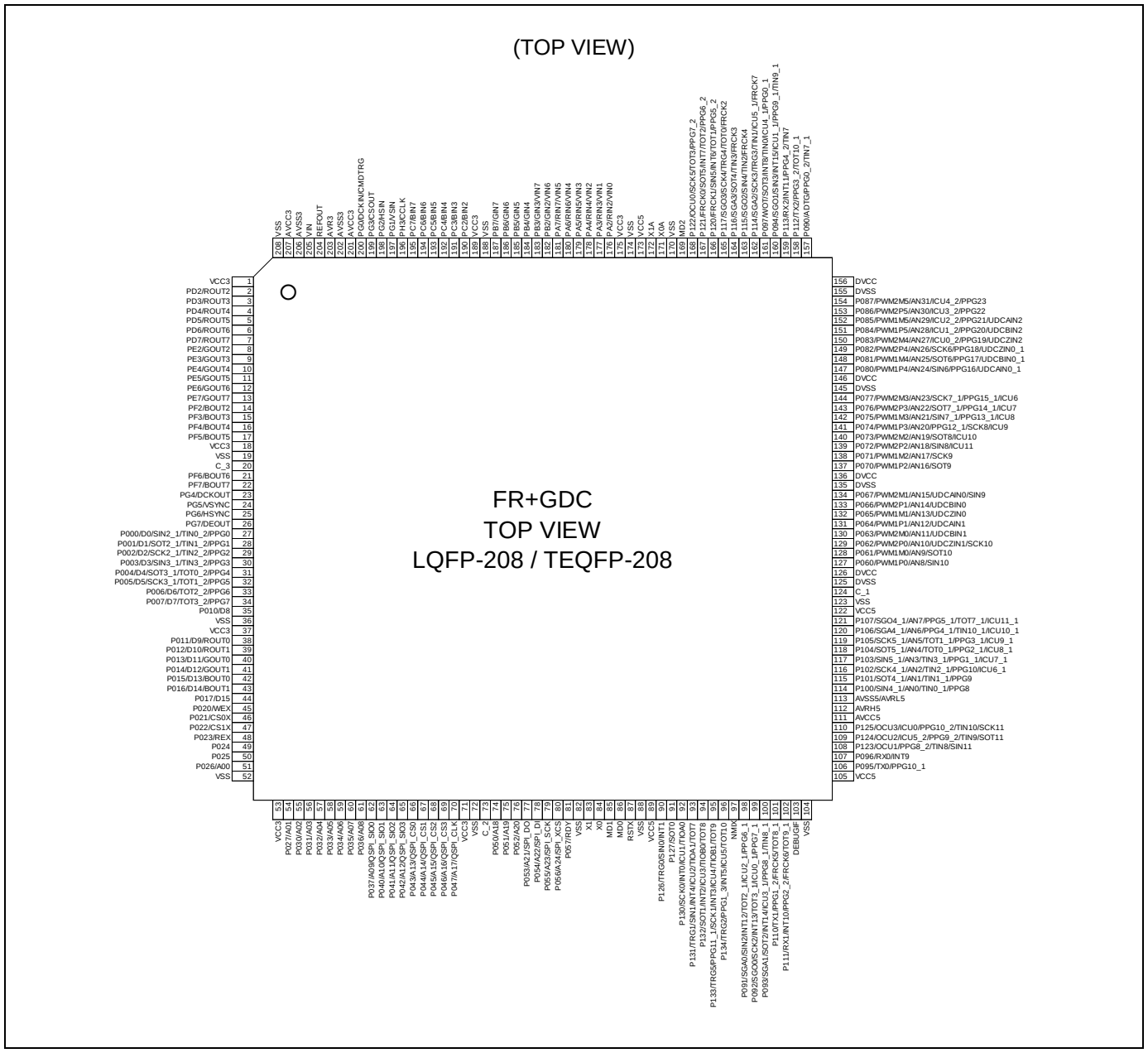
2.2 Pin Assignment (CY91F591/2/4/6/7/9 dual Clock Product)



2.3 Pin Assignment (CY91F59A/B Single Clock Product)



2.4 Pin Assignment (CY91F59A/B dual Clock Product)



2.5 Pin Assignment (BGA Product)

(TOP VIEW)

▲	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A
B	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	21	B
C	75	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	95	22	C
D	74	143	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	161	96	23	D
E	73	142	203	256													219	162	97	24	E
F	72	141	202	255													220	163	98	25	F
G	71	140	201	254			257	258	259	260	261	262	263	264			221	164	99	26	G
H	70	139	200	253			284	285	286	287	288	289	290	265			222	165	100	27	H
J	69	138	199	252			283	304	305	306	307	308	291	266			223	166	101	28	J
K	68	137	198	251			282	303	316	317	318	309	292	267			224	167	102	29	K
L	67	136	197	250			281	302	315	320	319	310	293	268			225	168	103	30	L
M	66	135	196	249			280	301	314	313	312	311	294	269			226	169	104	31	M
N	65	134	195	248			279	300	299	298	297	296	295	270			227	170	105	32	N
P	64	133	194	247			278	277	276	275	274	273	272	271			228	171	106	33	P
R	63	132	193	246													229	172	107	34	R
T	62	131	192	245													230	173	108	35	T
U	61	130	191	244	243	242	241	240	239	238	237	236	235	234	233	232	231	174	109	36	U
V	60	129	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	110	37	V
W	59	128	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	38	W
Y	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

3. Pin Description

3.1 Pin Description of LQFP-208/TEQFP-208

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
84	X0	–	L	Main clock oscillation input pin
83	X1	–	L	Main clock oscillation output pin
171 (dual clock product)	X0A	–	N	Sub clock oscillation input pin
172 (dual clock product)	X1A	–	N	Sub clock oscillation output pin
171 (single clock product)	P137	–	A	General-purpose I/O port
172 (single clock product)	P136	–	A	General-purpose I/O port
97	NMIX	N	F1	Non-masking interrupt input pin
87	RSTX	N	F1	External reset input pin
86	MD0	–	P	Mode pin 0
85	MD1	–	P	Mode pin 1
169	MD2	–	F2	Mode pin 2
27	P000	–	O	General-purpose I/O port (3V pin)
	D0	–		External bus · Data bit0 I/O pin
	SIN2_1	–		LIN-UART ch.2 serial data input pin (1)
	TIN0_2	–		Reload timer ch.0 event input pin (2)
	PPG0	–		PPG ch.0 output pin
28	P001	–	O	General-purpose I/O port (3V pin)
	D1	–		External bus · Data bit1 I/O pin
	SOT2_1	–		LIN-UART ch.2 serial data output pin (1)
	TIN1_2	–		Reload timer ch.1 event input pin (2)
	PPG1	–		PPG ch.1 output pin
29	P002	–	O	General-purpose I/O port (3V pin)
	D2	–		External bus · Data bit2 I/O pin
	SCK2_1	–		LIN-UART ch.2 clock I/O pin (1)
	TIN2_2	–		Reload timer ch.2 event input pin (2)
	PPG2	–		PPG ch.2 output pin
30	P003	–	O	General-purpose I/O port (3V pin)
	D3	–		External bus · Data bit3 I/O pin
	SIN3_1	–		LIN-UART ch.3 serial data input pin (1)
	TIN3_2	–		Reload timer ch.3 event input pin (2)
	PPG3	–		PPG ch.3 output pin
31	P004	–	O	General-purpose I/O port (3V pin)
	D4	–		External bus · Data bit4 I/O pin
	SOT3_1	–		LIN-UART ch.3 serial data output pin (1)
	TOT0_2	–		Reload timer ch.0 output pin (2)
	PPG4	–		PPG ch.4 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
32	P005	–	O	General-purpose I/O port (3V pin)
	D5	–		External bus · Data bit5 I/O pin
	SCK3_1	–		LIN-UART ch.3 clock I/O pin (1)
	TOT1_2	–		Reload timer ch.1 output pin (2)
	PPG5	–		PPG ch.5 output pin
33	P006	–	O	General-purpose I/O port (3V pin)
	D6	–		External bus · Data bit6 I/O pin
	TOT2_2	–		Reload timer ch.2 output pin (2)
	PPG6	–		PPG ch.6 output pin
34	P007	–	O	General-purpose I/O port (3V pin)
	D7	–		External bus · Data bit7 I/O pin
	TOT3_2	–		Reload timer ch.3 output pin (2)
	PPG7	–		PPG ch.7 output pin
35	P010	–	O	General-purpose I/O port (3V pin)
	D8	–		External bus · Data bit8 I/O pin
38	P011	–	O	General-purpose I/O port (3V pin)
	D9	–		External bus · Data bit9 I/O pin
	ROUT0	–		Display digital R0 output pin
39	P012	–	O	General-purpose I/O port (3V pin)
	D10	–		External bus · Data bit10 I/O pin
	ROUT1	–		Display digital R1 output pin
40	P013	–	O	General-purpose I/O port (3V pin)
	D11	–		External bus · Data bit11 I/O pin
	GOUT0	–		Display digital G0 output pin
41	P014	–	O	General-purpose I/O port (3V pin)
	D12	–		External bus · Data bit12 I/O pin
	GOUT1	–		Display digital G1 output pin
42	P015	–	O	General-purpose I/O port (3V pin)
	D13	–		External bus · Data bit13 I/O pin
	BOUT0	–		Display digital B0 output pin
43	P016	–	O	General-purpose I/O port (3V pin)
	D14	–		External bus · Data bit14 I/O pin
	BOUT1	–		Display digital B1 output pin
44	P017	–	O	General-purpose I/O port (3V pin)
	D15	–		External bus · Data bit15 I/O pin
45	P020	–	O	General-purpose I/O port (3V pin)
	WEX	–		External bus · Write enable output pin
46	P021	–	O	General-purpose I/O port (3V pin)
	CS0X	–		External bus · Chip select 0 output pin
47	P022	–	O	General-purpose I/O port (3V pin)
	CS1X	–		External bus · Chip select 1 output pin
48	P023	–	O	General-purpose I/O port (3V pin)
	REX	–		External bus · Read enable output pin
49	P024	–	O	General-purpose I/O port (3V pin)
50	P025	–	O	General-purpose I/O port (3V pin)
51	P026	–	O	General-purpose I/O port (3V pin)
	A00	–		External bus · Address bit0 output pin
54	P027	–	O	General-purpose I/O port (3V pin)
	A01	–		External bus · Address bit1 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
55	P030	–	O	General-purpose I/O port (3V pin)
	A02	–		External bus · Address bit2 output pin
56	P031	–	O	General-purpose I/O port (3V pin)
	A03	–		External bus · Address bit3 output pin
57	P032	–	O	General-purpose I/O port (3V pin)
	A04	–		External bus · Address bit4 output pin
58	P033	–	O	General-purpose I/O port (3V pin)
	A05	–		External bus · Address bit5 output pin
59	P034	–	O	General-purpose I/O port (3V pin)
	A06	–		External bus · Address bit6 output pin
60	P035	–	O	General-purpose I/O port (3V pin)
	A07	–		External bus · Address bit7 output pin
61	P036	–	O	General-purpose I/O port (3V pin)
	A08	–		External bus · Address bit8 output pin
62	P037	–	O	General-purpose I/O port (3V pin)
	A09	–		External bus · Address bit9 output pin
	QSPI_SIO0	–		HS_SPI SDATA0 I/O pin(CY91F59A/B only)
63	P040	–	O	General-purpose I/O port (3V pin)
	A10	–		External bus · Address bit10 output pin
	QSPI_SIO1	–		HS_SPI SDATA1 I/O pin(CY91F59A/B only)
64	P041	–	O	General-purpose I/O port (3V pin)
	A11	–		External bus · Address bit11 output pin
	QSPI_SIO2	–		HS_SPI SDATA2 I/O pin(CY91F59A/B only)
65	P042	–	O	General-purpose I/O port (3V pin)
	A12	–		External bus · Address bit12 output pin
	QSPI_SIO3	–		HS_SPI SDATA3 I/O pin(CY91F59A/B only)
66	P043	–	O	General-purpose I/O port (3V pin)
	A13	–		External bus · Address bit13 output pin
	QSPI_CS0	–		HS_SPI SSEL0 Output pin(CY91F59A/B only)
67	P044	–	O	General-purpose I/O port (3V pin)
	A14	–		External bus · Address bit14 output pin
	QSPI_CS1	–		HS_SPI SSEL1 Output pin(CY91F59A/B only)
68	P045	–	O	General-purpose I/O port (3V pin)
	A15	–		External bus · Address bit15 output pin
	QSPI_CS2	–		HS_SPI SSEL2 Output pin(CY91F59A/B only)
69	P046	–	O	General-purpose I/O port (3V pin)
	A16	–		External bus · Address bit16 output pin
	QSPI_CS3	–		HS_SPI SSEL3 Output pin(CY91F59A/B only)
70	P047	–	O	General-purpose I/O port (3V pin)
	A17	–		External bus · Address bit17 output pin
	QSPI_CLK	–		HS_SPI SCLK Output pin(CY91F59A/B only)
74	P050	–	O	General-purpose I/O port (3V pin)
	A18	–		External bus · Address bit18 output pin
75	P051	–	O	General-purpose I/O port(3V pin)
	A19	–		External bus · Address bit19 output pin
76	P052	–	O	General-purpose I/O port(3V pin)
	A20	–		External bus · Address bit20 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
77	P053	–	O	General-purpose I/O port(3V pin)
	A21	–		External bus · Address bit21 output pin
	SPI_DO	–		SPI data output pin
78	P054	–	O	General-purpose I/O port (3V pin)
	A22	–		External bus · Address bit22 output pin
	SPI_DI	–		SPI data input pin
79	P055	–	O	General-purpose I/O port (3V pin)
	A23	–		External bus · Address bit23 output pin
	SPI_SCK	–		SPI clock output pin
80	P056	–	O	General-purpose I/O port (3V pin)
	A24	–		External bus · Address bit24 output pin
	SPI_XCS	–		SPI chip select output pin
81	P057	–	O	General-purpose I/O port (3V pin)
	RDY	–		External bus · Wait input pin
127	P060	–	E	General-purpose I/O port
	PWM1P0	–		SMC ch.0 output pin
	AN8	–		ADC Analog 8 input pin
	SIN10	–		Multi-function serial ch.10 serial data input pin(CY91F59A/B only)
128	P061	–	E	General-purpose I/O port
	PWM1M0	–		SMC ch.0 output pin
	AN9	–		ADC Analog 9 input pin
	SOT10	–		Multi-function serial ch.10 serial data output pin(CY91F59A/B only)
129	P062	–	E	General-purpose I/O port
	PWM2P0	–		SMC ch.0 output pin
	AN10	–		ADC Analog 10 input pin
	UDCZIN1	–		Up/down counter ch.1 ZIN input pin(CY91F59A/B only)
	SCK10	–		Multi-function serial ch.10 clock I/O pin(CY91F59A/B only)
130	P063	–	E	General-purpose I/O port
	PWM2M0	–		SMC ch.0 output pin
	AN11	–		ADC Analog 11 input pin
	UDCBIN1	–		Up/down counter ch.1 BIN input pin(CY91F59A/B only)
131	P064	–	E	General-purpose I/O port
	PWM1P1	–		SMC ch.1 output pin
	AN12	–		ADC Analog 12 input pin
	UDCAIN1	–		Up/down counter ch.1 AIN input pin(CY91F59A/B only)
132	P065	–	E	General-purpose I/O port
	PWM1M1	–		SMC ch.1 output pin
	AN13	–		ADC Analog 13 input pin
	UDCZIN0	–		Up/down counter ch.0 ZIN input pin(CY91F59A/B only)
133	P066	–	E	General-purpose I/O port
	PWM2P1	–		SMC ch.1 output pin
	AN14	–		ADC Analog 14 input pin
	UDCBIN0	–		Up/down counter ch.0 BIN input pin(CY91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
134	P067	–	E	General-purpose I/O port
	PWM2M1	–		SMC ch.1 output pin
	AN15	–		ADC Analog 15 input pin
	UDCAIN0	–		Up/down counter ch.0 AIN input pin (CY91F59A/B only)
	SIN9	–		Multi-function serial ch.9 serial data input pin(CY91F59A/B only)
137	P070	–	E	General-purpose I/O port
	PWM1P2	–		SMC ch.2 output pin
	AN16	–		ADC Analog 16 input pin
	SOT9	–		Multi-function serial ch.9 serial data output pin(CY91F59A/B only)
138	P071	–	E	General-purpose I/O port
	PWM1M2	–		SMC ch.2 output pin
	AN17	–		ADC Analog 17 input pin
	SCK9	–		Multi-function serial ch.9 clock I/O pin(CY91F59A/B only)
139	P072	–	E	General-purpose I/O port
	PWM2P2	–		SMC ch.2 output pin
	AN18	–		ADC Analog 18 input pin
	SIN8	–		Multi-function serial ch.8 serial data input pin(CY91F59A/B only)
	ICU11	–		Input capture ch.11 input pin(CY91F59A/B only)
140	P073	–	E	General-purpose I/O port
	PWM2M2	–		SMC ch.2 output pin
	AN19	–		ADC Analog 19 input pin
	SOT8	–		Multi-function serial ch.8 serial data output pin(CY91F59A/B only)
	ICU10	–		Input capture ch.10 input pin(CY91F59A/B only)
141	P074	–	E	General-purpose I/O port
	PWM1P3	–		SMC ch.3 output pin
	AN20	–		ADC Analog 20 input pin
	PPG12_1	–		PPG ch.12 output pin (1)
	SCK8	–		Multi-function serial ch.8 clock I/O pin(CY91F59A/B only)
	ICU9	–		Input capture ch.9 input pin(CY91F59A/B only)
142	P075	–	E	General-purpose I/O port
	PWM1M3	–		SMC ch.3 output pin
	AN21	–		ADC Analog 21 input pin
	SIN7_1	–		LIN-UART ch.7 serial data input pin
	PPG13_1	–		PPG ch.13 output pin (1)
	ICU8	–		Input capture ch.8 input pin(CY91F59A/B only)
143	P076	–	E	General-purpose I/O port
	PWM2P3	–		SMC ch.3 output pin
	AN22	–		ADC Analog 22 input pin
	SOT7_1	–		LIN-UART ch.7 serial data output pin
	PPG14_1	–		PPG ch.14 output pin (1)
	ICU7	–		Input capture ch.7 input pin(CY91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
144	P077	–	E	General-purpose I/O port
	PWM2M3	–		SMC ch.3 output pin
	AN23	–		ADC Analog 23 input pin
	SCK7_1	–		LIN-UART ch.7 clock I/O pin
	PPG15_1	–		PPG ch.15 output pin (1)
	ICU6	–		Input capture ch.6 input pin(CY91F59A/B only)
147	P080	–	E	General-purpose I/O port
	PWM1P4	–		SMC ch.4 output pin
	AN24	–		ADC Analog 24 input pin
	SIN6	–		LIN-UART ch.6 serial data input pin
	PPG16	–		PPG ch.16 output pin
	UDCAIN0_1	–		Up/down counter ch.0 AIN input pin (1) (CY91F59A/B only)
148	P081	–	E	General-purpose I/O port
	PWM1M4	–		SMC ch.4 output pin
	AN25	–		ADC Analog 25 input pin
	SOT6	–		LIN-UART ch.6 serial data output pin
	PPG17	–		PPG ch.17 output pin
	UDCBIN0_1	–		Up/down counter ch.0 BIN input pin (1) (CY91F59A/B only)
149	P082	–	E	General-purpose I/O port
	PWM2P4	–		SMC ch.4 output pin
	AN26	–		ADC Analog 26 input pin
	SCK6	–		LIN-UART ch.6 clock I/O pin
	PPG18	–		PPG ch.18 output pin
	UDCZIN0_1	–		Up/down counter ch.0 ZIN input pin (1) (CY91F59A/B only)
150	P083	–	E	General-purpose I/O port
	PWM2M4	–		SMC ch.4 output pin
	AN27	–		ADC Analog 27 input pin
	ICU0_2	–		Input capture ch.0 input pin (2)
	PPG19	–		PPG ch.19 output pin
	UDCZIN2	–		Up/down counter ch.2 ZIN input pin(CY91F59A/B only)
151	P084	–	E	General-purpose I/O port
	PWM1P5	–		SMC ch.5 output pin
	AN28	–		ADC Analog 28 input pin
	ICU1_2	–		Input capture ch.1 input pin (2)
	PPG20	–		PPG ch.20 output pin
	UDCBIN2	–		Up/down counter ch.2 BIN input pin(CY91F59A/B only)
152	P085	–	E	General-purpose I/O port
	PWM1M5	–		SMC ch.5 output pin
	AN29	–		ADC Analog 29 input pin
	ICU2_2	–		Input capture ch.2 input pin (2)
	PPG21	–		PPG ch.21 output pin
	UDCAIN2	–		Up/down counter ch.2 AIN input pin(CY91F59A/B only)
153	P086	–	E	General-purpose I/O port
	PWM2P5	–		SMC ch.5 output pin
	AN30	–		ADC Analog 30 input pin
	ICU3_2	–		Input capture ch.3 input pin (2)
	PPG22	–		PPG ch.22 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
154	P087	–	E	General-purpose I/O port
	PWM2M5	–		SMC ch.5 output pin
	AN31	–		ADC Analog 31 input pin
	ICU4_2	–		Input capture ch.4 input pin (2)
	PPG23	–		PPG ch.23 output pin
157	P090	–	A	General-purpose I/O port
	ADTG	–		A/D convertor external trigger input pin
	PPG0_2	–		PPG ch.0 output pin (2)
	TIN7_1	–		Reload timer ch.7 event input pin (1) (CY91F59A/B only)
98	P091	–	C	General-purpose I/O port
	SGA0	–		Sound generator ch.0 SGA output pin
	SIN2	–		LIN-UART ch.2 serial data input pin
	INT12	–		INT12 External interrupt input pin
	TOT2_1	–		Reload timer ch.2 output pin (1)
	ICU2_1	–		Input capture ch.2 input pin (1)
	PPG6_1	–		PPG ch.6 output pin (1)
99	P092	–	C	General-purpose I/O port
	SGO0	–		Sound generator ch.0 SGO output pin
	SCK2	–		LIN-UART ch.2 clock I/O pin
	INT13	–		INT13 External interrupt input pin
	TOT3_1	–		Reload timer ch.3 output pin (1)
	ICU0_1	–		Input capture ch.0 input pin (1)
	PPG7_1	–		PPG ch.7 output pin (1)
100	P093	–	C	General-purpose I/O port
	SGA1	–		Sound generator ch.1 SGA output pin
	SOT2	–		LIN-UART ch.2 serial data output pin
	INT14	–		INT14 External interrupt input pin
	ICU3_1	–		Input capture ch.3 input pin (1)
	PPG8_1	–		PPG ch.8 output pin (1)
	TIN8_1	–		Reload timer ch.8 event input pin (1) (CY91F59A/B only)
160	P094	–	C	General-purpose I/O port
	SGO1	–		Sound generator ch.1 SGO output pin
	SIN3	–		LIN-UART ch.3 serial data input pin
	INT15	–		INT15 External interrupt input pin
	ICU1_1	–		Input capture ch.1 input pin (1)
	PPG9_1	–		PPG ch.9 output pin (1)
	TIN9_1	–		Reload timer ch.9 event input pin (1) (CY91F59A/B only)
106	P095	–	A	General-purpose I/O port
	TX0	–		CAN transmission data0 output pin
	PPG10_1	–		PPG ch.10 output pin (1)
107	P096	–	A	General-purpose I/O port
	RX0	–		CAN reception data0 input pin
	INT9	–		INT9 External interrupt input pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
161	P097	–	C	General-purpose I/O port
	WOT	–		RTC overflow output pin
	SOT3	–		LIN-UART ch.3 serial data output pin
	INT8	–		INT8 External interrupt input pin
	TIN0	–		Reload timer ch.0 event input pin
	ICU4_1	–		Input capture ch.4 input pin (1)
	PPG0_1	–		PPG ch.0 output pin (1)
114	P100	–	C	General-purpose I/O port
	SIN4_1	–		LIN-UART ch.4 serial data input pin (1)
	AN0	–		ADC Analog 0 input pin
	TIN0_1	–		Reload timer ch.0 event input pin (1)
	PPG8	–		PPG ch.8 output pin
115	P101	–	C	General-purpose I/O port
	SOT4_1	–		LIN-UART ch.4 serial data output pin (1)
	AN1	–		ADC Analog 1 input pin
	TIN1_1	–		Reload timer ch.1 event input pin (1)
	PPG9	–		PPG ch.9 output pin
116	P102	–	C	General-purpose I/O port
	SCK4_1	–		LIN-UART ch.4 clock I/O pin (1)
	AN2	–		ADC Analog 2 input pin
	TIN2_1	–		Reload timer ch.2 event input pin (1)
	PPG10	–		PPG ch.10 output pin
	ICU6_1	–		Input capture ch.6 input pin (1) (CY91F59A/B only)
117	P103	–	C	General-purpose I/O port
	SIN5_1	–		LIN-UART ch.5 serial data input pin (1)
	AN3	–		ADC Analog 3 input pin
	TIN3_1	–		Reload timer ch.3 event input pin (1)
	PPG1_1	–		PPG ch.1 output pin (1)
	ICU7_1	–		Input capture ch.7 input pin (1) (CY91F59A/B only)
118	P104	–	C	General-purpose I/O port
	SOT5_1	–		LIN-UART ch.5 serial data output pin (1)
	AN4	–		ADC Analog 4 input pin
	TOT0_1	–		Reload timer ch.0 output pin (1)
	PPG2_1	–		PPG ch.2 output pin (1)
	ICU8_1	–		Input capture ch.8 input pin (1) (CY91F59A/B only)
119	P105	–	C	General-purpose I/O port
	SCK5_1	–		LIN-UART ch.5 clock I/O pin (1)
	AN5	–		ADC Analog 5 input pin
	TOT1_1	–		Reload timer ch.1 output pin (1)
	PPG3_1	–		PPG ch.3 output pin (1)
	ICU9_1	–		Input capture ch.9 input pin (1) (CY91F59A/B only)
120	P106	–	C	General-purpose I/O port
	SGA4_1	–		Sound generator ch.4 SGA output pin
	AN6	–		ADC Analog 6 input pin
	PPG4_1	–		PPG ch.4 output pin (1)
	TIN10_1	–		Reload timer ch.10 event input pin (1) (CY91F59A/B only)
	ICU10_1	–		Input capture ch.10 input pin (1) (CY91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
121	P107	–	C	General-purpose I/O port
	SGO4_1	–		Sound generator ch.4 SGO output pin
	AN7	–		ADC Analog 7 input pin
	PPG5_1	–		PPG ch.5 output pin (1)
	TOT7_1	–		Reload timer ch.7 output pin (1) (CY91F59A/B only)
	ICU11_1	–		Input capture ch.11 input pin (1) (CY91F59A/B only)
101	P110	–	C	General-purpose I/O port
	TX1	–		CAN transmission data1 output pin
	PPG1_2	–		PPG ch.1 output pin (2)
	FRCK5	–		Free-run timer 5 clock input pin(CY91F59A/B only)
	TOT8_1	–		Reload timer ch.8 output pin (1) (CY91F59A/B only)
102	P111	–	C	General-purpose I/O port
	RX1	–		CAN reception data 1 input pin
	INT10	–		INT10 External interrupt input pin
	PPG2_2	–		PPG ch.2 output pin (2)
	FRCK6	–		Free-run timer 6 clock input pin(CY91F59A/B only)
	TOT9_1	–		Reload timer ch.9 output pin (1) (CY91F59A/B only)
158	P112	–	C	General-purpose I/O port
	TX2	–		CAN transmission data 2 output pin
	PPG3_2	–		PPG ch.3 output pin (2)
	TOT10_1	–		Reload timer ch.10 output pin (1) (CY91F59A/B only)
159	P113	–	C	General-purpose I/O port
	RX2	–		CAN reception data 2 input pin
	INT11	–		INT11 External interrupt input pin
	PPG4_2	–		PPG ch.4 output pin (2)
	TIN7	–		Reload timer ch.7 event input pin(CY91F59A/B only)
162	P114	–	C	General-purpose I/O port
	SGA2	–		Sound generator ch.2 SGA output pin
	SCK3	–		LIN-UART ch.3 clock I/O pin
	TRG3	–		PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1	–		Reload timer ch.1 event input pin
	ICU5_1	–		Input capture ch.5 input pin (1)
	FRCK7	–		Free-run timer 7 clock input pin(CY91F59A/B only)
163	P115	–	C	General-purpose I/O port
	SGO2	–		Sound generator ch.2 SGO output pin
	SIN4	–		LIN-UART ch.4 serial data input pin
	TIN2	–		Reload timer ch.2 event input pin
	FRCK4	–		Free-run timer 4 clock input pin(CY91F59A/B only)
164	P116	–	C	General-purpose I/O port
	SGA3	–		Sound generator ch.3 SGA output pin
	SOT4	–		LIN-UART ch.4 serial data output pin
	TIN3	–		Reload timer ch.3 event input pin
	FRCK3	–		Free-run timer 3 clock input pin(CY91F59A/B only)
165	P117	–	C	General-purpose I/O port
	SGO3	–		Sound generator ch.3 SGO output pin
	SCK4	–		LIN-UART ch.4 clock I/O pin
	TRG4	–		PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0	–		Reload timer ch.0 output pin
	FRCK2	–		Free-run timer 2 clock input pin(CY91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
166	P120	–	C	General-purpose I/O port
	FRCK1	–		Free-run timer 1 clock input pin
	SIN5	–		LIN-UART ch.5 serial data input pin
	INT6	–		INT6 External interrupt input pin
	TOT1	–		Reload timer ch.1 output pin
	PPG5_2	–		PPG ch.5 output pin (2)
167	P121	–	C	General-purpose I/O port
	FRCK0	–		Free-run timer 0 clock input pin
	SOT5	–		LIN-UART ch.5 serial data output pin
	INT7	–		INT7 External interrupt input pin
	TOT2	–		Reload timer ch.2 output pin
	PPG6_2	–		PPG ch.6 output pin (2)
168	P122	–	C	General-purpose I/O port
	OCU0	–		Output compare ch.0 output pin
	SCK5	–		LIN-UART ch.5 clock I/O pin
	TOT3	–		Reload timer ch.3 output pin
	PPG7_2	–		PPG ch.7 output pin (2)
108	P123	–	A	General-purpose I/O port
	OCU1	–		Output compare ch.1 output pin
	PPG8_2	–		PPG ch.8 output pin (2)
	TIN8	–		Reload timer ch.8 event input pin(CY91F59A/B only)
	SIN11	–		Multi-function serial ch.11 serial data input pin(CY91F59A/B only)
109	P124	–	A	General-purpose I/O port
	OCU2	–		Output compare ch.2 output pin
	ICU5_2	–		Input capture ch.5 input pin (2)
	PPG9_2	–		PPG ch.9 output pin (2)
	TIN9	–		Reload timer ch.9 event input pin(CY91F59A/B only)
	SOT11	–		Multi-function serial ch.11 serial data output pin(CY91F59A/B only)
110	P125	–	A	General-purpose I/O port
	OCU3	–		Output compare ch.3 output pin
	ICU0	–		Input capture ch.0 input pin
	PPG10_2	–		PPG ch.10 output pin (2)
	TIN10	–		Reload timer ch.10 event input pin(CY91F59A/B only)
	SCK11	–		Multi-function serial ch.11 clock I/O pin(CY91F59A/B only)
90	P126	–	A	General-purpose I/O port
	TRG0	–		PPG trigger 0 input pin (ch.0 to ch.3)
	SIN0	–		Multi-function serial ch.0 serial data input pin
	INT1	–		INT1 External interrupt input pin
91	P127	–	K	General-purpose I/O port
	SOT0	–		Multi-function serial ch.0 serial data output pin / I^2C ch.0 serial data I/O pin
92	P130	–	K	General-purpose I/O port
	SCK0	–		Multi-function serial ch.0 clock I/O pin / I^2C ch.0 clock I/O pin
	INT0	–		INT0 External interrupt input pin
	ICU1	–		Input capture ch.1 input pin
	TIOA0	–		Base timer TIOA0 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
93	P131	–	A	General-purpose I/O port
	TRG1	–		PPG trigger 1 input pin (ch.4 to ch.7)
	SIN1	–		Multi-function serial ch.1 serial data input pin
	INT4	–		INT4 External interrupt input pin
	ICU2	–		Input capture ch.2 input pin
	TIOA1	–		Base timer TIOA1 I/O pin
	TOT7	–		Reload timer ch.7 output pin(CY91F59A/B only)
94	P132	–	K	General-purpose I/O port
	SOT1	–		Multi-function serial ch.1 serial data output pin / I^2C ch.1 serial data I/O pin
	INT2	–		INT2 External interrupt input pin
	ICU3	–		Input capture ch.3 input pin
	TIOB0	–		Base timer TIOB0 input pin
	TOT8	–		Reload timer ch.8 output pin(CY91F59A/B only)
95	P133	–	K	General-purpose I/O port
	TRG5	–		PPG trigger 5 input pin (ch.20 to ch.23)
	PPG11_1	–		PPG ch.11 output pin (1)
	SCK1	–		Multi-function serial ch.1 clock I/O pin / I^2C ch.1 clock I/O pin
	INT3	–		INT3 External interrupt input pin
	ICU4	–		Input capture ch.4 input pin
	TIOB1	–		Base timer TIOB1 input pin
	TOT9	–		Reload timer ch.9 output pin(CY91F59A/B only)
96	P134	–	A	General-purpose I/O port
	TRG2	–		PPG trigger 2 input pin (ch.8 to ch.11)
	PPG1_3	–		PPG ch.1 output pin (3)
	INT5	–		INT5 External interrupt input pin
	ICU5	–		Input capture ch.5 input pin
	TOT10	–		Reload timer ch.10 output pin(CY91F59A/B only)
103	DEBUGIF	–	G	DEBUG I/F pin
176	PA2	–	O	General-purpose I/O port (3V pin)
	RIN2	–		Capture R2 input pin (RGB mode)
	VIN0	–		Capture VIN0 input pin (656 mode)
177	PA3	–	O	General-purpose I/O port (3V pin)
	RIN3	–		Capture R3 input pin (RGB mode)
	VIN1	–		Capture VIN1 input pin (656 mode)
178	PA4	–	O	General-purpose I/O port (3V pin)
	RIN4	–		Capture R4 input pin (RGB mode)
	VIN2	–		Capture VIN2 input pin (656 mode)
179	PA5	–	O	General-purpose I/O port (3V pin)
	RIN5	–		Capture R5 input pin (RGB mode)
	VIN3	–		Capture VIN3 input pin (656 mode)
180	PA6	–	O	General-purpose I/O port (3V pin)
	RIN6	–		Capture R6 input pin (RGB mode)
	VIN4	–		Capture VIN4 input pin (656 mode)
181	PA7	–	O	General-purpose I/O port (3V pin)
	RIN7	–		Capture R7 input pin (RGB mode)
	VIN5	–		Capture VIN5 input pin (656 mode)

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
182	PB2	–	O	General-purpose I/O port (3V pin)
	GIN2	–		Capture G2 input pin (RGB mode)
	VIN6	–		Capture VIN6 input pin (656 mode)
183	PB3	–	O	General-purpose I/O port (3V pin)
	GIN3	–		Capture G3 input pin (RGB mode)
	VIN7	–		Capture VIN7 input pin (656 mode)
184	PB4	–	O	General-purpose I/O port (3V pin)
	GIN4	–		Capture G4 input pin (RGB mode)
185	PB5	–	O	General-purpose I/O port (3V pin)
	GIN5	–		Capture G5 input pin (RGB mode)
186	PB6	–	O	General-purpose I/O port (3V pin)
	GIN6	–		Capture G6 input pin (RGB mode)
187	PB7	–	O	General-purpose I/O port (3V pin)
	GIN7	–		Capture G7 input pin (RGB mode)
190	PC2	–	O	General-purpose I/O port (3V pin)
	BIN2	–		Capture B2 input pin (RGB mode)
191	PC3	–	O	General-purpose I/O port (3V pin)
	BIN3	–		Capture B3 input pin (RGB mode)
192	PC4	–	O	General-purpose I/O port (3V pin)
	BIN4	–		Capture B4 input pin (RGB mode)
193	PC5	–	O	General-purpose I/O port (3V pin)
	BIN5	–		Capture B5 input pin (RGB mode)
194	PC6	–	O	General-purpose I/O port (3V pin)
	BIN6	–		Capture B6 input pin (RGB mode)
195	PC7	–	O	General-purpose I/O port (3V pin)
	BIN7	–		Capture B7 input pin (RGB mode)
2	PD2	–	O	General-purpose I/O port (3V pin)
	ROUT2	–		Display digital R2 output pin
3	PD3	–	O	General-purpose I/O port (3V pin)
	ROUT3	–		Display digital R3 output pin
4	PD4	–	O	General-purpose I/O port (3V pin)
	ROUT4	–		Display digital R4 output pin
5	PD5	–	O	General-purpose I/O port (3V pin)
	ROUT5	–		Display digital R5 output pin
6	PD6	–	O	General-purpose I/O port (3V pin)
	ROUT6	–		Display digital R6 output pin
7	PD7	–	O	General-purpose I/O port (3V pin)
	ROUT7	–		Display digital R7 output pin
8	PE2	–	O	General-purpose I/O port (3V pin)
	GOUT2	–		Display digital G2 output pin
9	PE3	–	O	General-purpose I/O port (3V pin)
	GOUT3	–		Display digital G3 output pin
10	PE4	–	O	General-purpose I/O port (3V pin)
	GOUT4	–		Display digital G4 output pin
11	PE5	–	O	General-purpose I/O port (3V pin)
	GOUT5	–		Display digital G5 output pin
12	PE6	–	O	General-purpose I/O port (3V pin)
	GOUT6	–		Display digital G6 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
13	PE7	–	O	General-purpose I/O port (3V pin)
	GOUT7	–		Display digital G7 output pin
14	PF2	–	O	General-purpose I/O port (3V pin)
	BOUT2	–		Display digital B2 output pin
15	PF3	–	O	General-purpose I/O port (3V pin)
	BOUT3	–		Display digital B3 output pin
16	PF4	–	O	General-purpose I/O port (3V pin)
	BOUT4	–		Display digital B4 output pin
17	PF5	–	O	General-purpose I/O port (3V pin)
	BOUT5	–		Display digital B5 output pin
21	PF6	–	O	General-purpose I/O port (3V pin)
	BOUT6	–		Display digital B6 output pin
22	PF7	–	O	General-purpose I/O port(3V pin)
	BOUT7	–		Display digital B7 output pin
200	PG0	–	O	General-purpose I/O port (3V pin)
	DCKIN	–		Display reference clock input pin (for External sync)
	CMDTRG	–		GDC command trigger input pin
197	PG1	–	O	General-purpose I/O port (3V pin)
	VSIN	P		Capture vertical sync signal input pin
198	PG2	–	O	General-purpose I/O port (3V pin)
	HSIN	P		Capture horizontal sync signal input pin
199	PG3	–	O	General-purpose I/O port (3V pin)
	CSOUT	–		Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin
23	PG4	–	O	General-purpose I/O port (3V pin)
	DCKOUT	–		Display reference clock output pin (for Internal sync)
24	PG5	–	O	General-purpose I/O port (3V pin)
	VSYNC	–		Display vertical sync signal output pin (for Internal sync)/Display vertical sync signal input pin (for External sync)
25	PG6	–	O	General-purpose I/O port (3V pin)
	HSYNC	–		Display horizontal sync signal output pin (for Internal sync)/Display horizontal sync signal input pin (for External sync)
26	PG7	–	O	General-purpose I/O port (3V pin)
	DEOUT	P		Display enable display period output pin
196	PH3	–	O	General-purpose I/O port (3V pin)
	CCLK	–		For capture, capture clock input pin
204	REFOUT	–	T	Clamp level output pin
203	AVR3	–	S	"L" side reference voltage for NTSC A/D converter pin
205	VIN	–	S	NTSC signal input pin
111	AVCC5	–	–	AD convertor analog power supply pin
201, 207	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
112	AVRH5	–	–	AD convertor upper limit reference voltage pin
113	AVSS5/ AVRL5	–	–	AD convertor GND/ AD convertor lower limit reference voltage pin
202, 206	AVSS3	–	–	NTSC AD convertor GND pin
124	C_1	–	–	Built-in regulator capacitor connected pin 1
73	C_2	–	–	Built-in regulator capacitor connected pin 2
20	C_3	–	–	Built-in regulator capacitor connected pin 3

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
126, 136, 146, 156	DVCC	–	–	SMC large current port power supply pin
125, 135, 145, 155	DVSS	–	–	SMC large current port GND pin
89, 105, 122, 173	VCC5	–	–	+5.0V power supply pin
1, 18, 37, 53, 71, 175, 189	VCC3	–	–	+3.3V power supply pin
19, 36, 52, 72, 82, 88, 104, 123, 170, 174, 188, 208	VSS	–	–	GND pin

[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

3.2 CY91F59A/B (BGA320)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
1	VSS	–	–	GND pin
2	VSS	–	–	GND pin
3	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
4	VIN	–	S	NTSC signal input pin
5	REFOUT	–	T	Clamp level output pin
6	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
7	BIN5	–	O	Capture B5 input pin (RGB mode)
	PC5			General-purpose I/O port (3V pin)
8	BIN2	–	O	Capture B2 input pin (RGB mode)
	PC2			General-purpose I/O port (3V pin)
9	GIN5	–	O	Capture G5 input pin (RGB mode)
	PB5			General-purpose I/O port (3V pin)
10	GIN2	–	O	Capture G2 input pin (RGB mode)
	VIN6			Capture VIN6 input pin (656 mode)
	PB2			General-purpose I/O port (3V pin)
11	RIN5	–	O	Capture R5 input pin (RGB mode)
	VIN3			Capture VIN3 input pin (656 mode)
	PA5			General-purpose I/O port (3V pin)
12	RIN2	–	O	Capture R2 input pin (RGB mode)
	VIN0			Capture VIN0 input pin (656 mode)
	PA2			General-purpose I/O port (3V pin)
13	VSS	–	–	GND pin
14	P136	–	A	General-purpose I/O port (Single clock product)
	(X1A)		N	Sub clock oscillation output pin (Dual clock product)
15	P137	–	A	General-purpose I/O port (Single clock product)
	(X0A)	–	N	Sub clock oscillation input pin (Dual clock product)
16	VSS	–	–	GND pin
17	P094	–	C	General-purpose I/O port
	ICU1_1			Input capture ch.1 input pin (1)
	INT15			INT15 External interrupt input pin
	SIN3			LIN-UART ch.3 serial data input pin
	PPG9_1			PPG ch.9 output pin (1)
	TIN9_1			Reload timer ch.9 event input pin (1)
	SGO1			Sound generator ch.1 SGO output pin
18	ADTG	–	A	A/D convertor external trigger input pin
	P090			General-purpose I/O port
	PPG0_2			PPG ch.0 output pin (2)
	TIN7_1			Reload timer ch.7 event input pin (1)
19	TCK	–	U	Test Clock (JTAG Boundary Scan Test)
20	VSS	–	–	GND pin
21	TMS	–	U	Test Mode State (JTAG Boundary Scan Test)
22	TDO	–	W	Test Data Out (JTAG Boundary Scan Test)
23	AN31	–	E	ADC Analog 31 input pin
	P087			General-purpose I/O port
	ICU4_2			Input capture ch.4 input pin (2)
	PPG23			PPG ch.23 output pin
23	PWM2M5	–	E	SMC ch.5 output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
24	AN28	–	E	ADC Analog 28 input pin
	P084			General-purpose I/O port
	ICU1_2			Input capture ch.1 input pin (2)
	PPG20			PPG ch.20 output pin
	PWM1P5			SMC ch.5 output pin
	UDCBIN2			Up/down counter ch.2 BIN input pin
25	AN25	–	E	ADC Analog 25 input pin
	P081			General-purpose I/O port
	SOT6			LIN-UART ch.6 serial data output pin
	PPG17			PPG ch.17 output pin
	PWM1M4			SMC ch.4 output pin
	UDCBIN0_1			Up/down counter ch.0 BIN input pin (1)
26	AN22	–	E	ADC Analog 22 input pin
	P076			General-purpose I/O port
	ICU7			Input capture ch.7 input pin
	SOT7_1			LIN-UART ch.7 serial data output pin
	PPG14_1			PPG ch.14 output pin (1)
	PWM2P3			SMC ch.3 output pin
27	AN19	–	E	ADC Analog 19 input pin
	P073			General-purpose I/O port
	ICU10			Input capture ch.10 input pin
	SOT8			Multi-function serial ch.8 serial data output pin
	PWM2M2			SMC ch.2 output pin
28	AN16	–	E	ADC Analog 16 input pin
	P070			General-purpose I/O port
	SOT9			Multi-function serial ch.9 serial data output pin
	PWM1P2			SMC ch.2 output pin
29	AN13	–	E	ADC Analog 13 input pin
	P065			General-purpose I/O port
	PWM1M1			SMC ch.1 output pin
	UDCZIN0			Up/down counter ch.0 ZIN input pin
30	AN10	–	E	ADC Analog 10 input pin
	P062			General-purpose I/O port
	SCK10			Multi-function serial ch.10 clock I/O pin
	PWM2P0			SMC ch.0 output pin
	UDCZIN1			Up/down counter ch.1 ZIN input pin
31	VSS	–	–	GND pin
32	C_1	–	–	Built-in regulator capacitor connected pin 1
33	AN5	–	C	ADC Analog 5 input pin
	P105			General-purpose I/O port
	ICU9_1			Input capture ch.9 input pin (1)
	SCK5_1			LIN-UART ch.5 clock I/O pin (1)
	PPG3_1			PPG ch.3 output pin (1)
	TOT1_1			Reload timer ch.1 output pin (1)
34	AVSS5	–	–	A/D convertor GND
	AVRL5			A/D convertor lower limit reference voltage pin
35	AVRH5	–	–	A/D convertor upper limit reference voltage pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
36	P125	–	A	General-purpose I/O port
	ICU0			Input capture ch.0 input pin
	SCK11			Multi-function serial ch.11 clock I/O pin
	OCU3			Output compare ch.3 output pin
	PPG10_2			PPG ch.10 output pin (2)
	TIN10			Reload timer ch.10 event input pin
37	P123	–	A	General-purpose I/O port
	SIN11			Multi-function serial ch.11 serial data input pin
	OCU1			Output compare ch.1 output pin
	PPG8_2			PPG ch.8 output pin (2)
	TIN8			Reload timer ch.8 event input pin
38	VSS	–	–	GND pin
39	VSS	–	–	GND pin
40	MD3	–	F3	Mode pin 3
41	DEBUGIF	–	G	DEBUG I/F pin
42	TX1	–	C	CAN transmission data1 output pin
	FRCK5			Free-run timer 5 clock input pin
	P110			General-purpose I/O port
	PPG1_2			PPG ch.1 output pin (2)
	TOT8_1			Reload timer ch.8 output pin (1)
43	P091	–	C	General-purpose I/O port
	ICU2_1			Input capture ch.2 input pin (1)
	INT12			INT12 External interrupt input pin
	SIN2			LIN-UART ch.2 serial data input pin
	PPG6_1			PPG ch.6 output pin (1)
	TOT2_1			Reload timer ch.2 output pin (1)
	SGA0			Sound generator ch.0 SGA output pin
44	VSS	–	–	GND pin
45	X0	–	L	Main clock oscillation input pin
46	X1	–	L	Main clock oscillation output pin
47	VSS	–	–	GND pin
48	A23	–	O	External bus · Address bit23 output pin
	P055			General-purpose I/O port (3V pin)
	SPI_SCK			SPI clock output pin
49	A22	–	O	External bus · Address bit22 output pin
	P054			General-purpose I/O port (3V pin)
	SPI_DI			SPI data input pin
50	C_2	–	–	Built-in regulator capacitor connected pin 2

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
51	A17	–	O	External bus · Address bit17 output pin
	P047			General-purpose I/O port (3V pin)
	QSPI_CLK			HS_SPI SCLK Output pin
52	A15	–	O	External bus · Address bit15 output pin
	P045			General-purpose I/O port (3V pin)
	QSPI_CS2			HS_SPI SSEL2 Output pin
53	A12	–	O	External bus · Address bit12 output pin
	P042			General-purpose I/O port (3V pin)
53	QSPI_SIO3	–	O	HS_SPI SDATA3 I/O pin
54	A09	–	O	External bus · Address bit9 output pin
	P037			General-purpose I/O port (3V pin)
	QSPI_SIO0			HS_SPI SDATA0 I/O pin
55	A05	–	O	External bus · Address bit5 output pin
	P033			General-purpose I/O port (3V pin)
56	A02	–	O	External bus · Address bit2 output pin
	P030			General-purpose I/O port (3V pin)
57	VSS	–	–	GND pin
58	VSS	–	–	GND pin
59	VSS	–	–	GND pin
60	P025	–	O	General-purpose I/O port (3V pin)
61	CS1X	–	O	External bus · Chip select 1 output pin
	P022			General-purpose I/O port (3V pin)
62	D15	–	O	External bus · Data bit15 I/O pin
	P017			General-purpose I/O port (3V pin)
63	GOUT1	–	O	Display digital G1 output pin
	D12			External bus · Data bit12 I/O pin
	P014			General-purpose I/O port (3V pin)
64	D8	–	O	External bus · Data bit8 I/O pin
	P010			General-purpose I/O port (3V pin)
65	D7	–	O	External bus · Data bit7 I/O pin
	P007			General-purpose I/O port (3V pin)
	PPG7			PPG ch.7 output pin
	TOT3_2			Reload timer ch.3 output pin (2)
66	D4	–	O	External bus · Data bit4 I/O pin
	P004			General-purpose I/O port (3V pin)
	SOT3_1			LIN-UART ch.3 serial data output pin (1)
	PPG4			PPG ch.4 output pin
	TOT0_2			Reload timer ch.0 output pin (2)
67	D1	–	O	External bus · Data bit1 I/O pin
	P001			General-purpose I/O port (3V pin)
	SOT2_1			LIN-UART ch.2 serial data output pin (1)
	PPG1			PPG ch.1 output pin
	TIN1_2			Reload timer ch.1 event input pin (2)
68	DCKOUT	–	O	Display reference clock output pin (for Internal sync)
	PG4			General-purpose I/O port (3V pin)
69	VSS	–	–	GND pin
70	C_3	–	–	Built-in regulator capacitor connected pin 3
71	BOUT4	–	O	Display digital B4 output pin
	PF4			General-purpose I/O port (3V pin)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
72	GOUT7	–	O	Display digital G7 output pin
	PE7			General-purpose I/O port (3V pin)
73	GOUT4	–	O	Display digital G4 output pin
	PE4			General-purpose I/O port (3V pin)
74	ROUT7	–	O	Display digital R7 output pin
	PD7			General-purpose I/O port (3V pin)
75	ROUT4	–	O	Display digital R4 output pin
	PD4			General-purpose I/O port (3V pin)
76	VSS	–	–	GND pin
77	VSS	–	–	GND pin
78	VSS	–	–	GND pin
79	AVSS3	–	–	NTSC AD convertor GND pin
80	AVR3	–	S	"L" side reference voltage for NTSC A/D converter pin
81	AVSS3	–	–	NTSC AD convertor GND pin
82	BIN6	–	O	Capture B6 input pin (RGB mode)
	PC6			General-purpose I/O port (3V pin)
83	BIN3	–	O	Capture B3 input pin (RGB mode)
	PC3			General-purpose I/O port (3V pin)
84	GIN6	–	O	Capture G6 input pin (RGB mode)
	PB6			General-purpose I/O port (3V pin)
85	GIN3	–	O	Capture G3 input pin (RGB mode)
	VIN7			Capture VIN7 input pin (656 mode)
	PB3			General-purpose I/O port (3V pin)
86	RIN6	–	O	Capture R6 input pin (RGB mode)
	VIN4			Capture VIN4 input pin (656 mode)
	PA6			General-purpose I/O port (3V pin)
87	RIN3	–	O	Capture R3 input pin (RGB mode)
	VIN1			Capture VIN1 input pin (656 mode)
	PA3			General-purpose I/O port (3V pin)
88	P122	–	C	General-purpose I/O port
	SCK5			LIN-UART ch.5 clock I/O pin
	OCU0			Output compare ch.0 output pin
	PPG7_2			PPG ch.7 output pin (2)
	TOT3			Reload timer ch.3 output pin
89	VSS	–	–	GND pin
90	MD2	–	F2	Mode pin 2
91	FRCK7	–	C	Free-run timer 7 clock input pin
	P114			General-purpose I/O port
	ICU5_1			Input capture ch.5 input pin (1)
	SCK3			LIN-UART ch.3 clock I/O pin
	TRG3			PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1			Reload timer ch.1 event input pin
	SGA2			Sound generator ch.2 SGA output pin
92	RX2	–	C	CAN reception data 2 input pin
	P113			General-purpose I/O port
	INT11			INT11 External interrupt input pin
	PPG4_2			PPG ch.4 output pin (2)
	TIN7			Reload timer ch.7 event input pin
93	TDI	–	U	Test Data In (JTAG Boundary Scan Test)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
94	VSS	–	–	GND pin
95	TRST	–	V	Test Reset (JTAG Boundary Scan Test)
96	AN30	–	E	ADC Analog 30 input pin
	P086			General-purpose I/O port
96	ICU3_2	–	E	Input capture ch.3 input pin (2)
	PPG22			PPG ch.22 output pin
	PWM2P5			SMC ch.5 output pin
97	AN27	–	E	ADC Analog 27 input pin
	P083			General-purpose I/O port
	ICU0_2			Input capture ch.0 input pin (2)
	PPG19			PPG ch.19 output pin
	PWM2M4			SMC ch.4 output pin
	UDCZIN2			Up/down counter ch.2 ZIN input pin
98	AN24	–	E	ADC Analog 24 input pin
	P080			General-purpose I/O port
	SIN6			LIN-UART ch.6 serial data input pin
	PPG16			PPG ch.16 output pin
	PWM1P4			SMC ch.4 output pin
	UDCAIN0_1			Up/down counter ch.0 AIN input pin (1)
99	AN21	–	E	ADC Analog 21 input pin
	P075			General-purpose I/O port
	ICU8			Input capture ch.8 input pin
	SIN7_1			LIN-UART ch.7 serial data input pin
	PPG13_1			PPG ch.13 output pin (1)
	PWM1M3			SMC ch.3 output pin
100	AN18	–	E	ADC Analog 18 input pin
	P072			General-purpose I/O port
	ICU11			Input capture ch.11 input pin
	SIN8			Multi-function serial ch.8 serial data input pin
	PWM2P2			SMC ch.2 output pin
101	AN15	–	E	ADC Analog 15 input pin
	P067			General-purpose I/O port
	SIN9			Multi-function serial ch.9 serial data input pin
	PWM2M1			SMC ch.1 output pin
	UDCAIN0			Up/down counter ch.0 AIN input pin
102	AN12	–	E	ADC Analog 12 input pin
	P064			General-purpose I/O port
	PWM1P1			SMC ch.1 output pin
	UDCAIN1			Up/down counter ch.1 AIN input pin
103	AN9	–	E	ADC Analog 9 input pin
	P061			General-purpose I/O port
	SOT10			Multi-function serial ch.10 serial data output pin
	PWM1M0			SMC ch.0 output pin
104	VSS	–	–	GND pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
105	AN7	–	C	ADC Analog 7 input pin
	P107			General-purpose I/O port
	ICU11_1			Input capture ch.11 input pin (1)
	PPG5_1			PPG ch.5 output pin (1)
	TOT7_1			Reload timer ch.7 output pin (1)
	SGO4_1			Sound generator ch.4 SGO output pin
106	AN4	–	C	ADC Analog 4 input pin
106	P104	–	C	General-purpose I/O port
	ICU8_1			Input capture ch.8 input pin (1)
	SOT5_1			LIN-UART ch.5 serial data output pin (1)
	PPG2_1			PPG ch.2 output pin (1)
	TOT0_1			Reload timer ch.0 output pin (1)
107	AN2	–	C	ADC Analog 2 input pin
	P102			General-purpose I/O port
	ICU6_1			Input capture ch.6 input pin (1)
	SCK4_1			LIN-UART ch.4 clock I/O pin (1)
	PPG10			PPG ch.10 output pin
	TIN2_1			Reload timer ch.2 event input pin (1)
108	AVCC5	–	–	A/D convertor analog power supply pin
109	P124	–	A	General-purpose I/O port
	ICU5_2			Input capture ch.5 input pin (2)
	SOT11			Multi-function serial ch.11 serial data output pin
	OCU2			Output compare ch.2 output pin
	PPG9_2			PPG ch.9 output pin (2)
	TIN9			Reload timer ch.9 event input pin
110	RX0	–	A	CAN reception data0 input pin
	P096			General-purpose I/O port
	INT9			INT9 External interrupt input pin
111	VSS	–	–	GND pin
112	RX1	–	C	CAN reception data 1 input pin
	FRCK6			Free-run timer 6 clock input pin
	P111			General-purpose I/O port
	INT10			INT10 External interrupt input pin
	PPG2_2			PPG ch.2 output pin (2)
	TOT9_1			Reload timer ch.9 output pin (1)
113	P093	–	C	General-purpose I/O port
	ICU3_1			Input capture ch.3 input pin (1)
	INT14			INT14 External interrupt input pin
	SOT2			LIN-UART ch.2 serial data output pin
	PPG8_1			PPG ch.8 output pin (1)
	TIN8_1			Reload timer ch.8 event input pin (1)
	SGA1			Sound generator ch.1 SGA output pin
114	NMIX	N	F1	Non-masking interrupt input pin
115	TIOA1	–	A	Base timer TIOA1 I/O pin
	P131			General-purpose I/O port
	ICU2			Input capture ch.2 input pin
	INT4			INT4 External interrupt input pin
	SIN1			Multi-function serial ch.1 serial data input pin
	TRG1			PPG trigger 1 input pin (ch.4 to ch.7)
	TOT7			Reload timer ch.7 output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
116	MD0	–	P	Mode pin 0
117	MD1	–	P	Mode pin 1
118	P126	–	A	General-purpose I/O port
	INT1			INT1 External interrupt input pin
118	SIN0	–	A	Multi-function serial ch.0 serial data input pin
	TRG0			PPG trigger 0 input pin (ch.0 to ch.3)
119	A24	–	O	External bus · Address bit24 output pin
	P056			General-purpose I/O port (3V pin)
	SPI_XCS			SPI chip select output pin
120	A21	–	O	External bus · Address bit21 output pin
	P053			General-purpose I/O port(3V pin)
	SPI_DO			SPI data output pin
121	VSS	–	–	GND pin
122	A16	–	O	External bus · Address bit16 output pin
	P046			General-purpose I/O port (3V pin)
	QSPI_CS3			HS_SPI SSEL3 Output pin
123	A14	–	O	External bus · Address bit14 output pin
	P044			General-purpose I/O port (3V pin)
	QSPI_CS1			HS_SPI SSEL1 Output pin
124	A11	–	O	External bus · Address bit11 output pin
	P041			General-purpose I/O port (3V pin)
	QSPI_SIO2			HS_SPI SDATA2 I/O pin
125	A08	–	O	External bus · Address bit8 output pin
	P036			General-purpose I/O port (3V pin)
126	A04	–	O	External bus · Address bit4 output pin
	P032			General-purpose I/O port (3V pin)
127	A01	–	O	External bus · Address bit1 output pin
	P027			General-purpose I/O port (3V pin)
128	VSS	–	–	GND pin
129	A00	–	O	External bus · Address bit0 output pin
	P026			General-purpose I/O port (3V pin)
130	REX	–	O	External bus · Read enable output pin
	P023			General-purpose I/O port (3V pin)
131	WEX	–	O	External bus · Write enable output pin
	P020			General-purpose I/O port (3V pin)
132	BOUT0	–	O	Display digital B0 output pin
	D13			External bus · Data bit13 I/O pin
	P015			General-purpose I/O port (3V pin)
133	ROUT0	–	O	Display digital R0 output pin
	D9			External bus · Data bit9 I/O pin
	P011			General-purpose I/O port (3V pin)
134	D6	–	O	External bus · Data bit6 I/O pin
	P006			General-purpose I/O port (3V pin)
	PPG6			PPG ch.6 output pin
	TOT2_2			Reload timer ch.2 output pin (2)
135	D3	–	O	External bus · Data bit3 I/O pin
	P003			General-purpose I/O port (3V pin)
	SIN3_1			LIN-UART ch.3 serial data input pin (1)
	PPG3			PPG ch.3 output pin
	TIN3_2			Reload timer ch.3 event input pin (2)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
136	D0	–	O	External bus · Data bit0 I/O pin
136	P000	–	O	General-purpose I/O port (3V pin)
	SIN2_1			LIN-UART ch.2 serial data input pin (1)
	PPG0			PPG ch.0 output pin
	TIN0_2			Reload timer ch.0 event input pin (2)
137	VSYNC	–	O	Display vertical sync signal output pin (for Internal sync)/ Display vertical sync signal input pin (for External sync)
	PG5			General-purpose I/O port (3V pin)
138	BOUT7	–	O	Display digital B7 output pin
	PF7			General-purpose I/O port(3V pin)
139	BOUT5	–	O	Display digital B5 output pin
	PF5			General-purpose I/O port (3V pin)
140	BOUT3	–	O	Display digital B3 output pin
	PF3			General-purpose I/O port (3V pin)
141	GOUT6	–	O	Display digital G6 output pin
	PE6			General-purpose I/O port (3V pin)
142	GOUT3	–	O	Display digital G3 output pin
	PE3			General-purpose I/O port (3V pin)
143	ROUT6	–	O	Display digital R6 output pin
	PD6			General-purpose I/O port (3V pin)
144	ROUT3	–	O	Display digital R3 output pin
	PD3			General-purpose I/O port (3V pin)
145	VSS	–	–	GND pin
146	DCKIN	–	O	Display reference clock input pin (for External sync)
	CMDTRG			GDC command trigger input pin
	PG0			General-purpose I/O port (3V pin)
147	CSOUT	–	O	Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin
	PG3			General-purpose I/O port (3V pin)
148	HSIN	P	O	Capture horizontal sync signal input pin
	PG2	–		General-purpose I/O port (3V pin)
149	BIN7	–	O	Capture B7 input pin (RGB mode)
	PC7			General-purpose I/O port (3V pin)
150	BIN4	–	O	Capture B4 input pin (RGB mode)
	PC4			General-purpose I/O port (3V pin)
151	GIN7	–	O	Capture G7 input pin (RGB mode)
	PB7			General-purpose I/O port (3V pin)
152	GIN4	–	O	Capture G4 input pin (RGB mode)
	PB4			General-purpose I/O port (3V pin)
153	RIN7	–	O	Capture R7 input pin (RGB mode)
	VIN5			Capture VIN5 input pin (656 mode)
	PA7			General-purpose I/O port (3V pin)
154	RIN4	–	O	Capture R4 input pin (RGB mode)
	VIN2			Capture VIN2 input pin (656 mode)
	PA4			General-purpose I/O port (3V pin)
155	FRCK0	–	C	Free-run timer 0 clock input pin
	P121			General-purpose I/O port
	INT7			INT7 External interrupt input pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
155	SOT5	–	C	LIN-UART ch.5 serial data output pin
	PPG6_2			PPG ch.6 output pin (2)
	TOT2			Reload timer ch.2 output pin
156	FRCK1	–	C	Free-run timer 1 clock input pin
	P120			General-purpose I/O port
	INT6			INT6 External interrupt input pin
	SIN5			LIN-UART ch.5 serial data input pin
	PPG5_2			PPG ch.5 output pin (2)
	TOT1			Reload timer ch.1 output pin
157	FRCK3	–	C	Free-run timer 3 clock input pin
	P116			General-purpose I/O port
	SOT4			LIN-UART ch.4 serial data output pin
	TIN3			Reload timer ch.3 event input pin
	SGA3			Sound generator ch.3 SGA output pin
158	P097	–	C	General-purpose I/O port
	ICU4_1			Input capture ch.4 input pin (1)
158	INT8			INT8 External interrupt input pin
	SOT3			LIN-UART ch.3 serial data output pin
	PPG0_1			PPG ch.0 output pin (1)
	TIN0			Reload timer ch.0 event input pin
	WOT			RTC overflow output pin
159	TX2	–	C	CAN transmission data 2 output pin
	P112			General-purpose I/O port
	PPG3_2			PPG ch.3 output pin (2)
	TOT10_1			Reload timer ch.10 output pin (1)
160	VSS	–	–	GND pin
161	AN29	–	E	ADC Analog 29 input pin
	P085			General-purpose I/O port
	ICU2_2			Input capture ch.2 input pin (2)
	PPG21			PPG ch.21 output pin
	PWM1M5			SMC ch.5 output pin
	UDCAIN2			Up/down counter ch.2 AIN input pin
162	AN26	–	E	ADC Analog 26 input pin
	P082			General-purpose I/O port
	SCK6			LIN-UART ch.6 clock I/O pin
	PPG18			PPG ch.18 output pin
	PWM2P4			SMC ch.4 output pin
	UDCZIN0_1			Up/down counter ch.0 ZIN input pin (1)
163	AN23	–	E	ADC Analog 23 input pin
	P077			General-purpose I/O port
	ICU6			Input capture ch.6 input pin
	SCK7_1			LIN-UART ch.7 clock I/O pin
	PPG15_1			PPG ch.15 output pin (1)
	PWM2M3			SMC ch.3 output pin
164	AN20	–	E	ADC Analog 20 input pin
	P074			General-purpose I/O port
	ICU9			Input capture ch.9 input pin
164	SCK8	–	E	Multi-function serial ch.8 clock I/O pin
	PPG12_1			PPG ch.12 output pin (1)
	PWM1P3			SMC ch.3 output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
165	AN17	–	E	ADC Analog 17 input pin
	P071			General-purpose I/O port
	SCK9			Multi-function serial ch.9 clock I/O pin
	PWM1M2			SMC ch.2 output pin
166	AN14	–	E	ADC Analog 14 input pin
	P066			General-purpose I/O port
	PWM2P1			SMC ch.1 output pin
	UDCBIN0			Up/down counter ch.0 BIN input pin
167	AN11	–	E	ADC Analog 11 input pin
	P063			General-purpose I/O port
167	PWM2M0			SMC ch.0 output pin
	UDCBIN1			Up/down counter ch.1 BIN input pin
168	AN8	–	E	ADC Analog 8 input pin
	P060			General-purpose I/O port
	SIN10			Multi-function serial ch.10 serial data input pin
	PWM1P0			SMC ch.0 output pin
169	VCC5	–	–	+5.0V power supply pin
170	AN6	–	C	ADC Analog 6 input pin
	P106			General-purpose I/O port
	ICU10_1			Input capture ch.10 input pin (1)
	PPG4_1			PPG ch.4 output pin (1)
	TIN10_1			Reload timer ch.10 event input pin (1)
	SGA4_1			Sound generator ch.4 SGA output pin
171	AN3	–	C	ADC Analog 3 input pin
	P103			General-purpose I/O port
	ICU7_1			Input capture ch.7 input pin (1)
	SIN5_1			LIN-UART ch.5 serial data input pin (1)
	PPG1_1			PPG ch.1 output pin (1)
	TIN3_1			Reload timer ch.3 event input pin (1)
172	AN1	–	C	ADC Analog 1 input pin
	P101			General-purpose I/O port
	SOT4_1			LIN-UART ch.4 serial data output pin (1)
	PPG9			PPG ch.9 output pin
	TIN1_1			Reload timer ch.1 event input pin (1)
173	AN0	–	C	ADC Analog 0 input pin
	P100			General-purpose I/O port
	SIN4_1			LIN-UART ch.4 serial data input pin (1)
	PPG8			PPG ch.8 output pin
	TIN0_1			Reload timer ch.0 event input pin (1)
174	TX0	–	A	CAN transmission data0 output pin
	P095			General-purpose I/O port
	PPG10_1			PPG ch.10 output pin (1)
175	VSS	–	–	GND pin
176	P092	–	C	General-purpose I/O port
	ICU0_1			Input capture ch.0 input pin (1)
	INT13			INT13 External interrupt input pin
	SCK2			LIN-UART ch.2 clock I/O pin
	PPG7_1			PPG ch.7 output pin (1)
	TOT3_1			Reload timer ch.3 output pin (1)
	SGO0			Sound generator ch.0 SGO output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
177	P134	–	A	General-purpose I/O port
	ICU5			Input capture ch.5 input pin
	INT5			INT5 External interrupt input pin
	PPG1_3			PPG ch.1 output pin (3)
177	TRG2			PPG trigger 2 input pin (ch.8 to ch.11)
	TOT10			Reload timer ch.10 output pin
178	TIOB0	–	K	Base timer TIOB0 input pin
	P132			General-purpose I/O port
	ICU3			Input capture ch.3 input pin
	INT2			INT2 External interrupt input pin
	SOT1			Multi-function serial ch.1 serial data output pin / I^{2}C ch.1 serial data I/O pin
	TOT8			Reload timer ch.8 output pin
179	TIOA0	–	K	Base timer TIOA0 output pin
	P130			General-purpose I/O port
	ICU1			Input capture ch.1 input pin
	INT0			INT0 External interrupt input pin
	SCK0			Multi-function serial ch.0 clock I/O pin / I^{2}C ch.0 clock I/O pin
180	P127	–	K	General-purpose I/O port
	SOT0			Multi-function serial ch.0 serial data output pin / I^{2}C ch.0 serial data I/O pin
181	RSTX	N	F1	External reset input pin
182	RDY	–	O	External bus · Wait input pin
	P057			General-purpose I/O port (3V pin)
183	A20	–	O	External bus · Address bit20 output pin
	P052			General-purpose I/O port(3V pin)
184	A19	–	O	External bus · Address bit19 output pin
	P051			General-purpose I/O port(3V pin)
185	A18	–	O	External bus · Address bit18 output pin
	P050			General-purpose I/O port (3V pin)
186	A13	–	O	External bus · Address bit13 output pin
	P043			General-purpose I/O port (3V pin)
	QSPI_CS0			HS_SPI SSEL0 Output pin
187	A10	–	O	External bus · Address bit10 output pin
	P040			General-purpose I/O port (3V pin)
	QSPI_SIO1			HS_SPI SDATA1 I/O pin
188	A07	–	O	External bus · Address bit7 output pin
	P035			General-purpose I/O port (3V pin)
189	A03	–	O	External bus · Address bit3 output pin
189	P031	–	O	General-purpose I/O port (3V pin)
190	VSS	–	–	GND pin
191	P024	–	O	General-purpose I/O port (3V pin)
192	CS0X	–	O	External bus · Chip select 0 output pin
	P021			General-purpose I/O port (3V pin)
193	BOUT1	–	O	Display digital B1 output pin
	D14			External bus · Data bit14 I/O pin
	P016			General-purpose I/O port (3V pin)

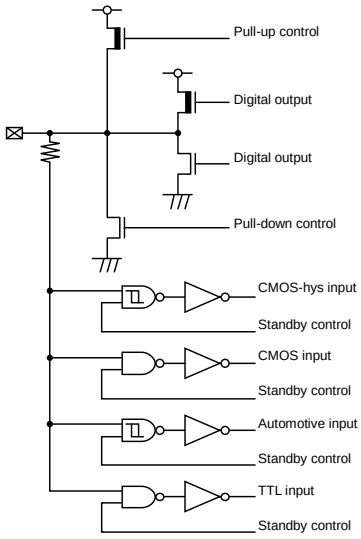
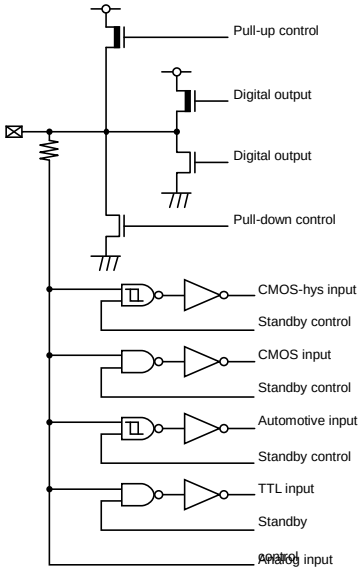
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
194	ROUT1	–	O	Display digital R1 output pin
	D10			External bus · Data bit10 I/O pin
	P012			General-purpose I/O port (3V pin)
195	D5	–	O	External bus · Data bit5 I/O pin
	P005			General-purpose I/O port (3V pin)
	SCK3_1			LIN-UART ch.3 clock I/O pin (1)
	PPG5			PPG ch.5 output pin
	TOT1_2			Reload timer ch.1 output pin (2)
196	D2	–	O	External bus · Data bit2 I/O pin
	P002			General-purpose I/O port (3V pin)
	SCK2_1			LIN-UART ch.2 clock I/O pin (1)
	PPG2			PPG ch.2 output pin
	TIN2_2			Reload timer ch.2 event input pin (2)
197	DEOUT	P	O	Display enable display period output pin
	PG7	–		General-purpose I/O port (3V pin)
198	HSYNC	–	O	Display horizontal sync signal output pin (for Internal sync)/ Display horizontal sync signal input pin (for External sync)
	PG6			General-purpose I/O port (3V pin)
199	BOUT6	–	O	Display digital B6 output pin
	PF6			General-purpose I/O port (3V pin)
200	BOUT2	–	O	Display digital B2 output pin
	PF2			General-purpose I/O port (3V pin)
201	GOUT5	–	O	Display digital G5 output pin
	PE5			General-purpose I/O port (3V pin)
202	GOUT2	–	O	Display digital G2 output pin
	PE2			General-purpose I/O port (3V pin)
203	ROUT5	–	O	Display digital R5 output pin
	PD5			General-purpose I/O port (3V pin)
204	ROUT2	–	O	Display digital R2 output pin
	PD2			General-purpose I/O port (3V pin)
205	VSS	–	–	GND pin
206	CCLK	–	O	For capture, capture clock input pin
	PH3			General-purpose I/O port (3V pin)
207	VSIN	P	O	Capture vertical sync signal input pin
	PG1	–		General-purpose I/O port (3V pin)
208	VCC3	–	–	+3.3V power supply pin
209	VSS	–	–	GND pin
210	VSS	–	–	GND pin
211	VCC3	–	–	+3.3V power supply pin
212	VCC3	–	–	+3.3V power supply pin
213	VSS	–	–	GND pin
214	VCC5	–	–	+5.0V power supply pin
215	FRCK2	–	C	Free-run timer 2 clock input pin
	P117			General-purpose I/O port
	SCK4			LIN-UART ch.4 clock I/O pin
	TRG4			PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0			Reload timer ch.0 output pin
	SGO3			Sound generator ch.3 SGO output pin

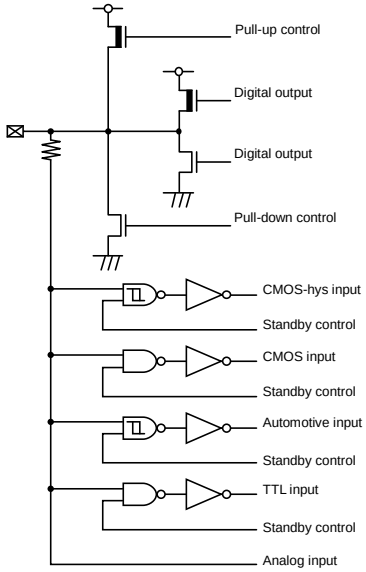
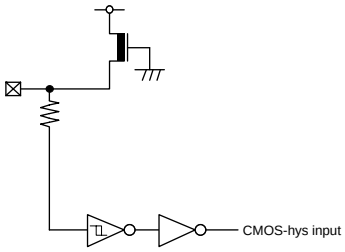
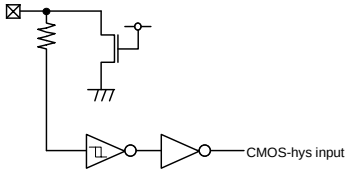
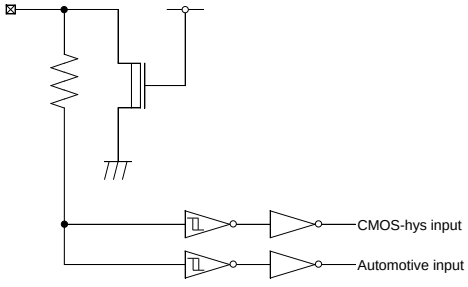
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
216	FRCK4	–	C	Free-run timer 4 clock input pin
	P115			General-purpose I/O port
	SIN4			LIN-UART ch.4 serial data input pin
	TIN2			Reload timer ch.2 event input pin
	SGO2			Sound generator ch.2 SGO output pin
217	VCC5	–	–	+5.0V power supply pin
218	VSS	–	–	GND pin
219	DVCC	–	–	SMC large current port power supply pin
220	DVSS	–	–	SMC large current port GND pin
221	DVCC	–	–	SMC large current port power supply pin
222	DVSS	–	–	SMC large current port GND pin
223	DVCC	–	–	SMC large current port power supply pin
224	DVSS	–	–	SMC large current port GND pin
225	DVCC	–	–	SMC large current port power supply pin
226	DVSS	–	–	SMC large current port GND pin
227	VCC5	–	–	+5.0V power supply pin
228	VSS	–	–	GND pin
229	VCC5	–	–	+5.0V power supply pin
230	VCC5	–	–	+5.0V power supply pin
231	VSS	–	–	GND pin
232	VSS	–	–	GND pin
233	TIOB1	–	K	Base timer TIOB1 input pin
	P133			General-purpose I/O port
	ICU4			Input capture ch.4 input pin
	INT3			INT3 External interrupt input pin
	SCK1			Multi-function serial ch.1 clock I/O pin / I^2C ch.1 clock I/O pin
	PPG11_1			PPG ch.11 output pin (1)
	TRG5			PPG trigger 5 input pin (ch.20 to ch.23)
	TOT9			Reload timer ch.9 output pin
234	VCC5	–	–	+5.0V power supply pin
235	VCC5	–	–	+5.0V power supply pin
236	VSS	–	–	GND pin
237	VSS	–	–	GND pin
238	VSS	–	–	GND pin
239	VCC3	–	–	+3.3V power supply pin
240	VCC3	–	–	+3.3V power supply pin
241	VSS	–	–	GND pin
242	VCC3	–	–	+3.3V power supply pin
243	A06	–	O	External bus · Address bit6 output pin
	P034			General-purpose I/O port (3V pin)
244	VSS	–	–	GND pin
245	VSS	–	–	GND pin
246	VCC3	–	–	+3.3V power supply pin
247	GOUT0	–	O	Display digital G0 output pin
	D11			External bus · Data bit11 I/O pin
	P013			General-purpose I/O port (3V pin)
248	VCC3	–	–	+3.3V power supply pin
249	VSS	–	–	GND pin
250	VSS	–	–	GND pin

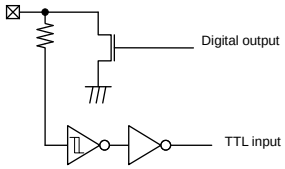
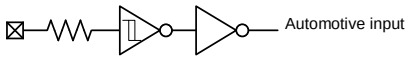
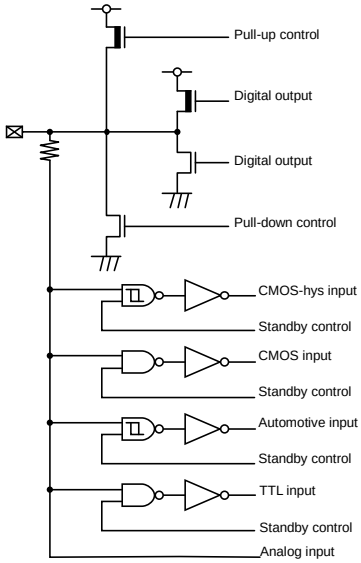
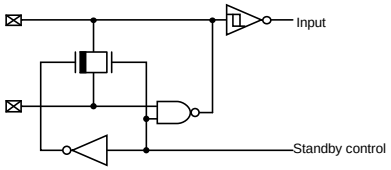
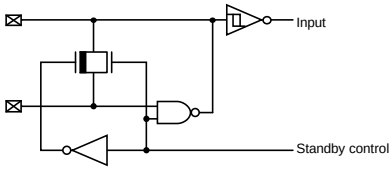
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
251	VSS	–	–	GND pin
252	VCC3	–	–	+3.3V power supply pin
253	VCC3	–	–	+3.3V power supply pin
254	VSS	–	–	GND pin
255	VCC3	–	–	+3.3V power supply pin
256	VCC3	–	–	+3.3V power supply pin
257	GND	–	–	GND pin
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
320	GND	–	–	GND pin

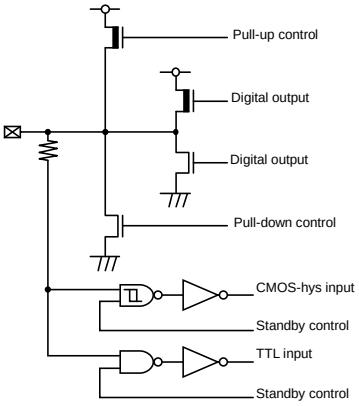
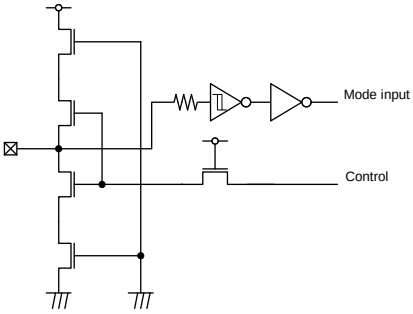
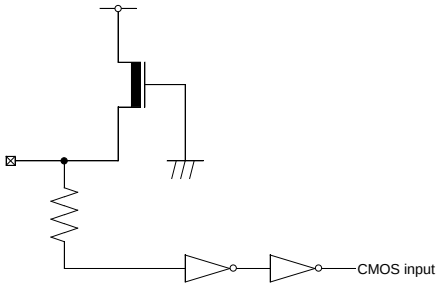
[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

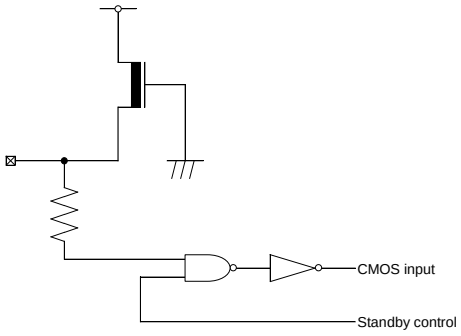
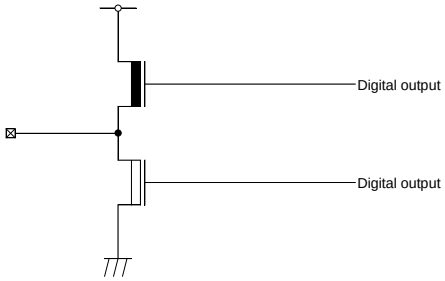
4. I/O Circuit Type

Type	Circuit	Remarks
A		• General-purpose I/O port • Output 1 mA, 2 mA • Pull-up resistor control 50 kΩ • Pull-down resistor control 50 kΩ • CMOS input • Schmitt input • TTL input • Automotive input
C		• Analog I/O, General-purpose I/O port • Output 1 mA, 2 mA • Pull-up resistor control 50 kΩ • Pull-down resistor control 50 kΩ • CMOS input • Schmitt input • TTL input • Automotive input

Type	Circuit	Remarks
E		• Analog input, General-purpose I/O port • Output 1mA,2mA,30mA (large current for SMC) • Pull-up resistor control 50 kΩ • Pull-down resistor control 50 kΩ • CMOS input • Schmitt input • TTL input • Automotive input
F1		• Schmitt input • Pull-up resistor control 50 kΩ (5 V cont)
F2		• Schmitt input • Pull-down resistor control 50 kΩ (5 V cont)
F3		• Schmitt input • Automotive input • Pull-down resister control 50 kΩ (5 V cont)

Type	Circuit	Remarks
G		• Open-drain I/O • Output 25 mA (NOD) • TTL input
J		Automotive input
K		• Analog input, General-purpose I/O port • Output 1 mA, 2 mA, 3 mA(I^2C) • Pull-up resistor control 50 kΩ • Pull-down resistor control 50 kΩ • CMOS input • Schmitt input • TTL input • Automotive input
L		Main oscillation I/O
N		Sub oscillation I/O

Type	Circuit	Remarks
O		• Output 2 mA,5 mA,10 mA and 20 mA • Pull-up resistor control 33 kΩ • Pull-down resistor control 33 kΩ • Schmitt input • TTL input
P		• Mode I/O • Schmitt input
S		Analog input (3 V)
T		Analog output (3 V)
U		• TDI/TMS/TCK (JTAG) • CMOS input • Pull-up resistor control 50 kΩ (1.2V Cont)

Type	Circuit	Remarks
V		• TRST (JTAG) • CMOS input • Pull-up resistor control 50 kΩ (1.2 V Cont)
W		• TDO (JTAG) In case of Boundary Scan Test mode. • High Impedance state In other case of Boundary Scan Test Mode. • 5mA output

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

■Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■Lead-Free Packaging
CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking
Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

6. Handling Devices

This section explains the latch-up prevention and treatment of a pin.

■For latch-up prevention
If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC pin and VSS pin, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC5, AVRH5), the NTSC power supply (AVCC3, AVR3), analog input and power supply to high-current output buffer pins must not be exceed the digital power supply (VCC5 or VCC3) when the power supply to the analog system and high-current output buffer pins is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC5), analog power supplies (AVCC5, AVRH5), and the power supply of high-current output buffer pins (DVCC) simultaneously. Or, turn on the digital power supply (VCC5), and then turn on analog power supplies (AVCC5, AVRH5) and the power supply of high-current output buffer pins (DVCC).

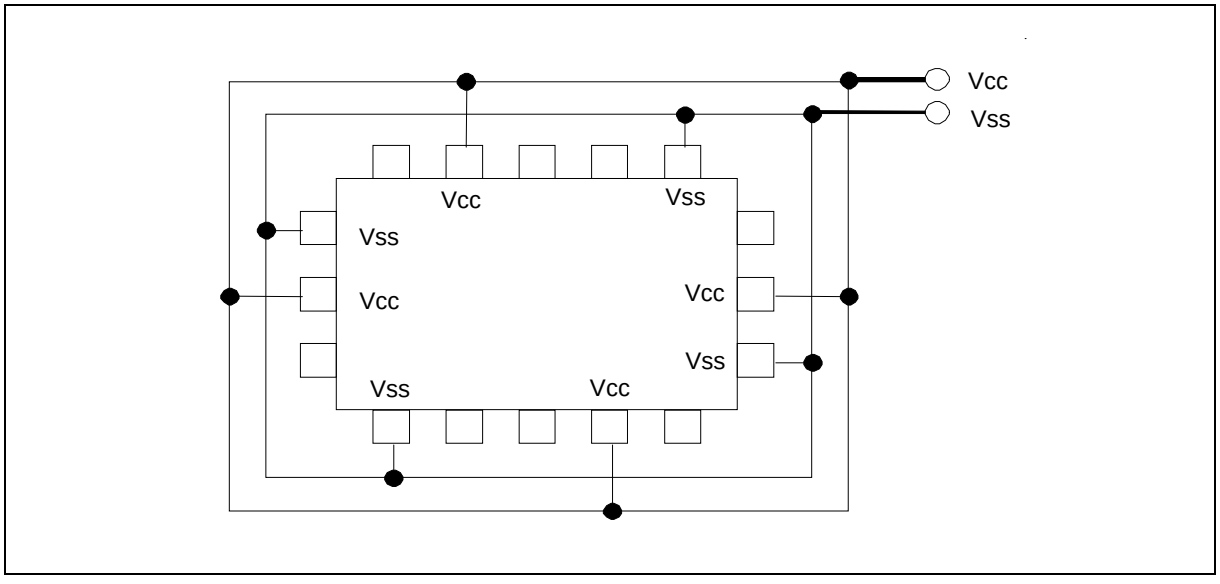
In the correct power-on sequence of GDC, similarly turn on the digital power supply (VCC3) and the NTSC analog power supply (AVCC3) simultaneously. Or, turn on the digital power supply (VCC3), and then turn on the NTSC analog power supply (AVCC3).

■Treatment of unused pins
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect a 2kΩ resistor to each of unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for opening or they must be set to the input state and treated in the same way as for the input pins.

■Power supply pins
The device is designed to ensure that if the device contains multiple VCC pin or VSS pin, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in Figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1. Power Supply Input Pins



The power supply pins should be connected to VCC pin and VSS pin of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

As for BGA package product, the solder balls of VSS and VCC are placed in the most internal circumference of solder-ball-placement. In order to connect bypass capacitor close to these balls, the capacitors had better be implemented on the back side of a system board surface on which BGA package is implemented.

■Crystal oscillation circuit
An external noise to the X0 pin or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out the X0 pin and the X1 pin, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 pin and X1 pin by ground circuits.

■Mode pins (MD2, MD1, MD0)
Connect the MD2, MD1and MD0 mode pin to the VCC pin or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and the VCC pin or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■During power-on
To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

■Notes during PLL clock operation
When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

■Treatment of A/D converter power supply pins
Connect the pins to have AVCC5=AVRH5=VCC5 and AVSS5/AVRL5=VSS even if the A/D converter is not used.

Also, similarly connect the pins of NTSC A/D converter power supply to have AVCC3=VCC3 and AVSS3=VSS. At this time, open VIN/REFOUT.

■Notes on using external clock
An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

■Power-on sequence of A/D converter analog inputs
Be sure to turn on the digital power supply (Vcc5) first, and then turn on the A/D converter power supplies (AVcc5, AVRH5, AVRL5) and analog inputs (AN0 to AN31). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc5). When the AVRH5 pin voltage is turned on or off, it must not exceed AVCC5. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc5. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

Be sure to similarly turn on the digital power supply (VCC3) first, and then turn on the A/D converter power supply (AVCC3) for NTSC and NTSC inputs (VIN, AVR). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (VCC3).

■Treatment of power supplies for high current output buffer pins (DVcc, DVss)
Be sure to turn on the digital power supply (Vcc) first, and then turn on the power supplies for high current output buffer pins (DVcc, DVss). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply (Vcc).

Even if the high current output buffer pins are used as general-purpose ports, the power supplies of high current output buffer pins (DVcc, DVss) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

■Treatment of C pin
This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

■Function switching of a multiplexed port
To switch between the port function and the multiplexed pin function, use the PFR (port function register).

■Low-power consumption mode
To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL".

Power supply for GDC can be turned off separately from the microcontroller.

Take the following notes when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

■Precautions when writing to registers including the status flag
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

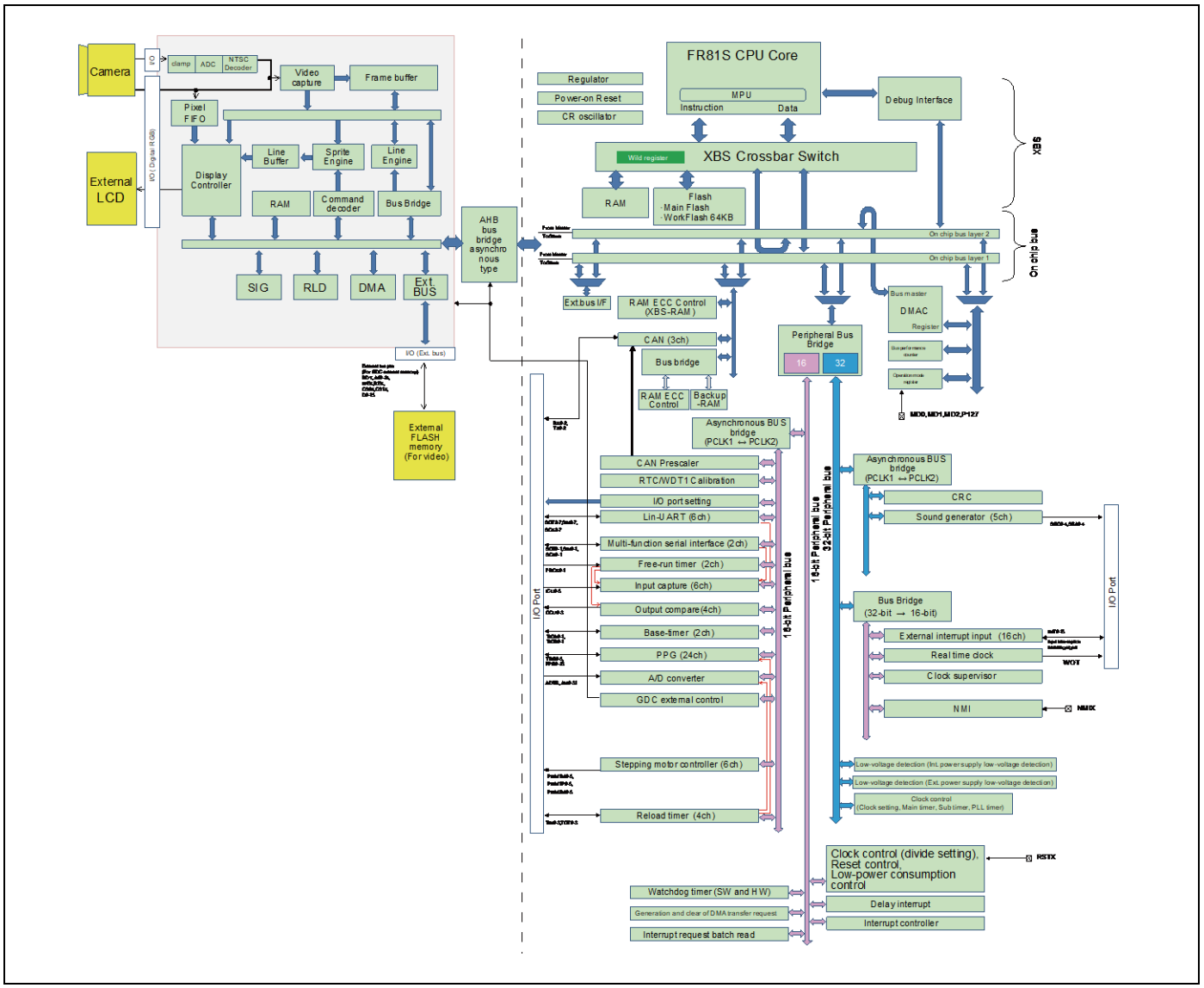
Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note:

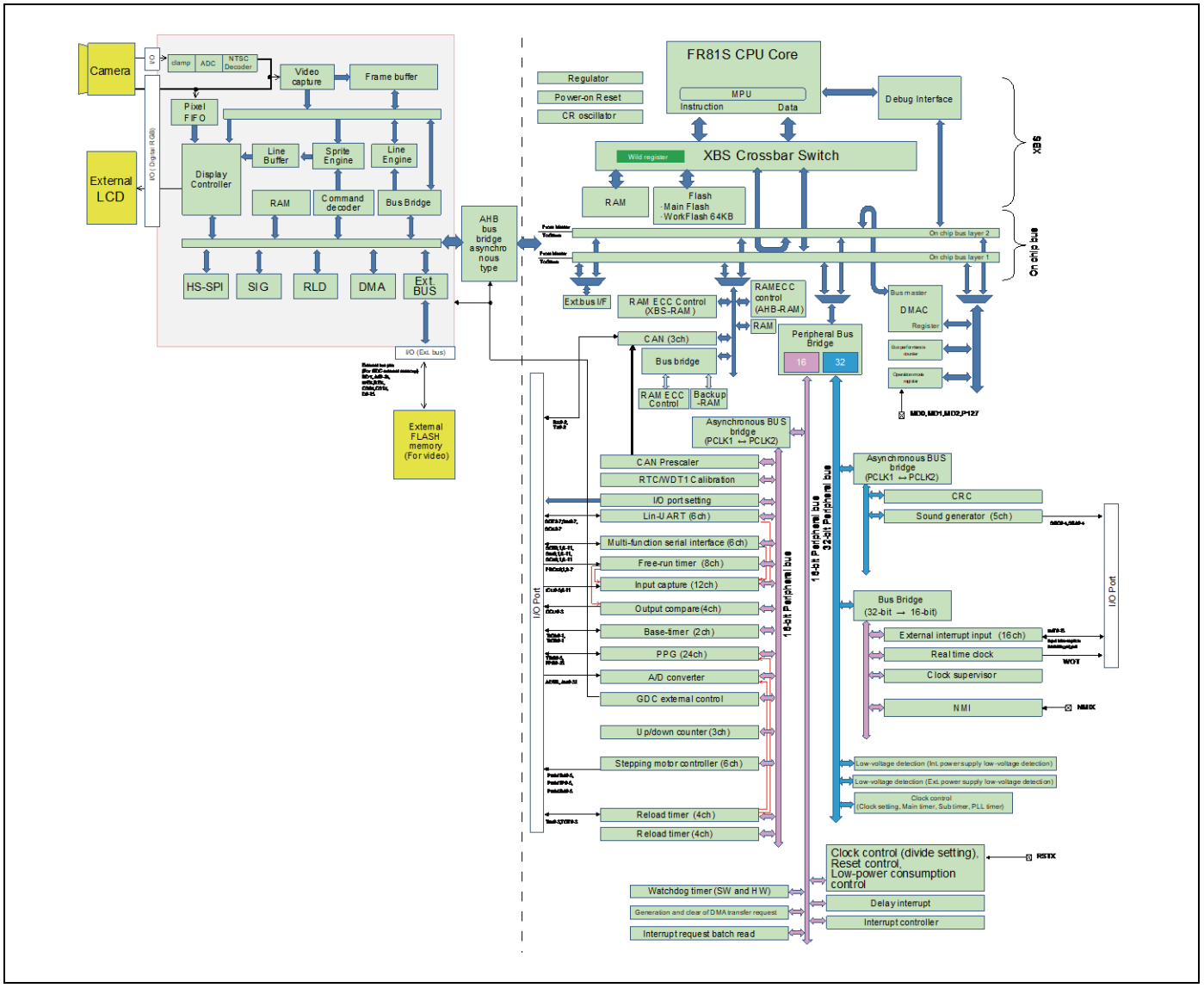
These points can be ignored because the bit instructions to a register which supports RMW are already taken the points into consideration. Care must be taken when the bit instruction is used to a register which does not support RMW.

7. Block Diagram

■CY91F591/592/594/596/597/599



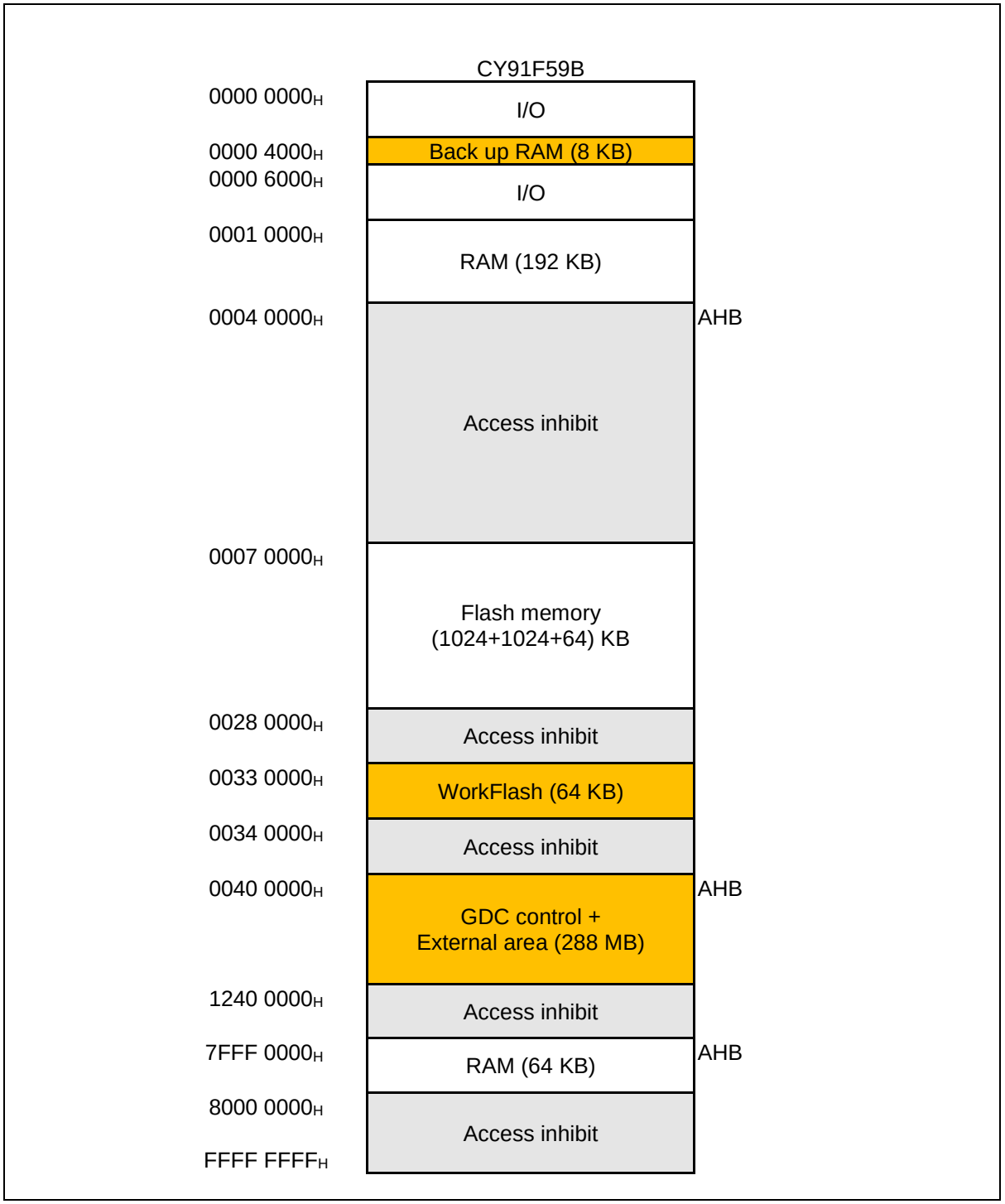
■CY91F59A/59B



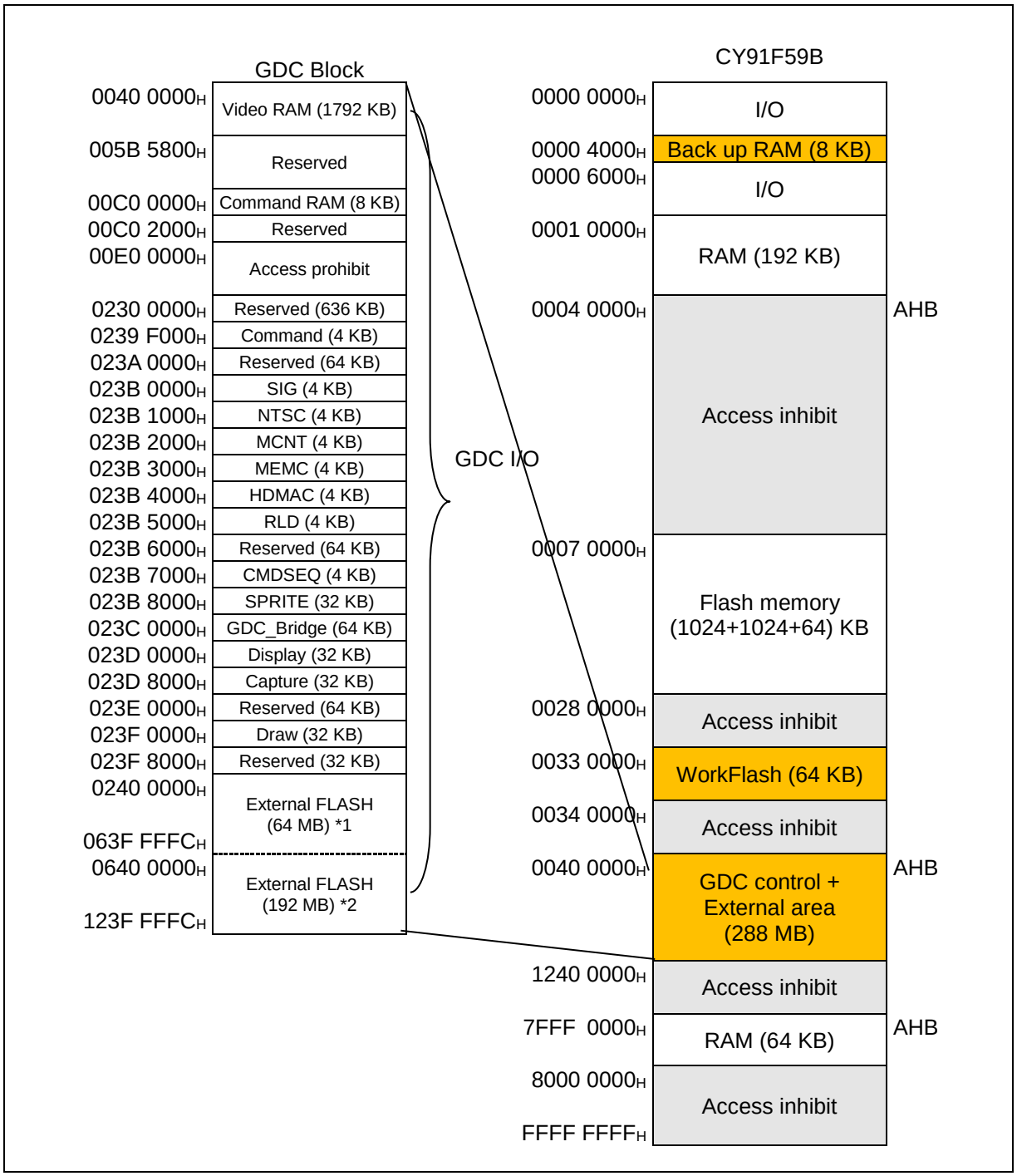
Note: I/O of peripheral functions can be confirmed at "PIN ASSIGNMENT" and "PIN DESCRIPTION".

8. Memory Map

■Memory map



■GDC memory map

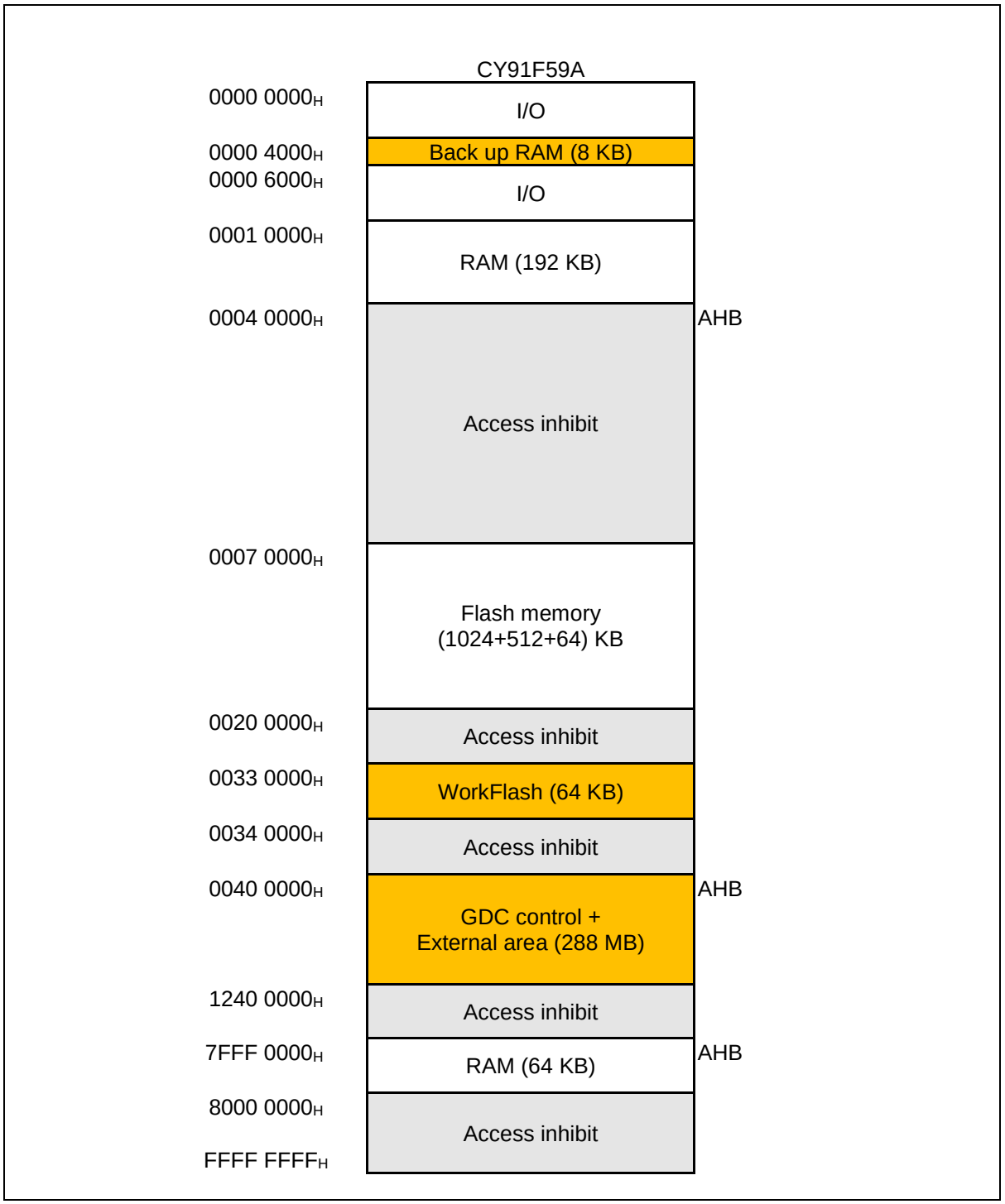


Note: The GDC area is executed mapping with the little endian.

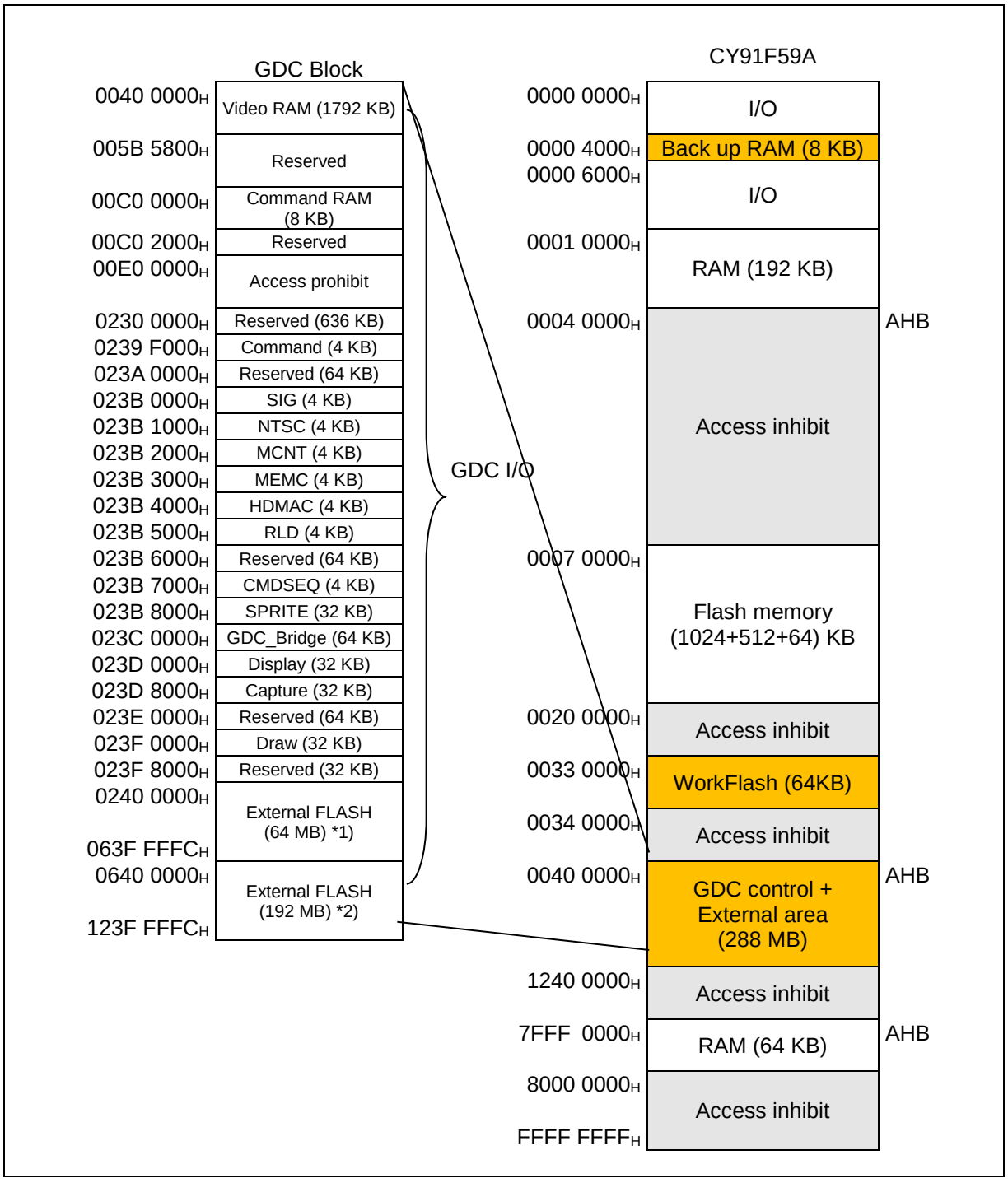
*1) Parallel interface supports 64 MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192 MB of memory space from 0640_0000H to 123F_FFFFH.
(HS-SPI totally supports 256 MB of memory space from 0240_0000H to 123F_FFFFH for External FLASH)

■Memory map


CY91F59A
0000 0000H
I/O
0000 4000H
Back up RAM (8 KB)
0000 6000H
I/O
0001 0000H
RAM (192 KB)
0004 0000H
AHB
Access inhibit
0007 0000H
Flash memory
(1024+512+64) KB
0020 0000H
Access inhibit
0033 0000H
WorkFlash (64 KB)
0034 0000H
Access inhibit
0040 0000H
AHB
GDC control +
External area (288 MB)
1240 0000H
Access inhibit
7FFF 0000H
AHB
RAM (64 KB)
8000 0000H
Access inhibit
FFFF FFFFH

■GDC memory map

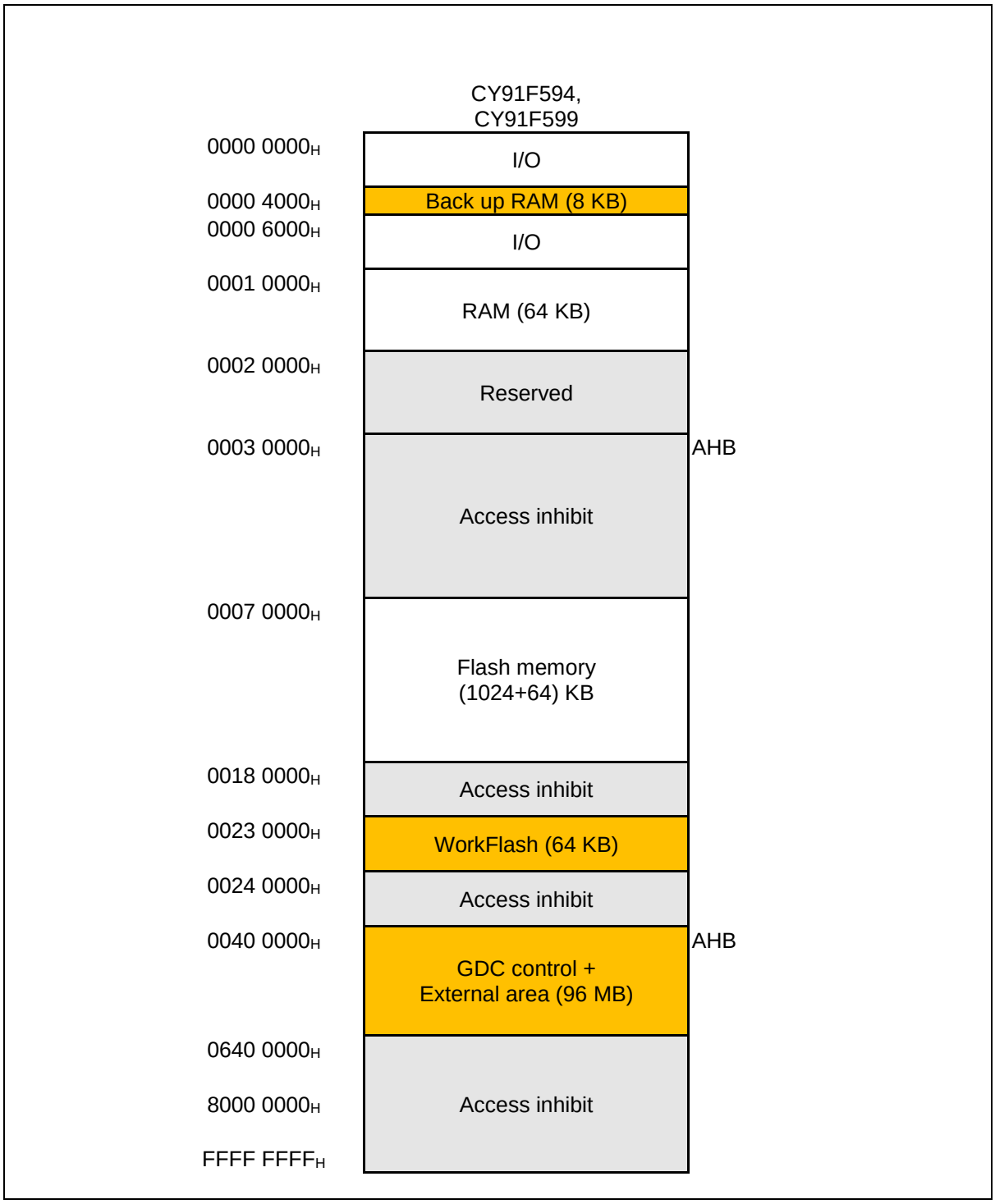


Note: The GDC area is executed mapping with the little endian.

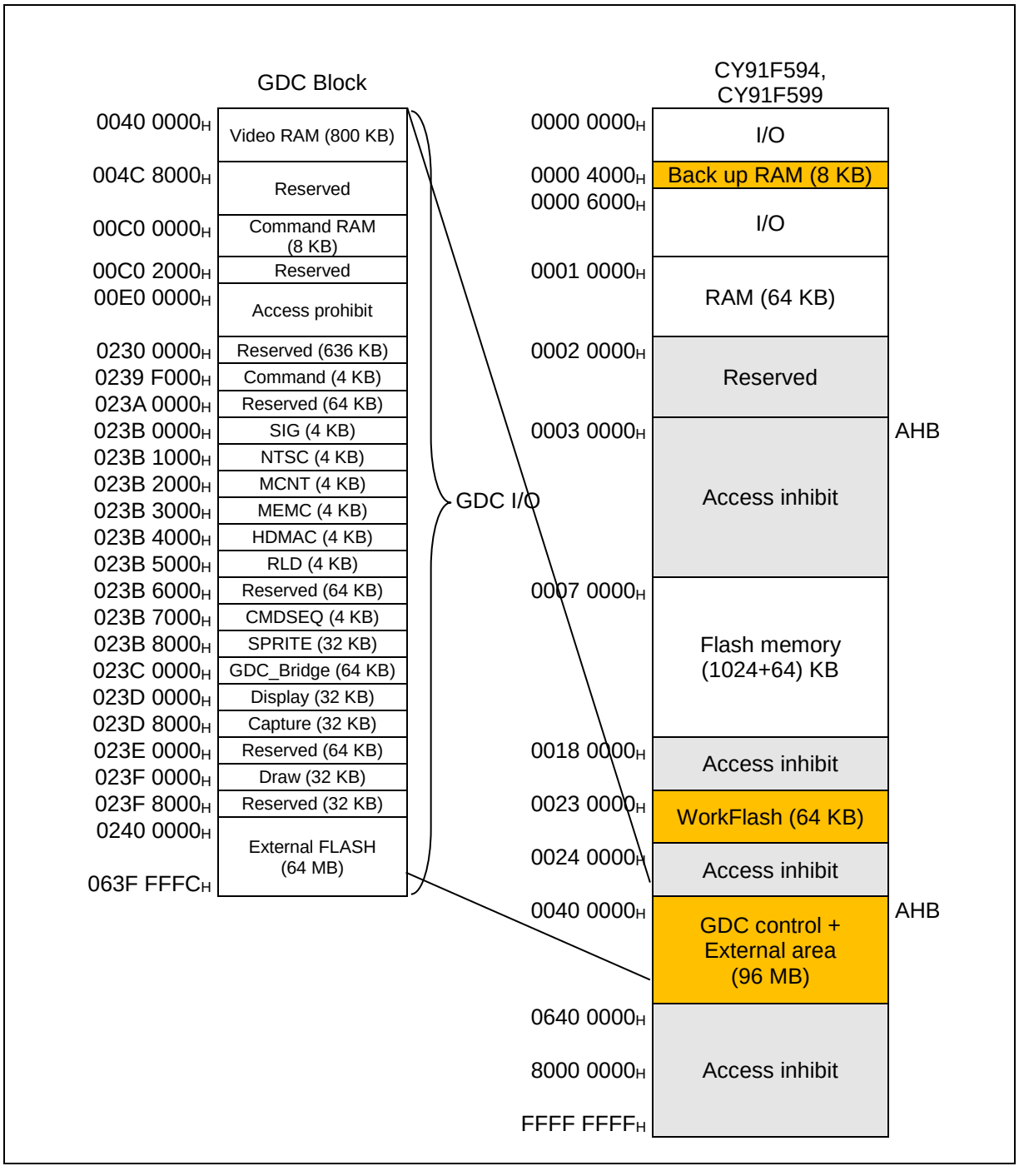
*1) Parallel interface supports 64 MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192 MB of memory space from 0640_0000H to 123F_FFFCH.
(HS-SPI totally supports 256 MB of memory space from 0240_0000H to 123F_FFFCH for External FLASH)

■Memory map

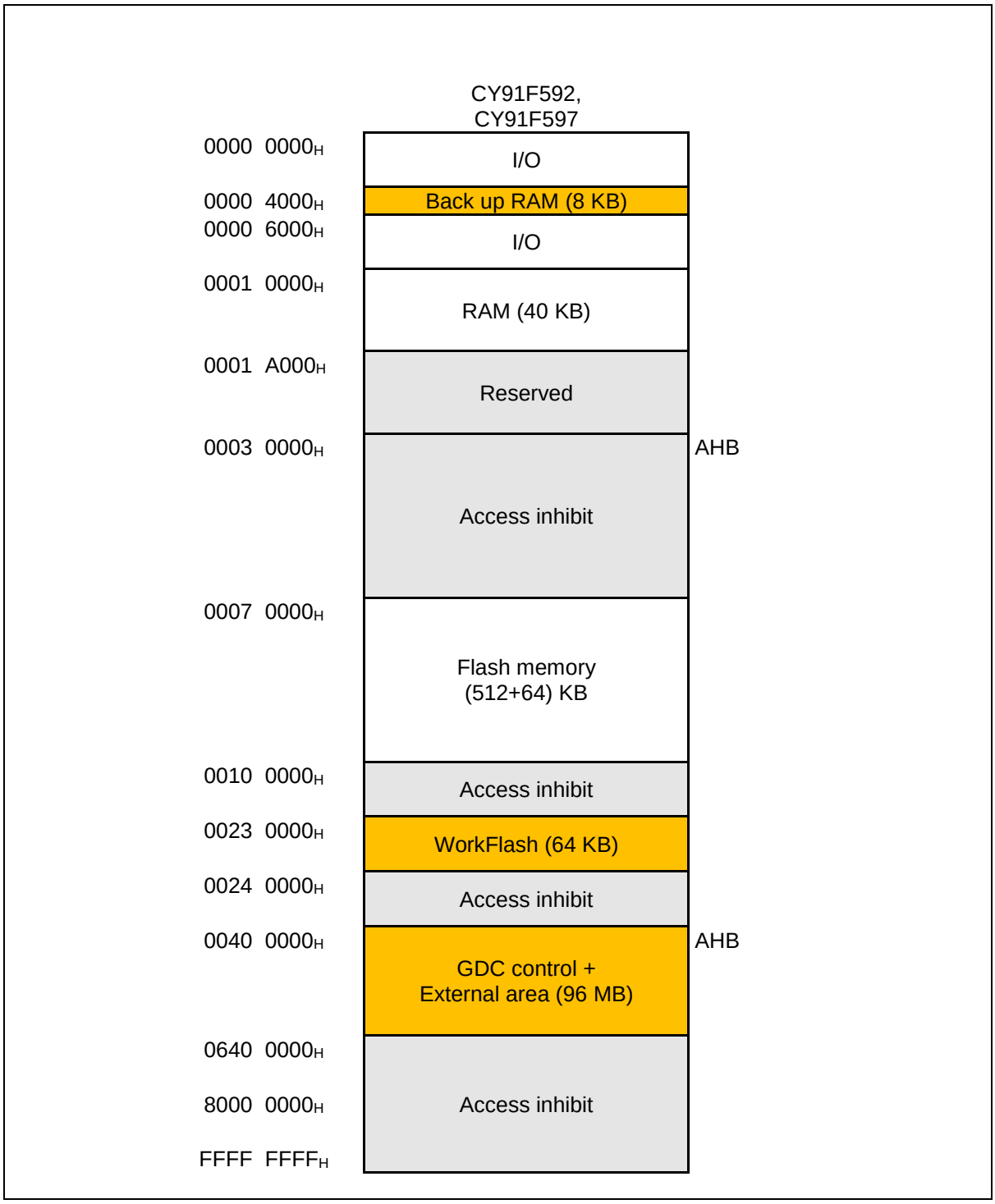

CY91F594,
CY91F599
0000 0000H
I/O
0000 4000H
Back up RAM (8 KB)
0000 6000H
I/O
0001 0000H
RAM (64 KB)
0002 0000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(1024+64) KB
0018 0000H
Access inhibit
0023 0000H
WorkFlash (64 KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96 MB)
AHB
0640 0000H
Access inhibit
8000 0000H
FFFF FFFFH

■GDC memory map

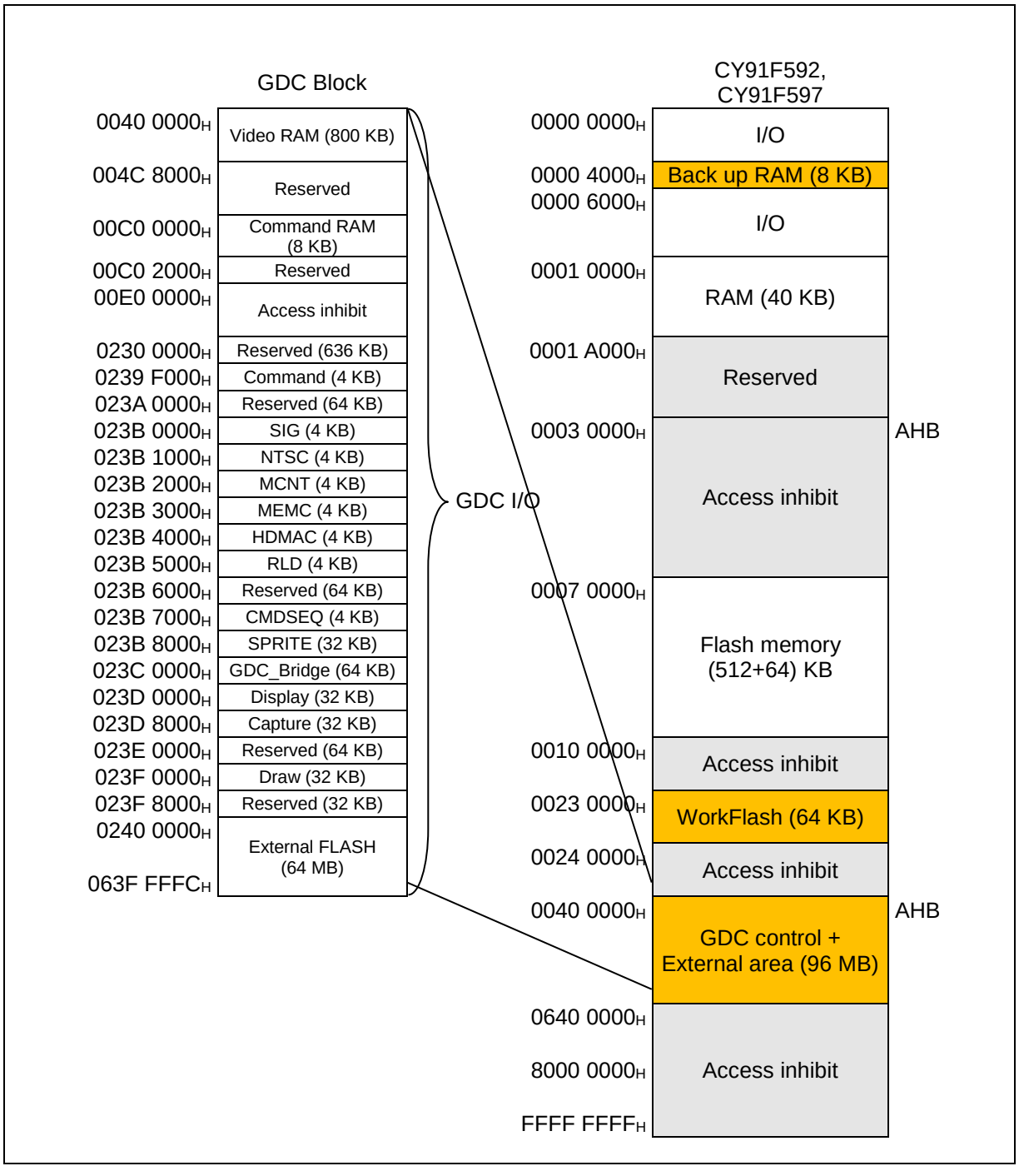


Note: The GDC area is executed mapping with the little endian.

■Memory map

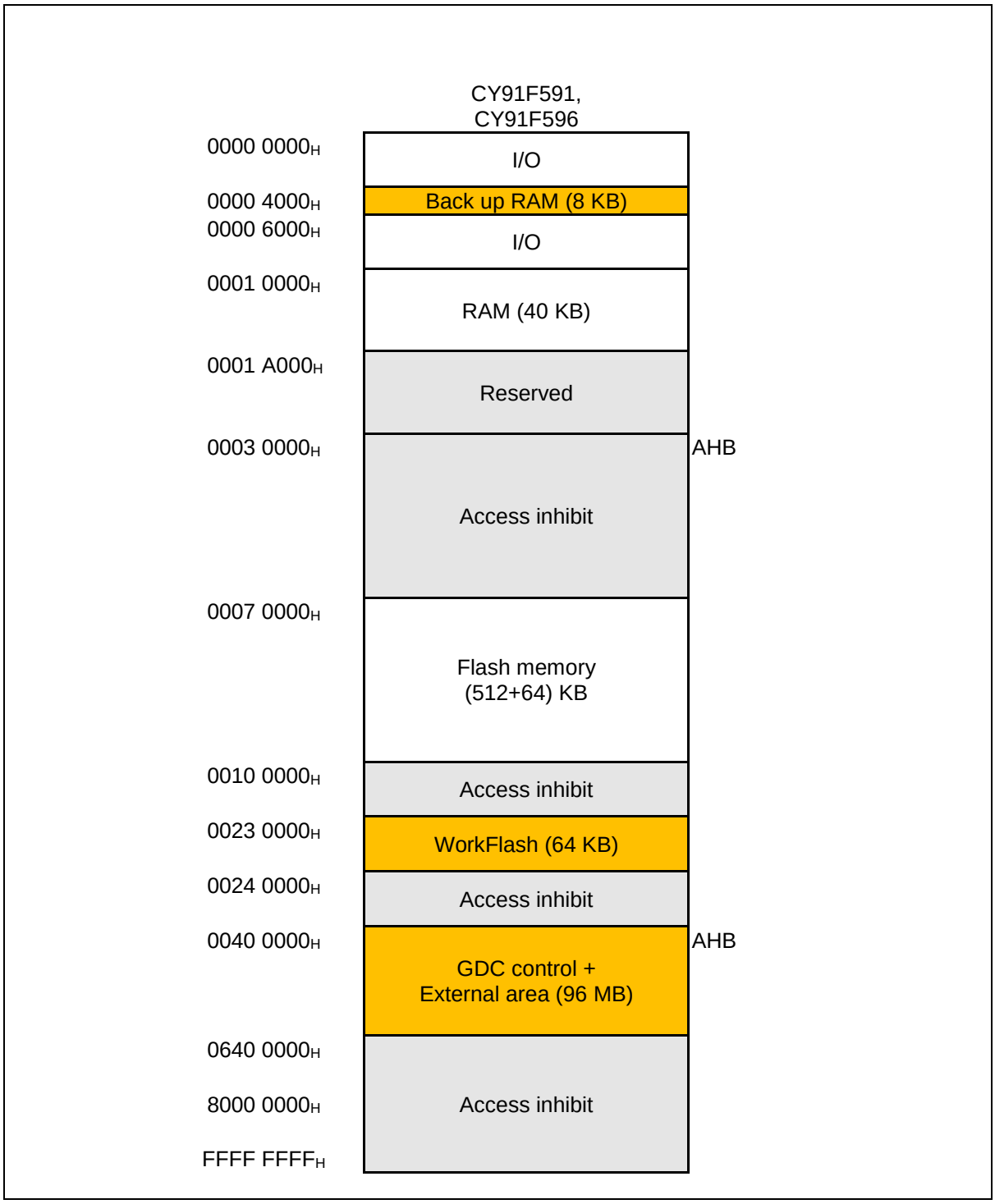

CY91F592,
CY91F597
0000 0000H
I/O
0000 4000H
Back up RAM (8 KB)
0000 6000H
I/O
0001 0000H
RAM (40 KB)
0001 A000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64 KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96 MB)
AHB
0640 0000H
8000 0000H
Access inhibit
FFFF FFFFH

■GDC memory map

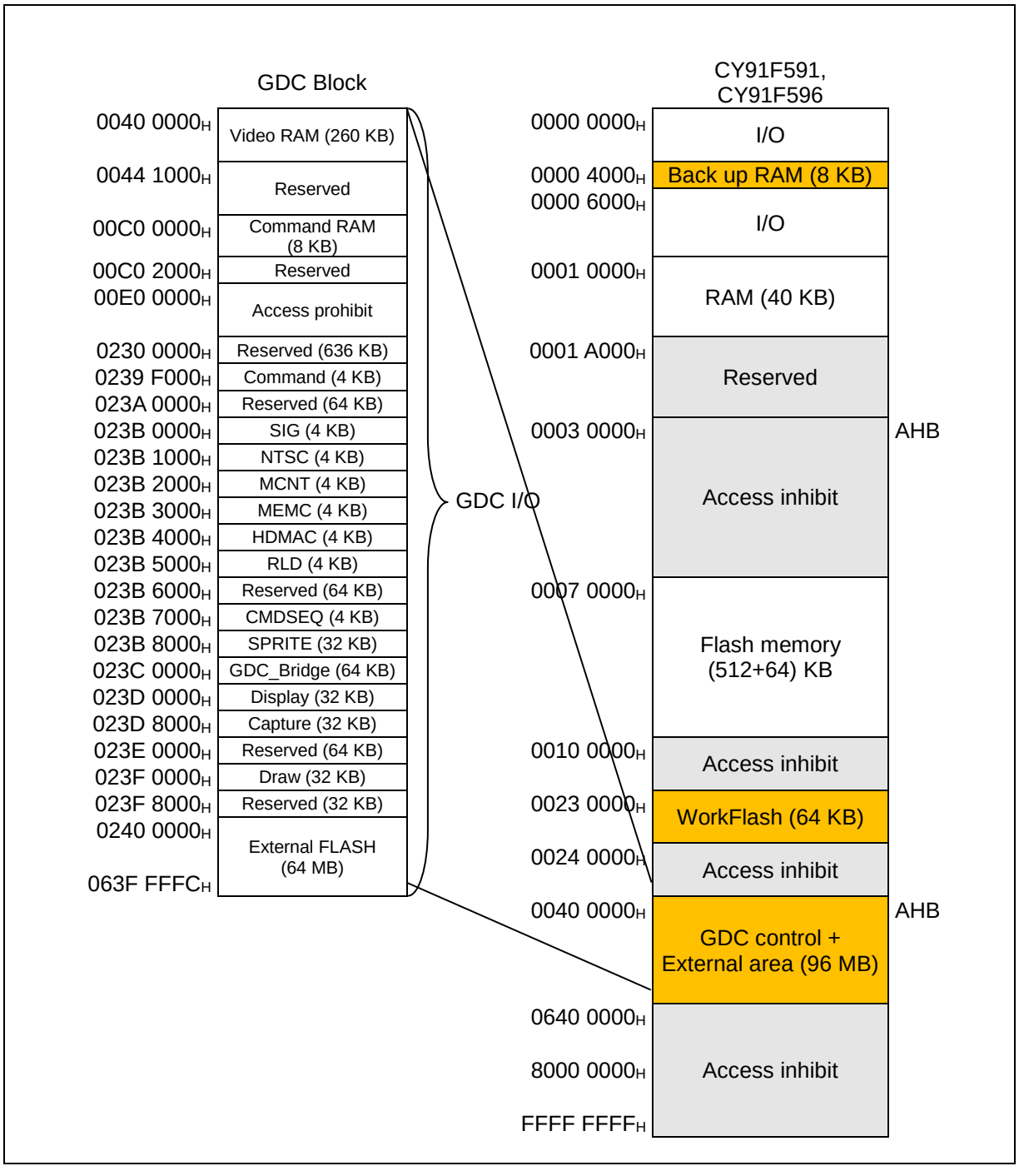


Note: The GDC area is executed mapping with the little endian.

■Memory map


CY91F591,
CY91F596
0000 0000H
I/O
0000 4000H
Back up RAM (8 KB)
0000 6000H
I/O
0001 0000H
RAM (40 KB)
0001 A000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64 KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96 MB)
AHB
0640 0000H
8000 0000H
Access inhibit
FFFF FFFFH

■GDC memory map

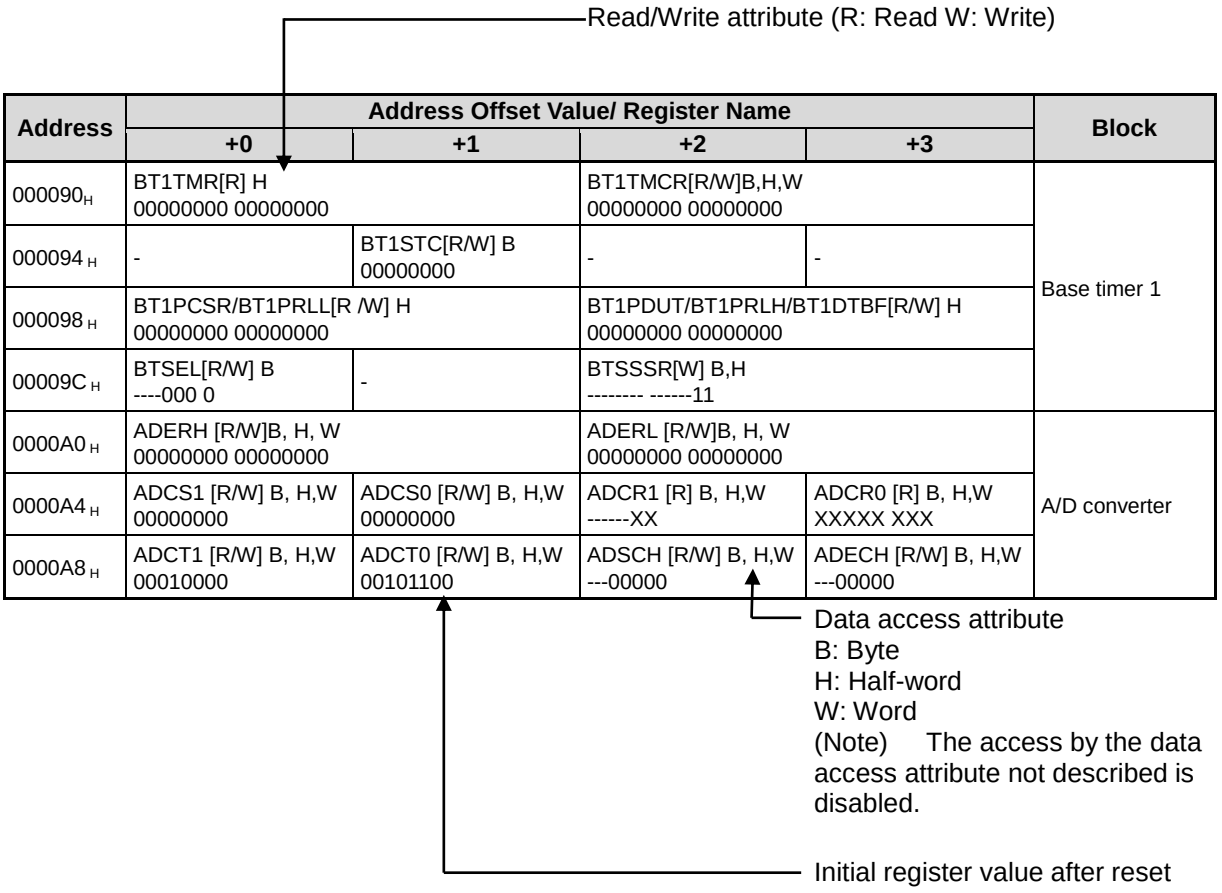


Note: The GDC area is executed mapping with the little endian.

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

■Legend of I/O Map



Address	Address Offset Value/ Register Name				Block
	+0	+1	+2	+3	
000090 H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 H	-	BT1STC[R/W] B 00000000	-	-	
000098 H	BT1PCSR/BT1PRLL[R /W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
00009C H	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
0000A0 H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access by the data access attribute not described is disabled.

■I/O map

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000000H	PDR00[R/W] B,H,W XXXXXXXX	PDR01[R/W] B,H,W XXXXXXXX	PDR02[R/W] B,H,W XXXXXXXX	PDR03[R/W] B,H,W XXXXXXXX	Port data register
000004H	PDR04[R/W] B,H,W XXXXXXXX	PDR05[R/W] B,H,W XXXXXXXX	PDR06[R/W] B,H,W XXXXXXXX	PDR07[R/W] B,H,W XXXXXXXX	
000008H	PDR08[R/W] B,H,W XXXXXXXX	PDR09[R/W] B,H,W XXXXXXXX	PDR10[R/W] B,H,W XXXXXXXX	PDR11[R/W] B,H,W XXXXXXXX	
00000CH	PDR12[R/W] B,H,W XXXXXXXX	PDR13[R/W] B,H,W XX-XXXXX	—	—	
000010H	PDRA[R/W] B,H,W XXXXXX--	PDRB[R/W] B,H,W XXXXXX--	PDRC[R/W] B,H,W XXXXXX--	PDRD[R/W] B,H,W XXXXXX--	
000014H	PDRE[R/W] B,H,W XXXXXX--	PDRF[R/W] B,H,W XXXXXX--	PDRG[R/W] B,H,W XXXXXXXX	PDRH[R/W] B,H,W ----X---	
000018H to 000028H	—	—	—	—	Reserved
00002CH to 000030H	—	—	—	—	Reserved
000034H to 000038H	—	—	—	—	Reserved
00003CH	WDTCR0[R/W] B,H,W -0--0000	WDTCPR0[W] B,H,W 00000000	WDTCR1[R] B,H,W ----0110	WDTCPR1[W] B,H,W 00000000	Watchdog timer [S]
000040H	—	—	—	—	Reserved
000044H	DICR [R/W] B XXXXXXX0	—	—	—	Delay interrupt
000048H to 00005CH	—	—	—	—	Reserved
000060H	TMRLRA0 [R/W] H XXXXXXXX XXXXXXXX		TMR0 [R] H XXXXXXXX XXXXXXXX		Reload timer 0
000064H	TMRLRB0 [R/W] H XXXXXXXX XXXXXXXX		TMCSR0 [R/W] B, H,W 00000000 0-000000		
000068H to 00007CH	—	—	—	—	Reserved
000080H	BT0TMR [R] H 00000000 00000000		BT0TMCR [R/W] H -0000000 00000000		Base timer 0
000084H	—	BT0STC [R/W] B 0000-000	—	—	
000088H	BT0PCSR/BT0PRLL [R/W] H XXXXXXXX XXXXXXXX		BT0PDUT/BT0PRLH/BT0DTBF [R/W] H XXXXXXXX XXXXXXXX		
00008CH	—	—	—	—	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000090H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -0000000 00000000		Base timer 1
000094H	—	BT1STC [R/W] B 0000-000	—	—	
000098H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
00009CH	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base timer 0,1
0000A0H	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
0000A4H	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXXXXX	
0000A8H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	
0000ACH	—	—	—	—	Reserved
0000B0H	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-function serial 0 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I2C mode is not set immediately after reset.
0000B4H	RDR0/(TDR0)[R/W] B,H,W *1 -------0 00000000		BGR0 [R/W] H,W 00000000 00000000		
0000B8H	— / (ISMK0) [R/W] B,H,W -------- *2	— / (ISBA0) [R/W] B,H,W -------- *2	—	—	
0000BCH	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	
0000C0H	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-function serial 1 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I2C mode is not set immediately after reset.
0000C4H	RDR1/(TDR1)[R/W] B,H,W *1 -------0 00000000		BGR1 [R/W] H,W 00000000 00000000		
0000C8H	— / (ISMK1) [R/W] B,H,W -------- *2	— /(ISBA1) [R/W] B,H,W -------- *2	—	—	
0000CCH	FCR11 [R/W] B, H, W ---00100	FCR01[R/W] B, H, W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
0000D0H	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
0000D4H	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
0000D8H	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
0000DCH	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0000E0H	SCR4 [R/W] B, H, W 00000000	SMR4 [R/W] B, H, W 00000000	SSR4 [R/W] B, H, W 00001000	RDR4 /TDR4 [R/W] B, H, W 00000000	LIN-UART4
0000E4H	ESCR4 [R/W] B, H, W 00000X00	ECCR4 [R/W] B, H, W -0000-XX	BGR4 [R/W] B, H, W -0000000 00000000		
0000E8H	SCR5 [R/W] B, H, W 00000000	SMR5 [R/W] B, H, W 00000000	SSR5 [R/W] B, H, W 00001000	RDR5 /TDR5 [R/W] B, H, W 00000000	LIN-UART5
0000ECH	ESCR5 [R/W] B, H, W 00000X00	ECCR5 [R/W] B, H, W -0000-XX	BGR5 [R/W] B, H, W -0000000 00000000		
0000F0H	SCR6 [R/W] B, H, W 00000000	SMR6 [R/W] B, H, W 00000000	SSR6 [R/W] B, H, W 00001000	RDR6 /TDR6 [R/W] B, H, W 00000000	LIN-UART6
0000F4H	ESCR6 [R/W] B, H, W 00000X00	ECCR6 [R/W] B, H, W -0000-XX	BGR6 [R/W] B, H, W -0000000 00000000		
0000F8H	SCR7 [R/W] B, H, W 00000000	SMR7 [R/W] B, H, W 00000000	SSR7 [R/W] B, H, W 00001000	RDR7 /TDR7 [R/W] B, H, W 00000000	LIN-UART7
0000FCH	ESCR7 [R/W] B, H, W 00000X00	ECCR7 [R/W] B, H, W -0000-XX	BGR7 [R/W] B, H, W -0000000 00000000		
000100H	TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX		TMR1 [R] H XXXXXXXX XXXXXXXX		Reload timer 1
000104H	TMRLRB1 [R/W] H XXXXXXXX XXXXXXXX		TMCSR1 [R/W] B, H,W 00000000 0-000000		
000108H	TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX		TMR2 [R] H XXXXXXXX XXXXXXXX		Reload timer 2
00010CH	TMRLRB2 [R/W] H XXXXXXXX XXXXXXXX		TMCSR2 [R/W] B, H,W 00000000 0-000000		
000110H	TMRLRA3 [R/W] H XXXXXXXX XXXXXXXX		TMR3 [R] H XXXXXXXX XXXXXXXX		Reload timer 3
000114H	TMRLRB3 [R/W] H XXXXXXXX XXXXXXXX		TMCSR3 [R/W] B, H,W 00000000 0-000000		
000118H to 000140H	—	—	—	—	Reserved
000144H	GCN13 [R/W] H 00110010 00010000		—	GCN23 [R/W] B ----0000	PPG12,13,14,15 control
000148H	GCN14 [R/W] H 00110010 00010000		—	GCN24 [R/W] B ----0000	PPG16,17,18,19 control
00014CH	GCN15 [R/W] H 00110010 00010000		—	GCN25 [R/W] B ----0000	PPG20,21,22,23 control
000150H	PTMR11 [R] H,W 11111111 11111111		PCSR11 [W] H, W XXXXXXXX XXXXXXXX		PPG11
000154H	PDUT11 [W] H,W XXXXXXXX XXXXXXXX		PCN11 [R/W] B, H,W 0000000- 000000-0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000158H	PTMR12 [R] H,W 11111111 11111111		PCSR12 [W] H,W XXXXXXXX XXXXXXXX		PPG12
00015CH	PDUT12 [W] H,W XXXXXXXX XXXXXXXX		PCN12 [R/W] B, H,W 0000000- 000000-0		
000160H	PTMR13 [R] H,W 11111111 11111111		PCSR13 [W] H,W XXXXXXXX XXXXXXXX		PPG13
000164H	PDUT13 [W] H,W XXXXXXXX XXXXXXXX		PCN13 [R/W] B, H,W 0000000- 000000-0		
000168H	PTMR14 [R] H,W 11111111 11111111		PCSR14 [W] H,W XXXXXXXX XXXXXXXX		PPG14
00016CH	PDUT14 [W] H,W XXXXXXXX XXXXXXXX		PCN14 [R/W] B, H,W 0000000- 000000-0		
000170H	PTMR15 [R] H,W 11111111 11111111		PCSR15 [W] H,W XXXXXXXX XXXXXXXX		PPG15
000174H	PDUT15 [W] H,W XXXXXXXX XXXXXXXX		PCN15 [R/W] B, H,W 0000000- 000000-0		
000178H	PTMR16 [R] H,W 11111111 11111111		PCSR16 [W] H, W XXXXXXXX XXXXXXXX		PPG16
00017CH	PDUT16 [W] H,W XXXXXXXX XXXXXXXX		PCN16 [R/W] B, H,W 0000000- 000000-0		
000180H	PTMR17 [R] H,W 11111111 11111111		PCSR17 [W] H,W XXXXXXXX XXXXXXXX		PPG17
000184H	PDUT17 [W] H,W XXXXXXXX XXXXXXXX		PCN17 [R/W] B, H,W 0000000- 000000-0		
000188H	PTMR18 [R] H,W 11111111 11111111		PCSR18 [W] H,W XXXXXXXX XXXXXXXX		PPG18
00018CH	PDUT18 [W] H,W XXXXXXXX XXXXXXXX		PCN18 [R/W] B, H,W 0000000- 000000-0		
000190H	PTMR19 [R] H,W 11111111 11111111		PCSR19 [W] H,W XXXXXXXX XXXXXXXX		PPG19
000194H	PDUT19 [W] H,W XXXXXXXX XXXXXXXX		PCN19 [R/W] B, H,W 0000000- 000000-0		
000198H	PTMR20 [R] H,W 11111111 11111111		PCSR20 [W] H,W XXXXXXXX XXXXXXXX		PPG20
00019CH	PDUT20 [W] H,W XXXXXXXX XXXXXXXX		PCN20 [R/W] B, H,W 0000000- 000000-0		
0001A0H	PTMR21 [R] H,W 11111111 11111111		PCSR21 [W] H, W XXXXXXXX XXXXXXXX		PPG21
0001A4H	PDUT21 [W] H,W XXXXXXXX XXXXXXXX		PCN21 [R/W] B, H,W 0000000- 000000-0		
0001A8H	PTMR22 [R] H,W 11111111 11111111		PCSR22 [W] H,W XXXXXXXX XXXXXXXX		PPG22
0001ACH	PDUT22 [W] H,W XXXXXXXX XXXXXXXX		PCN22 [R/W] B, H,W 0000000- 000000-0		
0001B0H	PTMR23 [R] H,W 11111111 11111111		PCSR23 [W] H,W XXXXXXXX XXXXXXXX		PPG23
0001B4H	PDUT23 [W] H,W XXXXXXXX XXXXXXXX		PCN23 [R/W] B, H,W 0000000- 000000-0		
0001B8H	TMRLRA7 [R/W] H XXXXXXXX XXXXXXXX		TMR7 [R] H XXXXXXXX XXXXXXXX		Reload timer 7 CY91F59A/B only
0001BCH	TMRLRB7 [R/W] H XXXXXXXX XXXXXXXX		TMCSR7 [R/W] B, H,W 00000000 0-000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0001C0H	TMRLRA8 [R/W] H XXXXXXXX XXXXXXXX		TMR8 [R] H XXXXXXXX XXXXXXXX		Reload timer 8 CY91F59A/B only
0001C4H	TMRLRB8 [R/W] H XXXXXXXX XXXXXXXX		TMCSR8 [R/W] B, H,W 00000000 0-000000		
0001C8H	TMRLRA9 [R/W] H XXXXXXXX XXXXXXXX		TMR9 [R] H XXXXXXXX XXXXXXXX		Reload timer 9 CY91F59A/B only
0001CCH	TMRLRB9 [R/W] H XXXXXXXX XXXXXXXX		TMCSR9 [R/W] B, H,W 00000000 0-000000		
0001D0H	TMRLRA10 [R/W] H XXXXXXXX XXXXXXXX		TMR10 [R] H XXXXXXXX XXXXXXXX		Reload timer 10 CY91F59A/B only
0001D4H	TMRLRB10 [R/W] H XXXXXXXX XXXXXXXX		TMCSR10 [R/W] B, H,W 00000000 0-000000		
0001D8H to 0001DCH	—	—	—	—	Reserved
0001E0H	SCR10 [R/W] B,H,W 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R/W] B,H,W 0-000011	ESCR10 [R/W] B,H,W -0000000	Multi-function serial 10 *1: Byte access is possible only for access to lower 8 bits. CY91F59A/B only
0001E4H	RDR10/(TDR10)[R/W] B,H,W *1 -------0 00000000		BGR10 [R/W] H,W 00000000 00000000		
0001E8H	—	—	—	—	
0001ECH	FCR110 [R/W] B,H,W ---00100	FCR010 [R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
0001F0H	SCR11 [R/W] B,H,W 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R/W] B,H,W 0-000011	ESCR11 [R/W] B,H,W -0000000	Multi-function serial 11 *1: Byte access is possible only for access to lower 8 bits. CY91F59A/B only
0001F4H	RDR11/(TDR11)[R/W] B,H,W *1 -------0 00000000		BGR11 [R/W] H,W 00000000 00000000		
0001F8H	—	—	—	—	
0001FCH	FCR111 [R/W] B,H,W ---00100	FCR011 [R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000200H	PWC20 [R/W] H,W ------XX XXXXXXXX		PWC10 [R/W] H,W ------XX XXXXXXXX		Stepping motor controller
000204H	—	PWC0 [R/W] B -00000--	PWS20 [R/W] B,H,W -0000000	PWS10 [R/W] B,H,W --000000	
000208H	PWC21 [R/W] H,W ------XX XXXXXXXX		PWC11 [R/W] H,W ------XX XXXXXXXX		
00020CH	—	PWC1 [R/W] B -00000--	PWS21 [R/W] B,H,W -0000000	PWS11 [R/W] B,H,W --000000	
000210H	PWC22 [R/W] H,W ------XX XXXXXXXX		PWC12 [R/W] H,W ------XX XXXXXXXX		
000214H	—	PWC2 [R/W] B -00000--	PWS22 [R/W] B,H,W -0000000	PWS12 [R/W] B,H,W --000000	
000218H	PWC23 [R/W] H,W ------XX XXXXXXXX		PWC13 [R/W] H,W ------XX XXXXXXXX		
00021CH	—	PWC3 [R/W] B -00000--	PWS23 [R/W] B,H,W -0000000	PWS13 [R/W] B,H,W --000000	
000220H	PWC24 [R/W] H,W ------XX XXXXXXXX		PWC14 [R/W] H,W ------XX XXXXXXXX		
000224H	—	PWC4 [R/W] B -00000--	PWS24 [R/W] B,H,W -0000000	PWS14 [R/W] B,H,W --000000	
000228H	PWC25 [R/W] H,W ------XX XXXXXXXX		PWC15 [R/W] H,W ------XX XXXXXXXX		
00022CH	—	PWC5 [R/W] B -00000--	PWS25 [R/W] B,H,W -0000000	PWS15 [R/W] B,H,W --000000	
000230H to 00023CH	—	—	—	—	Reserved
000240H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 0
000244H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
000248H	TCCSH0 [R/W]B, H, W 0-----00	TCCSL0 [R/W]B, H, W -1-00000	—		
00024CH	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 1
000250H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
000254H	TCCSH1 [R/W]B, H, W 0-----00	TCCSL1 [R/W]B, H, W -1-00000	—		
000258H	—	—	—	—	Reserved
00025CH	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B ----0000	PPG0,1,2,3 control
000260H	GCN11 [R/W] H 00110010 00010000		—	GCN21 [R/W] B ----0000	PPG4,5,6,7 control
000264H	GCN12 [R/W] H 00110010 00010000		—	GCN22 [R/W] B ----0000	PPG8,9,10,11 control

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000268H	—	—	—	PPGDIV [R/W] B ------00	PPG0
00026CH	PTMR0 [R] H,W 11111111 11111111		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		
000270H	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PCN0 [R/W] B, H,W 0000000- 000000-0		
000274H	PTMR1 [R] H,W 11111111 11111111		PCSR1 [W] H, W XXXXXXXX XXXXXXXX		PPG1
000278H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PCN1 [R/W] B, H,W 0000000- 000000-0		
00027CH	PTMR2 [R] H,W 11111111 11111111		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2
000280H	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PCN2 [R/W] B, H,W 0000000- 000000-0		
000284H	PTMR3 [R] H,W 11111111 11111111		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3
000288H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PCN3 [R/W] B, H,W 0000000- 000000-0		
00028CH	PTMR4 [R] H,W 11111111 11111111		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
000290H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PCN4 [R/W] B, H,W 0000000- 000000-0		
000294H	PTMR5 [R] H,W 11111111 11111111		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
000298H	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PCN5 [R/W] B, H,W 0000000- 000000-0		
00029CH	PTMR6 [R] H,W 11111111 11111111		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
0002A0H	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PCN6 [R/W] B, H,W 0000000- 000000-0		
0002A4H	PTMR7 [R] H,W 11111111 11111111		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
0002A8H	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PCN7 [R/W] B, H,W 0000000- 000000-0		
0002ACH	PTMR8 [R] H,W 11111111 11111111		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
0002B0H	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PCN8 [R/W] B, H,W 0000000- 000000-0		
0002B4H	PTMR9 [R] H,W 11111111 11111111		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
0002B8H	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PCN9 [R/W] B, H,W 0000000- 000000-0		
0002BCH	PTMR10 [R] H,W 11111111 11111111		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
0002C0H	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PCN10 [R/W] B, H,W 0000000- 000000-0		
0002C4H	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 0,1
0002C8H	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002CCH	ICFS01 [R/W] B, H, W ------00	—	LSYNS0 [R/W] B, H, W --000000	ICS01 [R/W] B, H, W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0002D0H	IPCP2 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 2,3
0002D4H	IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002D8H	ICFS23 [R/W] B, H, W ------00	—	—	ICS23 [R/W] B, H, W 00000000	
0002DCH	IPCP4 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 4,5
0002E0H	IPCP5 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0002E4H	ICFS45 [R/W] B, H, W ------00	—	—	ICS45 [R/W] B, H, W 00000000	
0002E8H	OCCP0 [R/W] W 00000000 00000000 00000000 00000000				Output compare 0,1
0002ECH	OCCP1 [R/W] W 00000000 00000000 00000000 00000000				
0002F0H	OCFS01 [R/W] B, H, W ------11	—	OCSH01[R/W] B, H, W ---0--00	OCSL01[R/W] B, H, W 0000--00	
0002F4H	OCCP2 [R/W] W 00000000 00000000 00000000 00000000				Output compare 2,3
0002F8H	OCCP3 [R/W] W 00000000 00000000 00000000 00000000				
0002FCH	OCFS23 [R/W] B, H, W ------11	—	OCSH23[R/W] B, H, W ---0--00	OCSL23[R/W] B, H, W 0000--00	
000300H to 00030CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000310H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314H	—	—	—	—	
000318H	—				
00031CH	—	—	—		
000320H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324H	—	—	DPVSR [R/W] H -------- 00000--0		
000328H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00032CH	—	—	DESR [R/W] H -------- 00000--0		
000330H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00033CH	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00034CH	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
000354H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00035CH	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00036CH	—	—	PACR7 [R/W] H 000000-0 00000--0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000370H	PABR8 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only product mounting MPU 12ch or 16ch) (Only the CPU can access this area)
000374H	—	—	PACR8 [R/W] H 000000-0 00000--0		
000378H	PABR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00037CH	—	—	PACR9 [R/W] H 000000-0 00000--0		
000380H	PABR10 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000384H	—	—	PACR10 [R/W] H 000000-0 00000--0		
000388H	PABR11 [R/W] ,W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00038CH	—	—	PACR11 [R/W] H 000000-0 00000--0		
000390H	PABR12 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000394H	—	—	PACR12 [R/W] H 000000-0 00000--0		
000398H	PABR13 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
00039CH	—	—	PACR13 [R/W] H 000000-0 00000--0		
0003A0H	PABR14 [R/W]W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
0003A4H	—	—	PACR14 [R/W] H 000000-0 00000--0		
0003A8H	PABR15 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
0003ACH	—	—	PACR15 [R/W] H 000000-0 00000--0		
0003B0H to 0003FCH	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000400H	ICSEL0[R/W] B, H, W -----000	ICSEL1[R/W] B, H, W -----000	ICSEL2[R/W] B, H, W -------0*1 ------00*2	ICSEL3[R/W] B, H, W -------0*1 ------00*2	Generation and clear of DMA transfer request *1:CY91F591/2/4/6/7/9 *2:CY91F59A/B
000404H	ICSEL4[R/W] B, H, W -------0	ICSEL5[R/W] B, H, W -------0	ICSEL6[R/W] B, H, W -----000	ICSEL7[R/W] B, H, W -----000	
000408H	ICSEL8[R/W] B, H, W ------00	ICSEL9[R/W] B, H, W ------00*1 -----000*2	ICSEL10[R/W] B, H, W ------00*1 -----000*2	ICSEL11[R/W] B, H, W ------00	
00040CH	ICSEL12[R/W] B, H, W ------00	ICSEL13[R/W] B, H, W -------0	ICSEL14[R/W] B, H, W -------0	ICSEL15[R/W] B, H, W --------*1 -------0*2	
000410H	ICSEL16[R/W] B, H, W --------*1 -------0*2	ICSEL17[R/W] B, H, W --------*1 -------0*2	ICSEL18[R/W] B, H, W --------*1 -------0*2	ICSEL19[R/W] B, H, W -----000	
000414H	ICSEL20[R/W] B, H, W -----000	ICSEL21[R/W] B, H, W ------00	ICSEL22[R/W] B, H, W ------00	—	
000418H	IRPR0H[R] B, H, W 00------*1 0000----*2	IRPR0L[R] B, H, W 00------*1 0000----*2	IRPR1H[R] B, H, W 00------	IRPR1L[R] B, H, W 00------	Interrupt request batch read register *1:CY91F591/2/4/6/7/9 *2:CY91F59A/B
00041CH	IRPR2H[R] B, H, W 00------	IRPR2L[R] B, H, W 00------	IRPR3H[R] B, H, W 000000--	IRPR3L[R] B, H, W 000000--	
000420H	IRPR4H[R] B, H, W 0000----*1 00000---*2	IRPR4L[R] B, H, W 0000----*1 000000--*2	IRPR5H[R] B, H, W 0000----*1 00000---*2	IRPR5L[R] B, H, W 0-------*1 000-----*2	
000424H	IRPR6H[R] B, H, W 00--0---*1 00000---*2	IRPR6L[R] B, H, W 000-----*1 0000----*2	IRPR7H[R] B, H, W -00-----*1 -0000---*2	IRPR7L[R] B, H, W ------0-*1 ------00*2	
000428H	IRPR8H[R] B, H, W 00------*1 0000----*2	IRPR8L[R] B, H, W 00------*1 0000----*2	IRPR9H[R] B, H, W 00------	IRPR9L[R] B, H, W 00------	
00042CH	IRPR10H[R] B, H, W 00------	IRPR10L[R] B, H, W 00------	IRPR11H[R] B, H, W 00------	IRPR11L[R] B, H, W 00------	Interrupt request batch read register CY91F59A/B only
000430H	IRPR12H[R] B, H, W 00------	IRPR12L[R] B, H, W 00------	IRPR13H[R] B, H, W 000-----*1 00000---*2	IRPR13L[R] B, H, W 00000---*1 0000000-*2	Interrupt request batch read register *1:CY91F591/2/4/6/7/9 *2:CY91F59A/B
000434H	IRPR14H[R] B, H, W 00000000	IRPR14L[R] B, H, W 00000000	IRPR15H[R] B, H, W 000-----*1 0000----*2	—	
000438H, 00043CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000440H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt controller [S]
000444H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
00044CH	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
00045CH	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
00046CH	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470H to 00047CH	—	—	—	—	Reserved [S]
000480H	RSTRR [R] B, H, W XXXX--XX	RSTCR [R/W] B, H, W 111----0	STBCR [R/W] B, H, W *3 000---11	—	Reset control [S] Power consumption control [S] *3: Writing to STBCR by DMA is disabled
000484H	—	—	—	—	Reserved [S]
000488H	DIVR0 [R/W] B, H, W 000-----	DIVR1 [R/W] B, H, W 0001----	DIVR2 [R/W] B, H, W 0011----	—	Clock control [S]
00048CH	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000490H	IORR0[R/W] B, H, W -0000000	IORR1[R/W] B, H, W -0000000	IORR2[R/W] B, H, W -0000000	IORR3[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
000494H	IORR4[R/W] B, H, W -0000000	IORR5[R/W] B, H, W -0000000	IORR6[R/W] B, H, W -0000000	IORR7[R/W] B, H, W -0000000	
000498H	IORR8[R/W] B, H, W -0000000	IORR9[R/W] B, H, W -0000000	IORR10[R/W] B, H, W -0000000	IORR11[R/W] B, H, W -0000000	
00049CH	IORR12[R/W] B, H, W -0000000	IORR13[R/W] B, H, W -0000000	IORR14[R/W] B, H, W -0000000	IORR15[R/W] B, H, W -0000000	
0004A0H	—	—	—	—	Reserved
0004A4H	CANPRE [R/W] B,H,W ----0000	—	—	—	CAN prescaler
0004A8H	CPCLR6 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 6 CY91F59A/B only
0004ACH	TCDT6 [R/W] W 00000000 00000000 00000000 00000000				
0004B0H	TCCSH6 [R/W] B, H, W 0-----00	TCCSL6 [R/W] B, H, W -1-00000	—		
0004B4H	—	—	—	—	Reserved
0004B8H	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration (Calibration)
0004BCH	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
0004C0H	—	—	—	—	
0004C4H	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		
0004C8H	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
0004CCH	CRTR [R/W] B,H,W 01111111	—	—	—	RC trimming setting register
0004D0H	CPCLR7 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 7 CY91F59A/B only
0004D4H	TCDT7 [R/W] W 00000000 00000000 00000000 00000000				
0004D8H	TCCSH7 [R/W] B, H, W 0-----00	TCCSL7 [R/W] B, H, W -1-00000	—		
0004DCH	—	—	—	—	Reserved
0004E0H	SCR8 [R/W] B,H,W 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R/W] B,H,W 0-000011	ESCR8 [R/W] B,H,W -0000000	Multi-function serial 8 *1: Byte access is possible only for access to lower 8 bits. CY91F59A/B only
0004E4H	RDR8/(TDR8)[R/W] B,H,W *1 -------0 00000000		BGR8 [R/W] H,W 00000000 00000000		
0004E8H	—	—	—	—	
0004ECH	FCR18 [R/W] B,H,W ---00100	FCR08 [R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0004F0H	SCR9 [R/W] B,H,W 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R/W] B,H,W 0-000011	ESCR9 [R/W] B,H,W -0000000	Multi-function serial 9 *1: Byte access is possible only for access to lower 8 bits. CY91F59A/B only
0004F4H	RDR9/(TDR9)[R/W] B,H,W *1 -------0 00000000		BGR9 [R/W] H,W 00000000 00000000		
0004F8H	—	—	—	—	
0004FCH	FCR19 [R/W] B,H,W ---00100	FCR09 [R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
000500H to 00050CH	—	—	—	—	Reserved
000510H	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514H	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518H	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset [S]
00051CH	—	—	—	—	Reserved [S]
000520H	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524H	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528H	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		Clock control 2
00052CH	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530H	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534H	—	—	—	—	
000538H	—	—	—	—	
00053CH	—	—	—	—	
000540H to 00054CH	—	—	—	—	Reserved
000550H	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554H	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558H	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00055C$_H$	—	—	WTDR[R/W] H 00000000 00000000		Real-time clock
000560$_H$	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564$_H$	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568$_H$	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C$_H$	—	CSVCR [R/W] B -001110- -001010-*4	—	—	Clock supervisor *4: An initial value is different by part number. For details, see the CSVCR register in chapter "Clock Supervisor"
000570$_H$ to 00057C$_H$	—	—	—	—	Reserved
000580$_H$	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator control
000584$_H$	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 0-100--1	LVD [R/W] B,H,W 01000--0	—	Low-power detection
000588$_H$	GLVD5R[R/W] B,H,W 0-01-0-X	GLVD5F[R/W] B,H,W 0-0100-X	GLVD[R/W] B,H,W 010000-X	—	
00058C$_H$	—	—	—	—	Reserved
000590$_H$	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594$_H$	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598$_H$	GSTR[R] B,H,W 0-------	GCTLR[R/W] B,H,W 0000-111	—	—	
00059C$_H$	—	—	—	—	
0005A0$_H$ to 0005FC$_H$	—	—	—	—	Reserved
000600$_H$ to 00060C$_H$	—	—	—	—	Reserved[S]
000610$_H$ to 00063C$_H$	—	—	—	—	Reserved[S]
000640$_H$ to 00064C$_H$	—	—	—	—	Reserved[S]
000650$_H$ to 00067C$_H$	—	—	—	—	Reserved[S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000680H to 00068CH	—	—	—	—	Reserved[S]
000690H to 0006BCH	—	—	—	—	Reserved[S]
0006C0H to 0006CCH	—	—	—	—	Reserved[S]
0006D0H to 0006F0H	—	—	—	—	Reserved
0006F4 H	—	—	—	—	Reserved
0006F8H to 00070CH	—	—	—	—	Reserved
000710H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	—	Bus performance counter
000714H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
00071CH	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720H to 0007F8H	—	—	—	—	Reserved
0007FCH	BMODR[R] B, H, W XXXXXXXX	—	—	—	Operation mode
000800H to 00083CH	—	—	—	—	Reserved [S]
000840H	FCTLR[R/W] H -0--1000 0--0----		—	FSTR[R/W] B -----001	Flash memory register [S]
000844H to 000854H	—	—	—	—	Reserved [S]
000858H	—	—	WREN[R/W] H 00000000 00000000		Wild register [S]
00085CH to 00087CH	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000880_H	WRAR00[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				Wild register [S]
000884_H	WRDR00[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000888_H	WRAR01[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00088C_H$	WRDR01[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000890_H	WRAR02[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
000894_H	WRDR02[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000898_H	WRAR03[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
$00089C_H$	WRDR03[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0008A0_H$	WRAR04[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0008A4H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
0008A8H	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008ACH	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0H	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008B4H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8H	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008BCH	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0H	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008C4H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8H	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008CCH	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0H	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008D4H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8H	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008DCH	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0H	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008E4H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8H	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008ECH	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0H	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008F4H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8H	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008FCH	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900H to 000BF8H	—	—	—	—	Reserved
000BFCH	—	—	UER [W] B,H,W -------- -------X		OCDU

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000C00H	DCCR0[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C04H	DCSR0[R/W] H 0------- -----000		DTCR0[R/W] H 00000000 00000000		
000C08H	DSAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C0CH	DDAR0[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C10H	DCCR1[R/W] W 0----000 --00--00 00000000 0-000000				
000C14H	DCSR1[R/W] H 0------- -----000		DTCR1[R/W] H 00000000 00000000		
000C18H	DSAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C1CH	DDAR1[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C20H	DCCR2[R/W] W 0----000 --00--00 00000000 0-000000				
000C24H	DCSR2[R/W] H 0------- -----000		DTCR2[R/W] H 00000000 00000000		
000C28H	DSAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C2CH	DDAR2[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C30H	DCCR3[R/W] W 0----000 --00--00 00000000 0-000000				
000C34H	DCSR3[R/W] H 0------- -----000		DTCR3[R/W] H 00000000 00000000		
000C38H	DSAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C3CH	DDAR3[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C40H	DCCR4[R/W] W 0----000 --00--00 00000000 0-000000				
000C44H	DCSR4[R/W] H 0------- -----000		DTCR4[R/W] H 00000000 00000000		
000C48H	DSAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C4CH	DDAR4[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000C50H	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
000C54H	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
000C58H	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C5CH	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C60H	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
000C64H	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
000C68H	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C6CH	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C70H	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
000C74H	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
000C78H	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C7CH	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C80H	DCCR8[R/W] W 0----000 --00--00 00000000 0-000000				
000C84H	DCSR8[R/W] H 0------- -----000		DTCR8[R/W] H 00000000 00000000		
000C88H	DSAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C8CH	DDAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C90H	DCCR9[R/W] W 0----000 --00--00 00000000 0-000000				
000C94H	DCSR9[R/W] H 0------- -----000		DTCR9[R/W] H 00000000 00000000		
000C98H	DSAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000C9CH	DDAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CA0H	DCCR10[R/W] W 0----000 --00--00 00000000 0-000000				
000CA4H	DCSR10[R/W] H 0------- -----000		DTCR10[R/W] H 00000000 00000000		
000CA8H	DSAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000CAC$_H$	DDAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
000CB0$_H$	DCCR11[R/W] W 0----000 --00--00 00000000 0-000000				
000CB4$_H$	DCSR11[R/W] H 0------- -----000		DTCR11[R/W] H 00000000 00000000		
000CB8$_H$	DSAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CBC$_H$	DDAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CC0$_H$	DCCR12[R/W] W 0----000 --00--00 00000000 0-000000				
000CC4$_H$	DCSR12[R/W] H 0------- -----000		DTCR12[R/W] H 00000000 00000000		
000CC8$_H$	DSAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CCC$_H$	DDAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CD0$_H$	DCCR13[R/W] W 0----000 --00--00 00000000 0-000000				
000CD4$_H$	DCSR13[R/W] H 0------- -----000		DTCR13[R/W] H 00000000 00000000		
000CD8$_H$	DSAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CDC$_H$	DDAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE0$_H$	DCCR14[R/W] W 0----000 --00--00 00000000 0-000000				
000CE4$_H$	DCSR14[R/W] H 0------- -----000		DTCR14[R/W] H 00000000 00000000		
000CE8$_H$	DSAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CEC$_H$	DDAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CF0$_H$	DCCR15[R/W] W 0----000 --00--00 00000000 0-000000				
000CF4$_H$	DCSR15[R/W] H 0------- -----000		DTCR15[R/W] H 00000000 00000000		
000CF8$_H$	DSAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CFC$_H$	DDAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00$_H$ to 000DF0$_H$	—	—	—	—	Reserved [S]
000DF4$_H$	—	—	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	DMA controller [S]
000DF8$_H$	DMACR[R/W] W 0------- -------- 0------- --------				
000DFC$_H$	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E00H	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
000E04H	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
000E08H	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
000E0CH	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
000E10H	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
000E14H	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
000E18H to 000E1CH	—	—	—	—	Reserved
000E20H	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
000E24H	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
000E28H	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
000E2CH	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
000E30H	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
000E34H	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	
000E38H to 000E3CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E40H	PDDR00[R] B,H,W XXXXXXXX	PDDR01[R] B,H,W XXXXXXXX	PDDR02[R] B,H,W XXXXXXXX	PDDR03[R] B,H,W XXXXXXXX	Input data direct read register
000E44H	PDDR04[R] B,H,W XXXXXXXX	PDDR05[R] B,H,W XXXXXXXX	PDDR06[R] B,H,W XXXXXXXX	PDDR07[R] B,H,W XXXXXXXX	
000E48H	PDDR08[R] B,H,W XXXXXXXX	PDDR09[R] B,H,W XXXXXXXX	PDDR10[R] B,H,W XXXXXXXX	PDDR11[R] B,H,W XXXXXXXX	
000E4CH	PDDR12[R] B,H,W XXXXXXXX	PDDR13[R] B,H,W XX-XXXXX	—	—	
000E50H	PDDRA[R] B,H,W XXXXXX--	PDDRB[R] B,H,W XXXXXX--	PDDRC[R] B,H,W XXXXXX--	PDDRD[R] B,H,W XXXXXX--	
000E54H	PDDRE[R] B,H,W XXXXXX--	PDDRF[R] B,H,W XXXXXX--	PDDRG[R] B,H,W XXXXXXXX	PDDRH[R] B,H,W ----X---	
000E58H to 000E5CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E60H	EPFR00[R/W] B,H,W 00000000	EPFR01[R/W] B,H,W ----0000*1 00000000*2	EPFR02[R/W] B,H,W ---00000	EPFR03[R/W] B,H,W ---00000	Extended port function register *1:CY91F591/2/4/6/7/9 *2:CY91F59A/B
000E64H	EPFR04[R/W] B,H,W ---00000	EPFR05[R/W] B,H,W ---00000	EPFR06[R/W] B,H,W ---00000	EPFR07[R/W] B,H,W ---00000	
000E68H	EPFR08[R/W] B,H,W ---00000	EPFR09[R/W] B,H,W ---00000	EPFR10[R/W] B,H,W -0000000	EPFR11[R/W] B,H,W --000000	
000E6CH	EPFR12[R/W] B,H,W --000000	EPFR13[R/W] B,H,W --000000	EPFR14[R/W] B,H,W --000000	EPFR15[R/W] B,H,W -0000000	
000E70H	EPFR16[R/W] B,H,W 00000000	EPFR17[R/W] B,H,W 00000000	EPFR18[R/W] B,H,W 10000000	EPFR19[R/W] B,H,W 11111111	
000E74H	EPFR20[R/W] B,H,W -1111111	EPFR21[R/W] B,H,W 00000000	EPFR22[R/W] B,H,W 00000000	EPFR23[R/W] B,H,W 00000000	
000E78H	EPFR24[R/W] B,H,W -----000	EPFR25[R/W] B,H,W -----000	EPFR26[R/W] B,H,W ----0000	EPFR27[R/W] B,H,W ---00000	
000E7CH	EPFR28[R/W] B,H,W ------00	EPFR29[R/W] B,H,W 00000000	EPFR30[R/W] B,H,W 00000000	EPFR31[R/W] B,H,W 00000000	
000E80H	EPFR32[R/W] B,H,W 00000000	EPFR33[R/W] B,H,W ---00000	EPFR34[R/W] B,H,W ---00000	EPFR35[R/W] B,H,W ---00000	
000E84H	EPFR36[R/W] B,H,W ---00000	EPFR37[R/W] B,H,W 00000000	EPFR38[R/W] B,H,W ---00000	EPFR39[R/W] B,H,W 00000000	
000E88H	EPFR40[R/W] B,H,W --000000	EPFR41[R/W] B,H,W -----000	EPFR42[R/W] B,H,W ------00	EPFR43[R/W] B,H,W 00000000	
000E8CH	EPFR44[R/W] B,H,W 00000000	EPFR45[R/W] B,H,W 00000000	EPFR46[R/W] B,H,W --000000	EPFR47[R/W] B,H,W -------0	
000E90H	EPFR48[R/W] B,H,W 00000000	EPFR49[R/W] B,H,W 00000000	EPFR50[R/W] B,H,W 00000000	EPFR51[R/W] B,H,W ---00000	
000E94H	EPFR52[R/W] B,H,W -----000	EPFR53[R/W] B,H,W ---00000	EPFR54[R/W] B,H,W ----0000	EPFR55[R/W] B,H,W ------01	
000E98H	EPFR56[R/W] B,H,W --000000	EPFR57[R/W] B,H,W --000000	EPFR58[R/W] B,H,W ----0000	—	Extended port function register CY91F59A/B only
000E9CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000EA0$_H$	PPCR00[R/W] B,H,W 11111111	PPCR01[R/W] B,H,W 11111111	PPCR02[R/W] B,H,W 11111111	PPCR03[R/W] B,H,W 11111111	Port pull-up/down control register
000EA4$_H$	PPCR04[R/W] B,H,W 11111111	PPCR05[R/W] B,H,W 11111111	PPCR06[R/W] B,H,W 11111111	PPCR07[R/W] B,H,W 11111111	
000EA8$_H$	PPCR08[R/W] B,H,W 11111111	PPCR09[R/W] B,H,W 11111111	PPCR10[R/W] B,H,W 11111111	PPCR11[R/W] B,H,W 11111111	
000EAC$_H$	PPCR12[R/W] B,H,W 11111111	PPCR13[R/W] B,H,W 11-11111	—	—	
000EB0$_H$	PPCRA[R/W] B,H,W 111111--	PPCRB[R/W] B,H,W 111111--	PPCRC[R/W] B,H,W 111111--	PPCRD[R/W] B,H,W 111111--	
000EB4$_H$	PPCRE[R/W] B,H,W 111111--	PPCRF[R/W] B,H,W 111111--	PPCRG[R/W] B,H,W 11111111	PPCRH[R/W] B,H,W ----1---	
000EB8$_H$ to 000EBC$_H$	—	—	—	—	Reserved
000EC0$_H$	PPER00[R/W] B,H,W 00000000	PPER01[R/W] B,H,W 00000000	PPER02[R/W] B,H,W 00000000	PPER03[R/W] B,H,W 00000000	Port pull-up/down enable register
000EC4$_H$	PPER04[R/W] B,H,W 00000000	PPER05[R/W] B,H,W 00000000	PPER06[R/W] B,H,W 00000000	PPER07[R/W] B,H,W 00000000	
000EC8$_H$	PPER08[R/W] B,H,W 00000000	PPER09[R/W] B,H,W 00000000	PPER10[R/W] B,H,W 00000000	PPER11[R/W] B,H,W 00000000	
000ECC$_H$	PPER12[R/W] B,H,W 00000000	PPER13[R/W] B,H,W 00-00000	—	—	
000ED0$_H$	PPERA[R/W] B,H,W 000000--	PPERB[R/W] B,H,W 000000--	PPERC[R/W] B,H,W 000000--	PPERD[R/W] B,H,W 000000--	
000ED4$_H$	PPERE[R/W] B,H,W 000000--	PPERF[R/W] B,H,W 000000--	PPERG[R/W] B,H,W 00000000	PPERH[R/W] B,H,W ----0---	
000ED8$_H$ to 000EDC$_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000EE0H	PILR00[R/W] B,H,W 11111111	PILR01[R/W] B,H,W 11111111	PILR02[R/W] B,H,W 11111111	PILR03[R/W] B,H,W 11111111	Port input level selection register
000EE4H	PILR04[R/W] B,H,W 11111111	PILR05[R/W] B,H,W 11111111	PILR06[R/W] B,H,W 11111111	PILR07[R/W] B,H,W 11111111	
000EE8H	PILR08[R/W] B,H,W 11111111	PILR09[R/W] B,H,W 11111111	PILR10[R/W] B,H,W 11111111	PILR11[R/W] B,H,W 11111111	
000EECH	PILR12[R/W] B,H,W 11111111	PILR13[R/W] B,H,W 11-11111	—	—	
000EF0H	PILRA[R/W] B,H,W 111111--	PILRB[R/W] B,H,W 111111--	PILRC[R/W] B,H,W 111111--	PILRD[R/W] B,H,W 111111--	
000EF4H	PILRE[R/W] B,H,W 111111--	PILRF[R/W] B,H,W 111111--	PILRG[R/W] B,H,W 11111111	PILRH[R/W] B,H,W ----1---	
000EF8H to 000EFCH	—	—	—	—	Reserved
000F00H	—	—	—	—	Extended Port input level selection register
000F04H	—	—	EPILR06[R/W] B,H,W 00000000	EPILR07[R/W] B,H,W 00000000	
000F08H	EPILR08[R/W] B,H,W 00000000	EPILR09[R/W] B,H,W 00000000	EPILR10[R/W] B,H,W 00000000	EPILR11[R/W] B,H,W 00000000	
000F0CH	EPILR12[R/W] B,H,W 00000000	EPILR13[R/W] B,H,W 00-00000	—	—	
000F10H	—	—	—	—	
000F14H	—	—	—	—	
000F18H to 000F1CH	—	—	—	—	Reserved
000F20H	—	—	—	—	Port output drive register
000F24H	—	—	PODR06[R/W] B,H,W 00000000	PODR07[R/W] B,H,W 00000000	
000F28H	PODR08[R/W] B,H,W 00000000	PODR09[R/W] B,H,W 00000000	PODR10[R/W] B,H,W 00000000	PODR11[R/W] B,H,W 00000000	
000F2CH	PODR12[R/W] B,H,W 00000000	PODR13[R/W] B,H,W 00-00000	—	—	
000F30H	—	—	—	—	
000F34H	—	—	—	—	
000F38H	EPODR06[R/W] B,H,W 00000000	EPODR07[R/W] B,H,W 00000000	EPODR08[R/W] B,H,W 00000000	—	Extended Port output drive register
000F3CH	EPODRGD [R/W]B,H,W ----1010	EPODRGF [R/W]B,H,W --101010	—	—	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000F40H	PORTEN [R/W] B,H,W -------0	—	—	—	Port input enable register
000F44H to 000F4CH	—	—	—	—	Reserved
000F50H	—	GPLLCR[R/W] B,H,W 0------0	PTIMCR[R/W] B,H,W ----1111	PEDIVCR[R/W] B,H,W -000-000	GDC control register
000F54H	—	PDIVCR[R/W] B,H,W -0000000	SDIVCR0[R/W] B,H,W --000000	SDIVCR1[R/W] B,H,W ---00000	
000F58H	—	SSSCR0[R/W] B,H,W ----0000	SSSCR1[R/W] H,W 000----- --------		
000F5CH	—	PGRCR0[R/W] B,H,W 00----00	PGRCR1[R/W] B,H,W 00000000	PGRCR2[R/W] B,H,W 00000000	
000F60H	—	SGRCR0[R/W] B,H,W 00----00	SGRCR1[R/W] B,H,W 00000000	SGRCR2[R/W] B,H,W 00000000	
000F64H	—	GDCCR[R/W] B,H,W --000001	GDCTRGR [R/W] B,H,W 0000--00	GDCSWPR [R/W] B,H,W ---00101	
000F68H to 000F6CH	—	—	—	—	Reserved
000F70H	RCRH0[W] H,W XXXXXXXX	RCRL0[W] B,H,W XXXXXXXX	UDCRH0[R] H,W 00000000	UDCRL0[R] B,H,W 00000000	Up/down counter 0 CY91F59A/B only
000F74H	CCR0[R/W] B,H 00000000 -0001000		—	CSR0[R/W] B 00000000	
000F78H to 000F7CH	—	—	—	—	Reserved
000F80H	RCRH1[W] H,W XXXXXXXX	RCRL1[W] B,H,W XXXXXXXX	UDCRH1[R] H,W 00000000	UDCRL1[R] B,H,W 00000000	Up/down counter 1 CY91F59A/B only
000F84H	CCR1[R/W] B,H 00000000 -0001000		—	CSR1[R/W] B 00000000	
000F88H to 000F9CH	—	—	—	—	Reserved
000FA0H	CPCLR2 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 2
000FA4H	TCDT2 [R/W] W 00000000 00000000 00000000 00000000				
000FA8H	TCCSH2 [R/W] B, H, W 0-----00	TCCSL2 [R/W] B, H, W -1-00000	—		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000FAC$_H$	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 3
000FB0$_H$	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000FB4$_H$	TCCSH3 [R/W] B, H, W 0-----00	TCCSL3 [R/W] B, H, W -1-00000	—		
000FB8$_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 4 CY91F59A/B only
000FBC$_H$	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000FC0$_H$	TCCSH4 [R/W] B, H, W 0-----00	TCCSL4 [R/W] B, H, W -1-00000	—		
000FC4$_H$	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 5 CY91F59A/B only
000FC8$_H$	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FCC$_H$	TCCSH5 [R/W] B, H, W 0-----00	TCCSL5 [R/W] B, H, W -1-00000	—		
000FD0$_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 6,7 *1:CY91F591/2/4/6/7/9 *2:CY91F59A/B
000FD4$_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8$_H$	ICFS67 [R/W] B, H, W ------00	—	LSYNS1 [R/W] B,H,W ------00*1 --000000*2	ICS67 [R/W] B, H, W 00000000	
000FDC$_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 CY91F59A/B only
000FE0$_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4$_H$	ICFS89 [R/W] B, H, W ------00	—	—	ICS89 [R/W] B, H, W 00000000	
000FE8$_H$	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 10,11 CY91F59A/B only
000FEC$_H$	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0$_H$	ICFS1011 [R/W] B, H, W ------00	—	—	ICS1011 [R/W] B, H, W 00000000	
000FF4$_H$	RCRH2[W] H,W XXXXXXXX	RCRL2[W] B,H,W XXXXXXXX	UDCRH2[R] H,W 00000000	UDCRL2[R] B,H,W 00000000	Up/down counter 2 CY91F59A/B only
000FF8$_H$	CCR2[R/W] B,H 00000000 -0001000		—	CSR2[R/W] B 00000000	
000FFC$_H$	—	—	—	—	Reserved
001000$_H$	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Synchronous/asynchronous switching control
001004$_H$ to 00103C$_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
001040H	—	SGDER0[R/W] B,H,W 00000000	SGCR0[R/W] B,H,W -0000-0- 000--000		Sound generator 0
001044H	SGAR0[R/W] B,H,W 00000000 00000000		SGFR0[R/W] B,H,W 00000000	SGNR0[R/W] B,H,W 00000000	
001048H	SGTCR0[R/W] B,H,W 00000000	SGIDR0[R/W] B,H,W 00000000	SGPCR0[R/W] B,H,W 00000000 11111111		
00104CH	SGDMAR0[W] B,H,W 00000000 00000000 00000000 00000000				
001050H to 00105CH	—	—	—	—	Reserved
001060H	—	SGDER1[R/W] B,H,W 00000000	SGCR1[R/W] B,H,W -0000-0- 000--000		Sound generator 1
001064H	SGAR1[R/W] B,H,W 00000000 00000000		SGFR1[R/W] B,H,W 00000000	SGNR1[R/W] B,H,W 00000000	
001068H	SGTCR1[R/W] B,H,W 00000000	SGIDR1[R/W] B,H,W 00000000	SGPCR1[R/W] B,H,W 00000000 11111111		
00106CH	SGDMAR1[W] B,H,W 00000000 00000000 00000000 00000000				
001070H to 00107CH	—	—	—	—	Reserved
001080H	—	SGDER2[R/W] B,H,W 00000000	SGCR2[R/W] B,H,W -0000-0- 000--000		Sound generator 2
001084H	SGAR2[R/W] B,H,W 00000000 00000000		SGFR2[R/W] B,H,W 00000000	SGNR2[R/W] B,H,W 00000000	
001088H	SGTCR2[R/W] B,H,W 00000000	SGIDR2[R/W] B,H,W 00000000	SGPCR2[R/W] B,H,W 00000000 11111111		
00108CH	SGDMAR2[W] B,H,W 00000000 00000000 00000000 00000000				
001090H to 00109CH	—	—	—	—	Reserved
0010A0H	—	SGDER3[R/W] B,H,W 00000000	SGCR3[R/W] B,H,W -0000-0- 000--000		Sound generator 3
0010A4H	SGAR3[R/W] B,H,W 00000000 00000000		SGFR3[R/W] B,H,W 00000000	SGNR3[R/W] B,H,W 00000000	
0010A8H	SGTCR3[R/W] B,H,W 00000000	SGIDR3[R/W] B,H,W 00000000	SGPCR3[R/W] B,H,W 00000000 11111111		
0010ACH	SGDMAR3[W] B,H,W 00000000 00000000 00000000 00000000				
0010B0H to 0010BCH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0010C0H	—	SGDER4[R/W] B,H,W 00000000	SGCR4[R/W] B,H,W -0000-0- 000--000		Sound generator 4
0010C4H	SGAR4[R/W] B,H,W 00000000 00000000		SGFR4[R/W] B,H,W 00000000	SGNR4[R/W] B,H,W 00000000	
0010C8H	SGTCR4[R/W] B,H,W 00000000	SGIDR4[R/W] B,H,W 00000000	SGPCR4[R/W] B,H,W 00000000 11111111		
0010CCH	SGDMAR4[W] B,H,W 00000000 00000000 00000000 00000000				
0010D0H to 00112CH	—	—	—	—	Reserved
001130H	—	—	—	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
001134H	CRCINIT[R/W] B,H,W 1111111 1111111 1111111 1111111				
001138H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
00113CH	CRCR[R] B,H,W 1111111 1111111 1111111 1111111				
001140H to 0013FCH	—	—	—	—	Reserved
001400H to 001FFCH	—	—	—	—	Reserved (3KB)

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002000H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN0 (64msg)
002004H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008H	INTR0 [R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
00200CH	BRPER0 [R/W] B,H,W -------- ----0000		—		
002010H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
00201CH	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—		
002020H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028H, 00202CH	Reserved				
002030H, 002034H	Reserved (IF1 data mirror)				
002038H, 00203CH	Reserved				
002040H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
00204CH	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002050H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		CAN0 (64msg)
002054H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058H, 00205CH	Reserved				
002060H, 002064H	Reserved (IF2 data mirror)				
002068H to 00207CH	Reserved				
002080H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088H	—		—		
00208CH	—		—		
002090H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R]B,H,W 00000000 00000000		
002098H	—		—		
00209CH	—		—		
0020A0H	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
0020A4H	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
0020A8 H	—		—		
0020ACH	—		—		
0020B0H	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
0020B4H	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
0020B8H	—		—		
0020BCH	—		—		
0020C0H to 0020FCH	Reserved				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002100H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN1 (32msg)
002104H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108H	INTR1 [R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
00210CH	BRPER1 [R/W] B,H,W -------- ----0000		—		
002110H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
00211CH	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—		
002120H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128H, 00212CH	Reserved				
002130H, 002134H	Reserved (IF1 data mirror)				
002138H, 00213CH	Reserved				
002140H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00214C$_H$	IF2MCTR1 [R/W] B,H,W 00000000 0---0000		—		CAN1 (32msg)
002150$_H$	IF2DTA11 [R/W] B,H,W 00000000 00000000		IF2DTA21 [R/W] B,H,W 00000000 00000000		
002154$_H$	IF2DTB11 [R/W] B,H,W 00000000 00000000		IF2DTB21 [R/W] B,H,W 00000000 00000000		
002158$_H$, 00215C$_H$	Reserved				
002160$_H$, 002164$_H$	Reserved (IF2 data mirror)				
002168$_H$ to 00217C$_H$	Reserved				
002180$_H$	TREQR21 [R] B,H,W 00000000 00000000		TREQR11 [R] B,H,W 00000000 00000000		
002184$_H$	—		—		
002188$_H$	—		—		
00218C$_H$	—		—		
002190$_H$	NEWDT21 [R] B,H,W 00000000 00000000		NEWDT11 [R] B,H,W 00000000 00000000		
002194$_H$	—		—		
002198$_H$	—		—		
00219C$_H$	—		—		
0021A0$_H$	INTPND21 [R] B,H,W 00000000 00000000		INTPND11 [R] B,H,W 00000000 00000000		
0021A4$_H$	—		—		
0021A8$_H$	—		—		
0021AC$_H$	—		—		
0021B0$_H$	MSGVAL21 [R] B,H,W 00000000 00000000		MSGVAL11 [R] B,H,W 00000000 00000000		
0021B4$_H$	—		—		
0021B8$_H$	—		—		
0021BC$_H$	—		—		
0021C0$_H$ to 0021FC$_H$	Reserved				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002200H	CTRLR2 [R/W] B,H,W -------- 000-0001		STATR2[R/W] B,H,W -------- 00000000		CAN2 (32msg)
002204H	ERRCNT2[R] B,H,W 00000000 00000000		BTR2[R/W] B,H,W -0100011 00000001		
002208H	INTR2[R] B,H,W 00000000 00000000		TESTR2[R/W] B,H,W -------- X00000--		
00220CH	BRPER2 [R/W] B,H,W -------- ----0000		—		
002210H	IF1CREQ2[R/W] B,H,W 0------- 00000001		IF1CMSK2[R/W] B,H,W -------- 00000000		
002214H	IF1MSK22 [R/W] B,H,W 11-11111 11111111		IF1MSK12 [R/W] B,H,W 11111111 11111111		
002218H	IF1ARB22 [R/W] B,H,W 00000000 00000000		IF1ARB12 [R/W] B,H,W 00000000 00000000		
00221CH	IF1MCTR2[R/W] B,H,W 00000000 0---0000		—		
002220H	IF1DTA12 [R/W] B,H,W 00000000 00000000		IF1DTA22 [R/W] B,H,W 00000000 00000000		
002224H	IF1DTB12 [R/W] B,H,W 00000000 00000000		IF1DTB22 [R/W] B,H,W 00000000 00000000		
002228 H, 00222CH	Reserved				
002230 H, 002234H	Reserved (IF1 data mirror)				
002238H, 00223CH	Reserved				
002240H	IF2CREQ2[R/W] B,H,W 0------- 00000001		IF2CMSK2[R/W] B,H,W -------- 00000000		
002244H	IF2MSK22 [R/W] B,H,W 11-11111 11111111		IF2MSK12[R/W] B,H,W 11111111 11111111		
002248H	IF2ARB22[R/W] B,H,W 00000000 00000000		IF2ARB12[R/W] B,H,W 00000000 00000000		
00224CH	IF2MCTR2[R/W] B,H,W 00000000 0---0000		—		
002250H	IF2DTA12[R/W] B,H,W 00000000 00000000		IF2DTA22[R/W] B,H,W 00000000 00000000		
002254H	IF2DTB12[R/W] B,H,W 00000000 00000000		IF2DTB22[R/W] B,H,W 00000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002258H, 00225CH	Reserved				CAN2 (32msg)
002260H, 002264H	Reserved (IF2 data mirror)				
002268H to 00227CH	Reserved				
002280H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284H	—		—		
002288H	—		—		
00228CH	—		—		
002290 H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294H	—		—		
002298H	—		—		
00229CH	—		—		
0022A0H	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
0022A4H	—		—		
0022A8H	—		—		
0022ACH	—		—		
0022B0H	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
0022B4H	—		—		
0022B8H	—		—		
0022BCH	—		—		
0022C0H to 0022FCH	—	—	—	—	Reserved
002300H	DFCTLR[R/W]B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304H	—	—	—	—	
002308H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	
00230CH to 0023FCH	—	—	—	—	Reserved
002400H	SEEARX[R] B,H,W 00000000 00000000		DEEARX[R] B,H,W 00000000 00000000		XBS RAM ECC control register
002404H	EECSRX [R/W] B,H,W ----0000	—	EFEARX[R/W] B,H,W 00000000 00000000		
002408H	—	EFECRX[R/W] B,H,W -------0 00000000 00000000			
00240CH to 0024FCH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002500H	SEEARH[R] B,H,W --000000 00000000		DEEARH[R] B,H,W --000000 00000000		AHB RAM ECC control register CY91F59A/B only
002504H	EECSRH[R/W] B,H,W ----0000	—	EFEARH[R/W]B,H,W --000000 00000000		
002508H	—	EFECRH[R/W]B,H,W -------0 00000000 00000000			
00250CH to 002FFCH	—	—	—	—	Reserved
003000H	SEEARA[R] B,H,W -----000 00000000		DEEARA[R] B,H,W -----000 00000000		Backup RAM ECC control register
003004H	EECSRA [R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W -----000 00000000		
003008H	—	EFECRA[R/W] B,H,W -------0 00000000 00000000			
00300CH to 003FFCH	—	—	—	—	Reserved
004000H to 005FFCH	Backup RAM				Backup RAM area
006000H to 00EFFCH	—	—	—	—	Reserved
00F000H to 00FEFCH	—	—	—	—	Reserved [S]
00FF00H	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
00FF04H to 00FF0CH	—	—	—	—	Reserved [S]
00FF10H	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FF14H	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00FF18H to 00FFF4H	—	—	—	—	Reserved [S]
00FFF8H	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
00FFFCH	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]:It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

■ Interrupt vector

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN*1
	Decimal	Hexa-Decimal				
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	06	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	07	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	08	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System Reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System Reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System Reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request/ XBS RAM double-bit error generation/ AHB RAM double-bit error generation**/ Backup RAM double-bit error generation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1
Reload timer 0/1/7**/8**	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2
Reload timer 2/3/9**/10**	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3
Multi-function serial interface ch.0 (reception completed)/ Multi-function serial interface ch.0(status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*2
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5
Multi-function serial interface ch.1 (reception completed)/ Multi-function serial interface ch.1(status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*2
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7
LIN-UART2(reception completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8
LIN-UART2(transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9
LIN-UART3(reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10
LIN-UART3(transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
LIN-UART4(reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12
LIN-UART4(transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
LIN-UART5(reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14
LIN-UART5(transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
LIN-UART6(reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16
LIN-UART6(transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2/UDC0**/1**	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN*1
	Decimal	Hexa-Decimal				
Sound generator 0 / LIN-UART7 (reception completed)	38	26	ICR22	364_H	$000FFF64_H$	22
Sound generator 1 / LIN-UART7 (transmission completed)	39	27	ICR23	360_H	$000FFF60_H$	23
PPG0/1/10/11/20/21	40	28	ICR24	$35C_H$	$000FFF5C_H$	24
PPG2/3/12/13/22/23	41	29	ICR25	358_H	$000FFF58_H$	25
PPG4/5/14/15/UDC2**	42	2A	ICR26	354_H	$000FFF54_H$	26*6
PPG6/7/16/17/Multi-function serial interface ch.10 (reception completed)**/ Multi-function serial interface ch.10(status)**	43	2B	ICR27	350_H	$000FFF50_H$	27
PPG8/9/18/19/ Multi-function serial interface ch.10 (transmission completed)**	44	2C	ICR28	$34C_H$	$000FFF4C_H$	28
GDC/GDC_ALM/GDC_LVD/Multi-function serial interface ch.8 (reception completed)**/ Multi-function serial interface ch.8(status)**	45	2D	ICR29	348_H	$000FFF48_H$	29*7
Main timer/Sub timer/PLL timer/ Multi-function serial interface ch.8 (transmission completed)**	46	2E	ICR30	344_H	$000FFF44_H$	30
Clock calibration unit (Sub oscillation) / Sound generator 4/Multi-function serial interface ch.9 (reception completed)**/ Multi-function serial interface ch.9(status)**	47	2F	ICR31	340_H	$000FFF40_H$	31*3
A/D converter	48	30	ICR32	$33C_H$	$000FFF3C_H$	32
Clock calibration Unit (CR oscillation) / Multi-function serial interface ch.9 (transmission completed)**	49	31	ICR33	338_H	$000FFF38_H$	33*3
Free-run timer 0/2/4**/6**	50	32	ICR34	334_H	$000FFF34_H$	-
Free-run timer 1/3/5**/7**	51	33	ICR35	330_H	$000FFF30_H$	-
ICU0/6(fetching)	52	34	ICR36	$32C_H$	$000FFF2C_H$	36
ICU1/7(fetching)	53	35	ICR37	328_H	$000FFF28_H$	37
ICU2/8** (fetching)	54	36	ICR38	324_H	$000FFF24_H$	38
ICU3/9** (fetching)	55	37	ICR39	320_H	$000FFF20_H$	39
ICU4/10** (fetching)	56	38	ICR40	$31C_H$	$000FFF1C_H$	40
ICU5/11** (fetching)	57	39	ICR41	318_H	$000FFF18_H$	41
OCU0/1(match)	58	3A	ICR42	314_H	$000FFF14_H$	42
OCU2/3(match)	59	3B	ICR43	310_H	$000FFF10_H$	43
Base timer 0 IRQ0 / Base timer 0 IRQ1 / Sound generator 2/Multi-function serial interface ch.11 (reception completed)**/ Multi-function serial interface ch.11(status)**	60	3C	ICR44	$30C_H$	$000FFF0C_H$	44
Base timer 1 IRQ0 / Base timer 1 IRQ1/ Sound generator3 / XBS RAM single bit error generation / AHB RAM single bit error generation**/ Backup RAM single bit error generation/ Multi-function serial interface ch.11 (transmission completed)**	61	3D	ICR45	308_H	$000FFF08_H$	45*4
DMAC0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15	62	3E	ICR46	304_H	$000FFF04_H$	-
Delay interrupt	63	3F	ICR47	300_H	$000FFF00_H$	-
System Reserved (Used for REALOS™*5.)	64	40	-	$2FC_H$	$000FFEFC_H$	-
System Reserved (Used for REALOS.)	65	41	-	$2F8_H$	$000FFEF8_H$	-
Used with the INT instruction.	66 | 255	42 | FF	-	$2F4_H$ | 000_H	$000FFEF4_H$ | $000FFC00_H$	-

*1: Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*2: The status of the multi-function serial interface does not support a DMA transfer caused by I^2C reception.

*3: The clock calibration unit does not support a DMA transfer caused by an interrupt.

*4: RAM ECC bit error does not support a DMA transfer caused by an interrupt.

*5: REALOS is a trademark of Cypress

*6: An interrupt of Up/down counter ch.2 does not support a DMA transfer.

*7: An interrupt related GDC does not support a DMA transfer.

**: Only supported by CY91F59A/B

UDCn: Up/down counter ch.n

ICUn: Input capture unit.n

OCUn: Output compare unit.n

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	$V_{CC}5$	Vss-0.3	Vss+6.0	V	
	$V_{CC}3$	Vss-0.3	Vss+4.0	V	Vcc3 ≤ Vcc5
	DV_{CC}	Vss-0.3	Vss+6.0	V	DVcc ≤ Vcc5
Analog power supply voltage*1,*2	$AV_{CC}5$	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5 ≤ Vcc5
	$AV_{CC}3$	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3 ≤ Vcc3
Analog reference voltage*1	AVRH5	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5
	AVR3	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3
Input voltage*1	V_{I1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{I2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{I3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Analog pin input voltage*1	$V_{IA}5$	Vss-0.3	Vcc5+0.3	V	
	$V_{IA}3$	Vss-0.3	Vcc3+0.3	V	
Output voltage*1	V_{O1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{O2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{O3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Maximum clamp current	I_{CLAMP}	-4	4	mA	*9
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	–	20	mA	*9
"L" level maximum output current *3	I_{OL1}	–	7	mA	When setting to 2mA*6
	I_{OL2}	–	40	mA	When setting to 30mA*7
	I_{OL3}	–	30	mA	When setting to 20mA*8
"L" level average output current *4	I_{OLAV1}	–	2	mA	When setting to 2mA*6
	I_{OLAV2}	–	30	mA	When setting to 30mA*7
	I_{OLAV3}	–	20	mA	When setting to 20mA*8
"L" level total output current *5	ΣI_{OL1}	–	50	mA	*6
	ΣI_{OL2}	–	250	mA	*7
	ΣI_{OL3}	–	50	mA	*8
"H" level maximum output current *3	I_{OH1}	–	-7	mA	When setting to 2mA*6
	I_{OH2}	–	-40	mA	When setting to 30mA*7
	I_{OH3}	–	-30	mA	When setting to 20mA*8
"H" level average output current *4	I_{OHAV1}	–	-2	mA	When setting to 2mA*6
	I_{OHAV2}	–	-30	mA	When setting to 30mA*7
	I_{OHAV3}	–	-20	mA	When setting to 20mA*8
"H" level total output current *5	ΣI_{OH1}	–	-50	mA	*6
	ΣI_{OH2}	–	-250	mA	*7
	ΣI_{OH3}	–	-50	mA	*8
Power consumption	P_D	–	1250	mW	LQFP product
		–	2500	mW	BGA product TEQFP product HQFP product
Operating temperature	T_A	-40	+105	°C	*10
Storage temperature	Tstg	-55	+150	°C	

*1: These parameters are based on the condition that $V_{SS}=AV_{SS}=DV_{SS}=0.0V$

*2: Caution must be taken that $AV_{CC}5$ and DV_{CC} do not exceed $V_{CC}5$. Similarly, $AV_{CC}3$ must not exceed $V_{CC}3$.

*3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

*5: The total output current is defined as the maximum current value flowing through all of corresponding pins.

*6: Outputs other than P60-P87 and 3V pin.

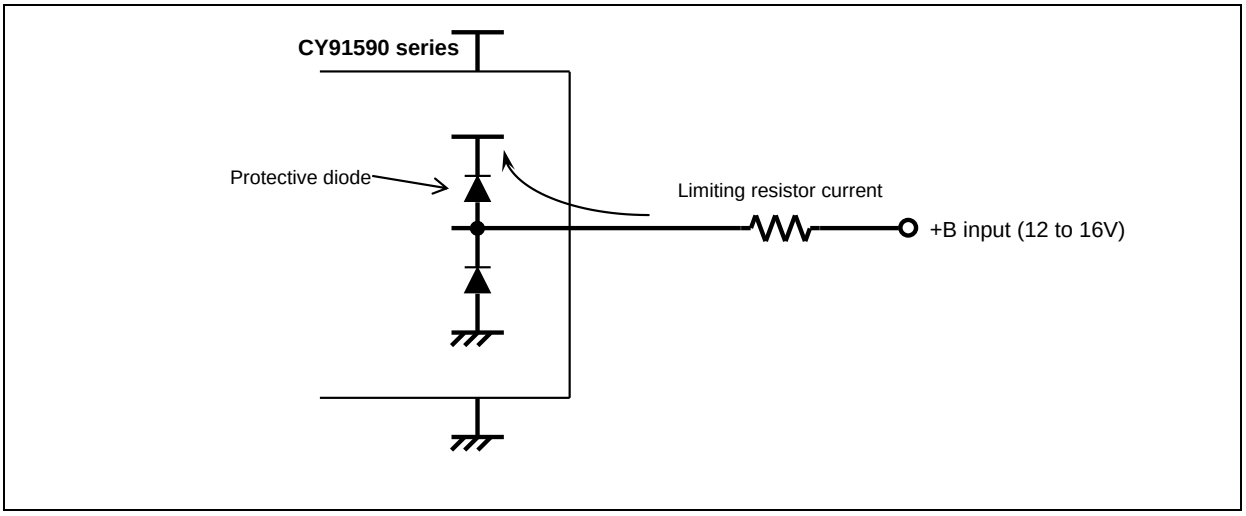
*7: Output of P60-P87 pins.

*8: Output of 3V pin.

*9: Corresponding pins: all general-purpose ports except P90/ADTG. (Except for the dedicated analog port)

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample Recommended Circuit



*10: To use this product at T_A=105°C, equip this on a multilayer board with four or more layers.

WARNING:
Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

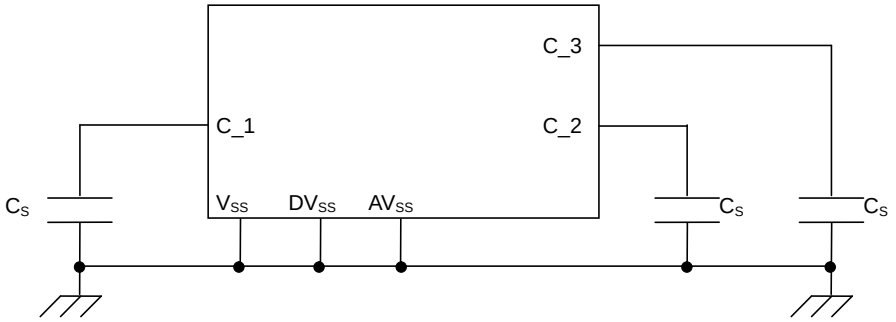
11.2 Recommended Operating Conditions

(V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}5$	4.5	5.5	V	Recommended operation guarantee range
	DV_{CC}	4.5	5.5	V	
	$AV_{CC}5$	4.5	5.5	V	
	$V_{CC}3$	3.0	3.6	V	
	$AV_{CC}3$	3.0	3.6	V	
	$V_{CC}5$	3.5	5.5	V	Operation guarantee range
	DV_{CC}	3.5	5.5	V	
	$AV_{CC}5$	3.5	5.5	V	
	$V_{CC}3$	2.7	3.6	V	
	$AV_{CC}3$	2.7	3.6	V	
Smoothing capacitor*	C_S	4.7 (tolerance within ±50%)		µF	Use a ceramic capacitor or a capacitor that has the similar frequency characteristics. Use a capacitor with a capacitance greater than C_S as the smoothing capacitor on the VCC pin.
Operating temperature	T_A	-40	+105	°C	

*: See the following diagram for details on the connection of smoothing capacitor C_S.

• C Pin Connection Diagram



WARNING:

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure. No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

11.3 DC Characteristics

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	CMOS input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH2}		CMOS hysteresis input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH3}		Automotive input level is selected	0.8× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH4}		TTL input level is selected	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH5}	RSTX, NMIX, MD2	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH7}	MD0,MD1	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH8}	DEBUGIF	–	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH10}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	CMOS hysteresis input level is selected	0.7× $V_{CC}3$	–	$V_{CC}3$+ 0.3	V	3.3V dedicated pin
	V_{IH11}		TTL input level is selected	2.0	–	$V_{CC}3$+ 0.3	V	
	V_{IH12}	MD3	-	0.8× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only
	V_{IH13}	TDI, TMS, TRST, TCK	-	0.7× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	$V_{CC}5$ = 4.5 V I_{OH} = -1.0 mA	$V_{CC}5$- 0.5	–	$V_{CC}5$	V	
	V_{OH2}		$V_{CC}5$ = 4.5 V I_{OH} = -2.0 mA	$V_{CC}5$- 0.5	–	$V_{CC}5$	V	
	V_{OH3}	P060 to P067, P070 to P077, P080 to P087	DV_{CC} = 4.5 V I_{OH} = -30.0 mA	DV_{CC}- 0.5	–	DV_{CC}	V	SMC shared pin
	V_{OH4}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	$V_{CC}3$ = 3.0 V I_{OH} = -2.0 mA	$V_{CC}3$- 0.5	–	$V_{CC}3$	V	3.3V dedicated pin
	V_{OH5}		$V_{CC}3$ = 3.0 V I_{OH} = -5.0 mA					
	V_{OH6}		$V_{CC}3$ = 3.0 V I_{OH} = -10.0 mA					
	V_{OH7}		$V_{CC}3$ = 3.0 V I_{OH} = -20.0 mA					
	V_{OH8}	TDO	$V_{CC}5$ = 4.5 V I_{OH} = -5.0 mA	$V_{CC}5$- 0.5	–	$V_{CC}5$	V	BGA product only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	CMOS input level is selected	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL2}		CMOS hysteresis Input level is selected	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL3}		Automotive input level is selected	Vss-0.3	–	0.5× $V_{CC}5$	V	
	V_{IL4}		TTL input level is selected	Vss-0.3	–	0.8	V	
	V_{IL5}	RSTX, NMIX, MD2	–	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL7}	MD0, MD1	–	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL8}	DEBUGIF	–	Vss-0.3	–	0.8	V	
	V_{IL10}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	CMOS hysteresis input level is selected	Vss-0.3	–	0.3× $V_{CC}3$	V	3.3V dedicated pin
	V_{IL11}		TTL input level is selected	Vss- 0.3	–	0.8	V	
	V_{IL12}	MD3	-	V_{SS}- 0.3	-	0.3× V_{CC5}	V	BGA product only
	V_{IL13}	TDI, TMS, TRST, TCK	-	V_{SS}- 0.3	-	0.3× V_{CC5}	V	BGA product only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	$V_{CC}5$ = 4.5 V I_{OL} = 1.0 mA	0	–	0.4	V	
	V_{OL2}		$V_{CC}5$ = 4.5 V I_{OL} = 2.0 mA	0	–	0.4	V	
	V_{OL3}	P060 to P067, P070 to P077, P080 to P087	DV_{CC} = 4.5 V I_{OL} = 30.0 mA	0	–	0.55	V	SMC shared pin
	V_{OL4}	P127, P130, P132, P133	$V_{CC}5$ = 4.5 V I_{OL} = 3.0 mA	0	–	0.4	V	I^2C shared pin (I^2C is selected)
	V_{OL5}	DEBUGIF	$V_{CC}5$ = 2.7 V I_{OL} = 25.0 mA	0	–	0.25	V	
	V_{OL6}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	$V_{CC}3$ = 3.0 V I_{OL} = 2.0 mA	0	–	0.4	V	3.3V dedicated pin
	V_{OL7}		$V_{CC}3$ = 3.0 V I_{OL} = 5.0 mA					
	V_{OL8}		$V_{CC}3$ = 3.0 V I_{OL} = 10.0 mA					
	V_{OL9}		$V_{CC}3$ = 3.0 V I_{OL} = 20.0 mA					
	V_{OL10}	TDO	$V_{CC}5$ = 4.5 V I_{OH} = 5.0 mA	0	–	0.4	V	BGA product only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	All input pins	VCC = DVCC = AVCC = 5.5 V VSS<VI<VCC	-5	–	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	–	25	–	100	kΩ	
	R_{UP2}	All 5V port input pins	Pull-up resistance is selected	25	–	100	kΩ	
	R_{UP3}	All 3V port input pins	Pull-up resistance is selected	17	–	66	kΩ	
Pull-down resistance	R_{DOWN1}	MD2	–	25	–	100	kΩ	
	R_{DOWN2}	All 5V port input pins	Pull-down resistance is selected	25	–	100	kΩ	
	R_{DOWN3}	All 3V port input pins	Pull-down resistance is selected	17	–	66	kΩ	
Input capacitance	C_{IN1}	Other than $V_{CC}3$, $V_{CC}5$, V_{SS}, DV_{CC}, DV_{SS}, $AV_{CC}3$, $AV_{SS}3$, $AV_{CC}5$, $AV_{SS}5$, C1, C2, C3, P060 to P067, P070 to P077, P080 to P087	–	–	5	15	pF	
	C_{IN2}	P060 to P067, P070 to P077, P080 to P087	When using SMC	–	15	45	pF	

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	$I_{CC}5$	$V_{CC}5$	At normal operation F_{CP}=128 MHz, Fcpp=32 MHz	–	80	120	mA	*4
				–	80	155	mA	*5
			At normal operation F_{CP}=80 MHz, Fcpp=40 MHz	–	60	100	mA	*4
				–	60	130	mA	*5
			At FLASH write F_{CP}=128 MHz, Fcpp=32 MHz	–	95	135	mA	*3, *4
				–	95	165	mA	*3, *5
			At FLASH erase F_{CP}=128 MHz, Fcpp=32 MHz	–	95	135	mA	*3, *4
				–	95	165	mA	*3, *5
	$I_{CCS}5$		At sleep mode F_{CP}=128 MHz, Fcpp=32 MHz	–	25	65	mA	*4
				–	25	80	mA	*5
	$I_{CCBS}5$		At bus sleep mode F_{CP}=128 MHz, Fcpp=32 MHz	–	15	55	mA	*4
				–	15	70	mA	*5
	$I_{CCT}5$		At RTC mode, 4 MHz source oscillation	–	650	1800	µA	When using external clock*1, T_A=+25°C
				–	800	1950	µA	When using crystal T_A=+25°C
	$I_{CCTS}5$		When RTC mode shutdown, 4 MHz source oscillation	–	130	230	µA	When using external clock*1, T_A=+25°C
				–	280	380	µA	When using crystal T_A=+25°C
	$I_{CCH}5$		At stop mode	–	250	1400	µA	T_A=+25°C
	$I_{CCHS}5$		When stop mode shutdown	–	100	200	µA	T_A=+25°C
	$I_{CC}3$	$V_{CC}3$	When GDC normal operation F_{gdC}=81 MHz, $F_{gdC\text{-}IF}$=108 MHz	–	100	200	mA	*4
				–	200	300	mA	*5
			When GDC operation stop	–	2	100	mA	*4
					2	155	mA	*5
			When GDC side regulator stop	–	70	200	µA	
	I_A3	$AV_{CC}3$	When NTSC operates	–	30	60	mA	At AVR3=AVss3
			When NTSC stop	–	5	10	mA	At AVR3=AVss3

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	ΔV_{OH3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	DVcc=4.5 V I_{OH}=-30.0 mA Maximum deviation of V_{OH3}	–	–	90	mV	*2
High current output drive capacity Phase-to-phase deviation2	ΔV_{OL3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	DVcc=4.5 V I_{OL}=30.0 mA Maximum deviation of V_{OL3}	–	–	90	mV	*2

*1: The power supply current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

*2: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH3} / V_{OL3} for each pin is defined. Same for other channels.

*3: This product contains both program Flash and WorkFlash. This parameter is defined when only one of them is in the write/erase state.

*4: CY91F591/2/4/6/7/9

*5: CY91F59A/B

11.4 AC Characteristics

11.4.1 Main Clock Timing

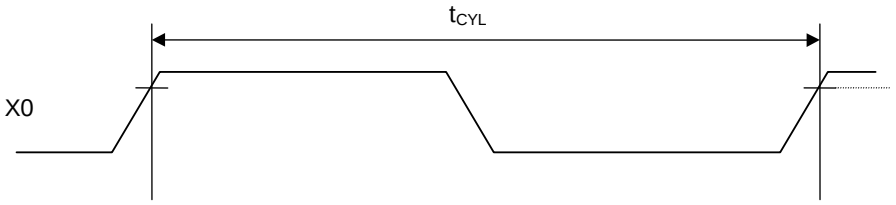
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	–	–	4	–	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		–	250	–	ns	
Internal operating clock frequency*1, *2	F_{CP}	–	–	2	–	128	MHz	CPU clock
	F_{CPP}	–	–	2	–	40	MHz	Peripheral bus clock
Internal operating clock cycle time*1, *2	t_{CP}	–	–	7.8125	–	500	ns	CPU clock
	t_{CPP}	–	–	25	–	500	ns	Peripheral bus clock
CAN PLL jitter (when lock)	t_{PJ}	–	–	-10	–	+10	ns	
Built-in CR oscillation frequency	F_{CCR}	–	–	50	100	200	kHz	

*1: The maximum frequency of CPU clock is described in the table of Product Type.

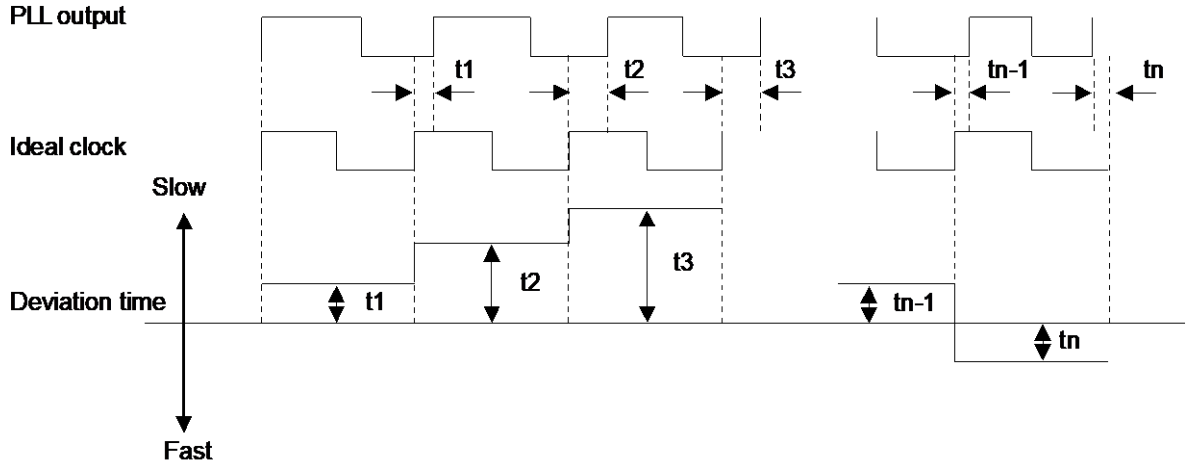
*2: The maximum / minimum value is defined when using the main clock and PLL clock.

• X0,X1 Clock Timing



• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

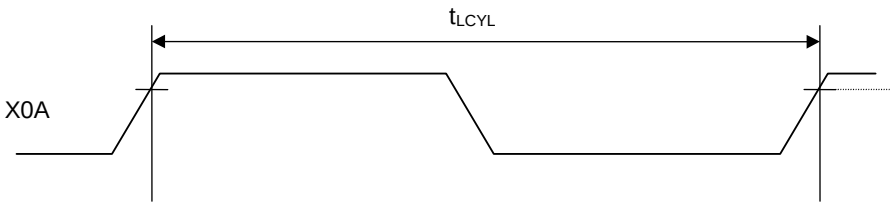


11.4.1.1 Sub clock timing (products without s-suffix)

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

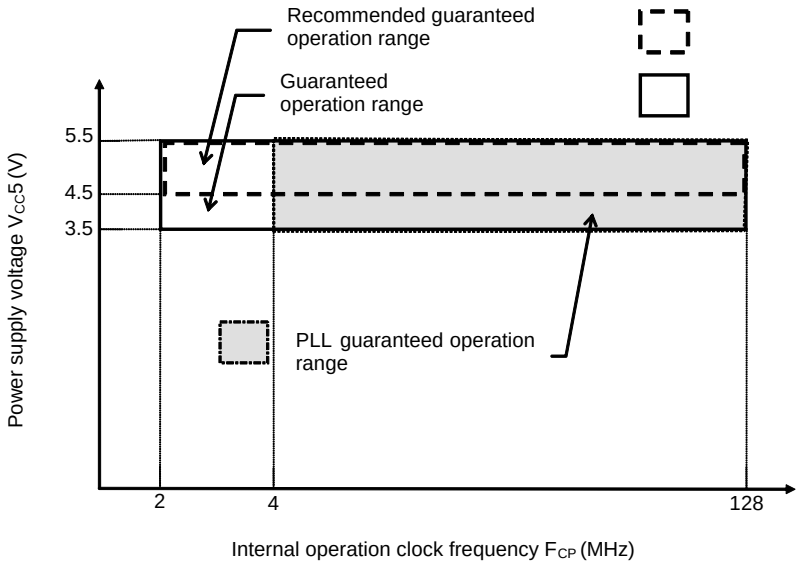
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	–	–	30.52	–	µs	

• X0A,X1A Clock Timing



Guaranteed Operation Range (5V Operating Microcontroller Section)

Internal operation clock frequency vs. Power supply voltage

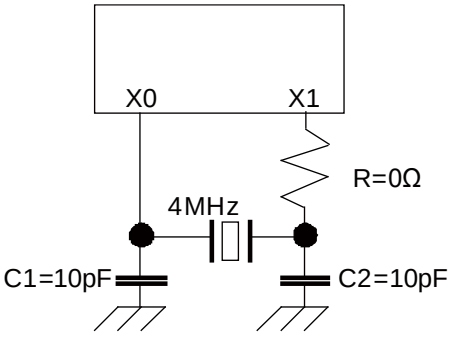


Note: The CPU will be reset at the power supply voltage 4V±0.3V or less.

Oscillation Clock Frequency vs. Internal Operation Clock Frequency

		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	128MHz

• Example of Oscillation Circuit

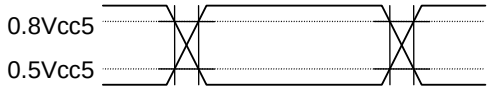


Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your printed circuit board so that the oscillator can start oscillation within 20ms.

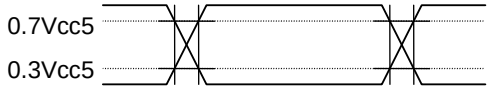
AC characteristics are specified by the following measurement reference voltage values.

• Input Signal Waveform

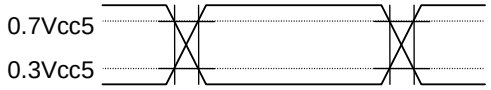
Hysteresis Input Pin (Automotive)



Hysteresis Input Pin (CMOS Normal)



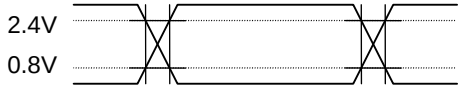
Hysteresis Input Pin (CMOS Hysteresis)



TTL Input Pin

• Output Signal Waveform

Output Pin

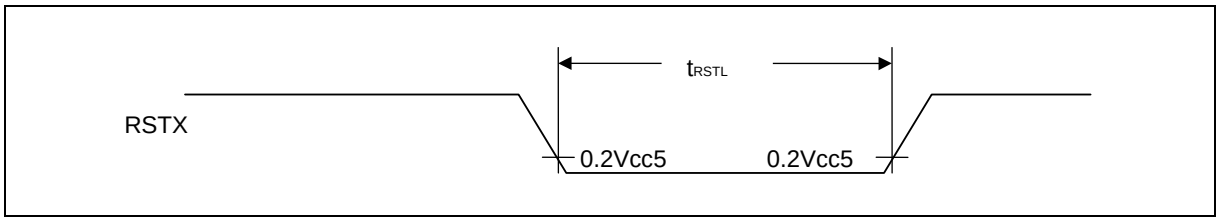


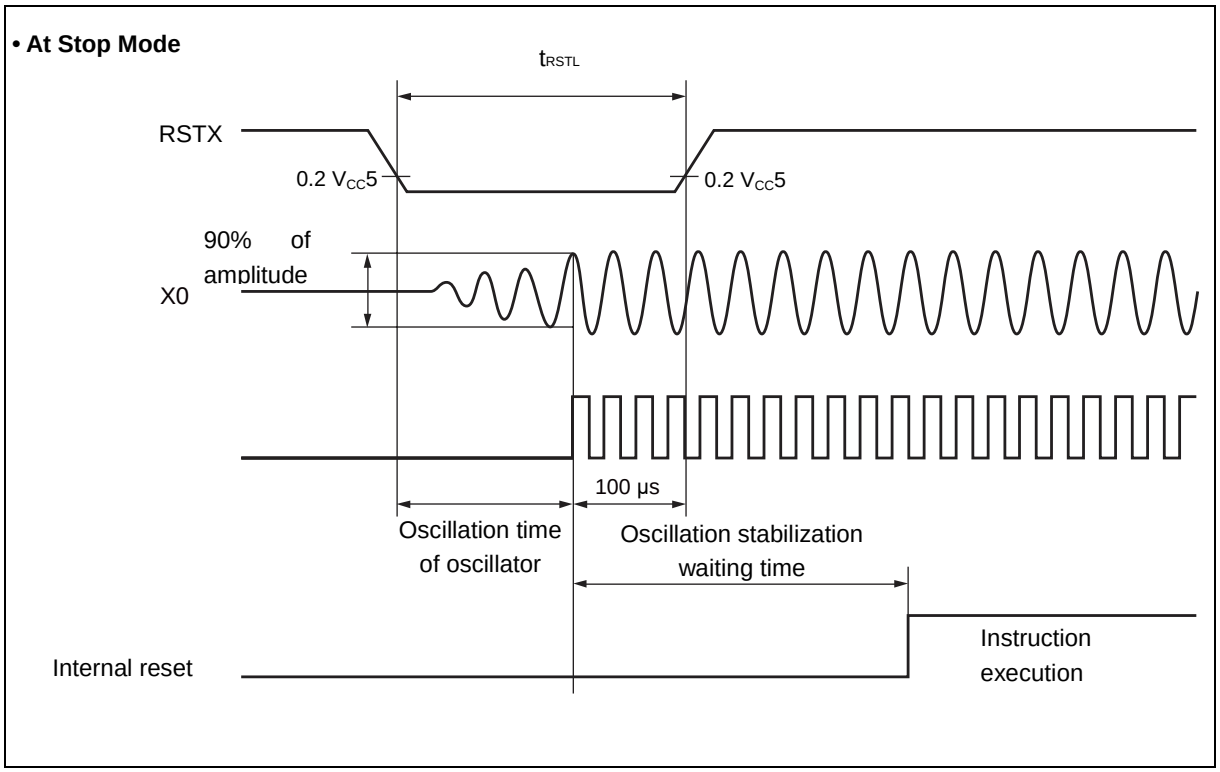
11.4.1.2 Reset Input

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* + 100 µs	–	ms	At Stop mode
				100 µs	–	µs	At RTC mode
Width for reset input removal				1 µs	–	µs	

*: The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.





11.4.1.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	$V_{CC}5$	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	$V_{CC}5$	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Specification for voltage slope detection	–	$V_{CC}5$	$V_{CC}5$ = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	$V_{CC}5$	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this specification or less, it is possible to suppress the voltage slope detection. This is the specification when the power supply fluctuation is stable.

*3: This time is to start the voltage slope detection at next power on after power down and internal charge loss.

11.4.1.4 Multi-function Serial

UART Timing

■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=0

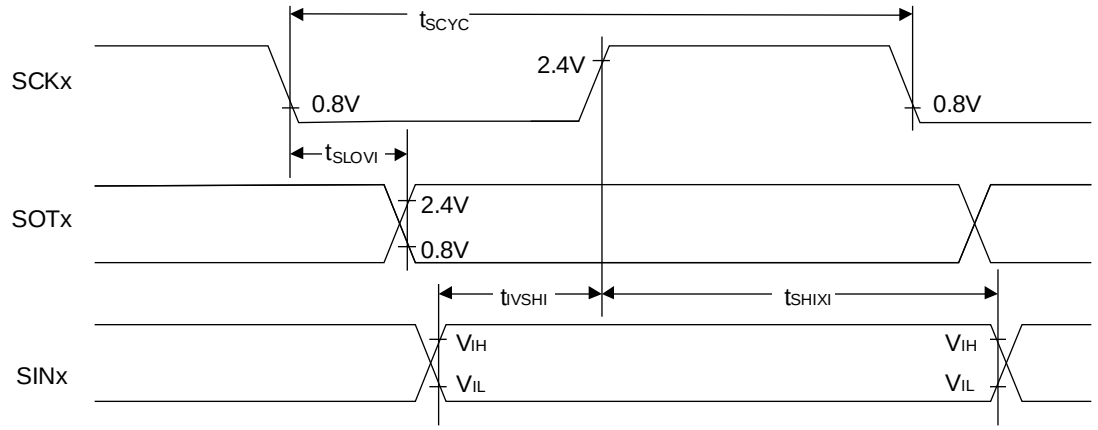
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCKx	–	$4t_{CPP}$	–	ns	Internal shift clock mode: C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		34	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
Serial clock "H"pulse width	t_{SHSL}	SCKx	–	t_{CPP}+10	–	ns	External shift clock mode: C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		–	33	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINn		10	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns	
SCK fall time	t_F	SCKx		–	5	ns	
SCK rise time	t_R	SCKx		–	5	ns	

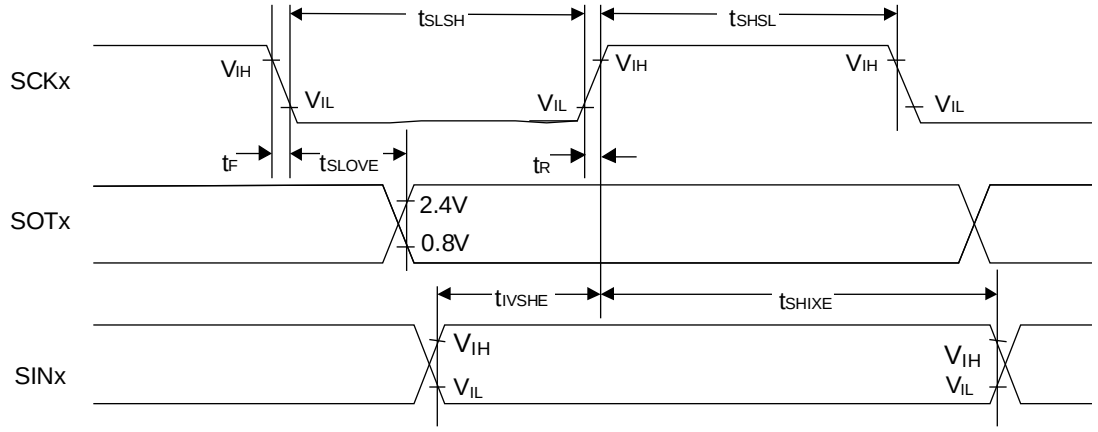
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

• Internal shift clock mode



• External shift clock mode



■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=0

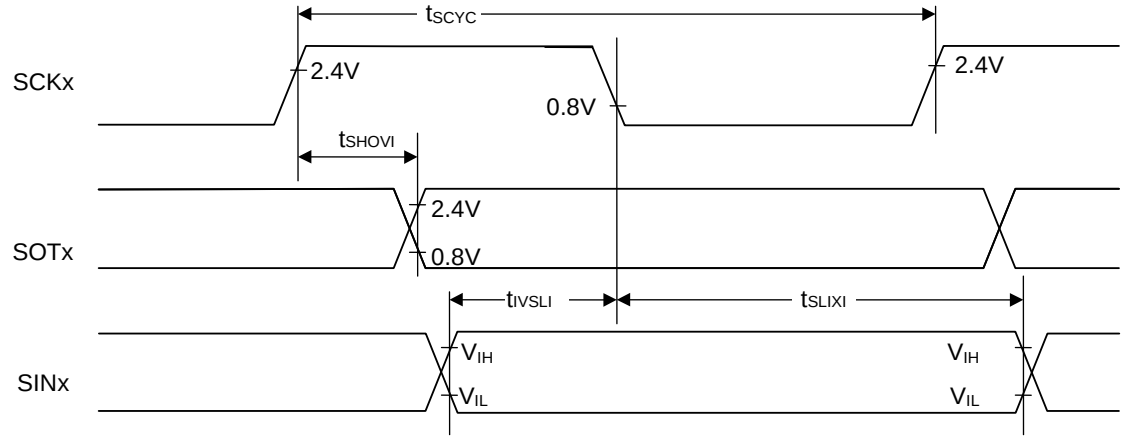
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCKx	–	$4t_{CPP}$	–	ns	Internal shift clock mode: C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-30	+30	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		34	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCKx	–	t_{CPP}+10	–	ns	External shift clock mode: C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)
Serial clock "L"pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		–	33	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	–	ns	
SCK fall time	t_F	SCKx		–	5	ns	
SCK rise time	t_R	SCKx		–	5	ns	

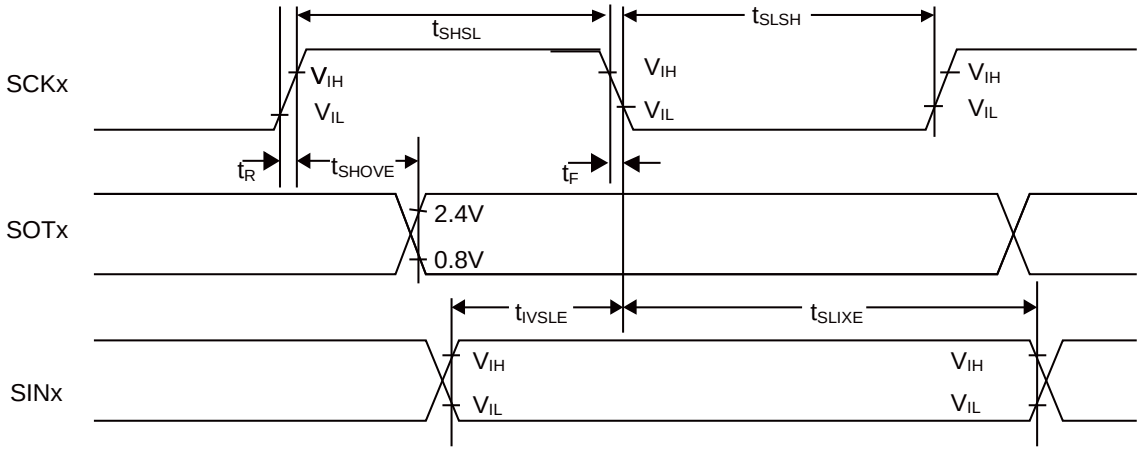
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=1

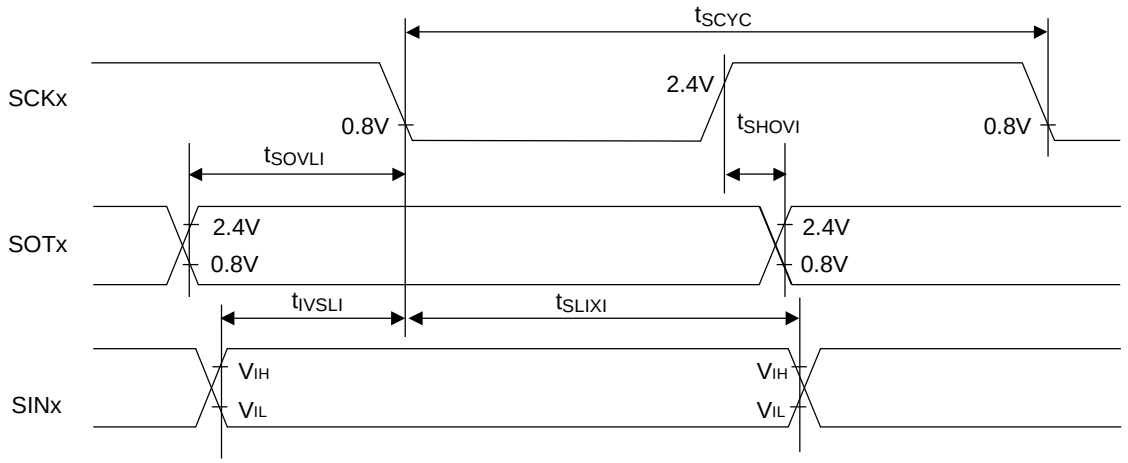
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)	$4t_{CPP}$	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		34	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

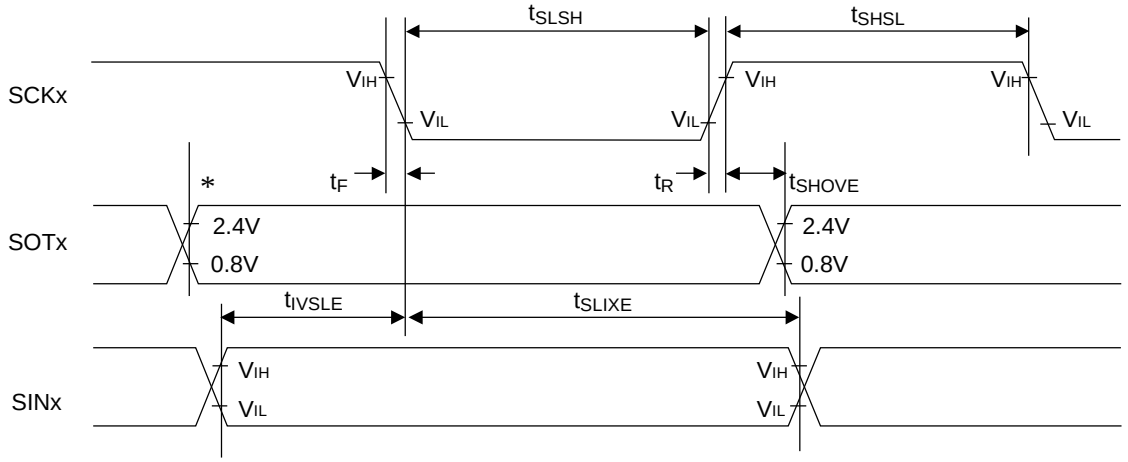
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



***: Changes when Writing to TDR Register**

■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

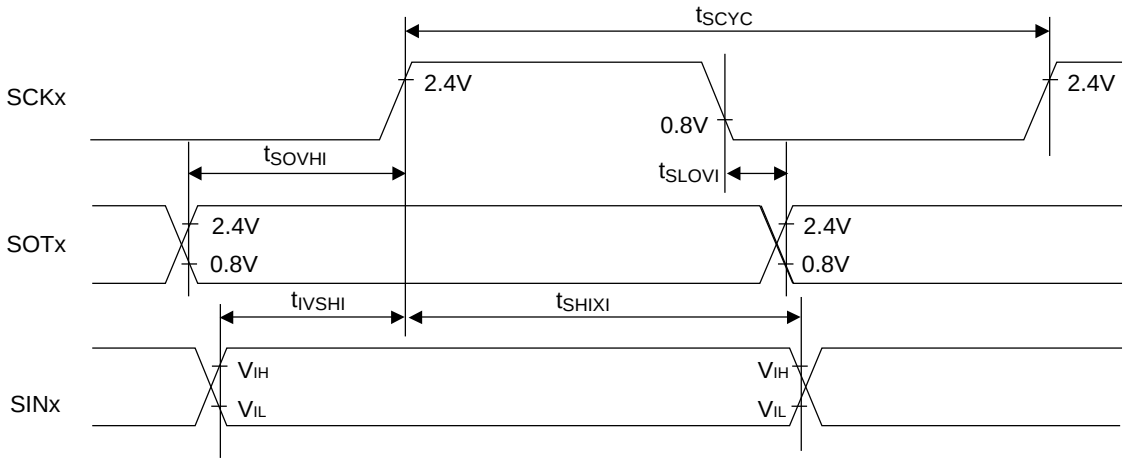
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50 pF(When drive capability is 2 mA or more.) C_L=20 pF(When drive capability is 1 mA)	$4t_{CPP}$	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		34	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H"pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50 pF(When drive capability is 2 mA or more.) C_L=20 pF(When drive capability is 1 mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

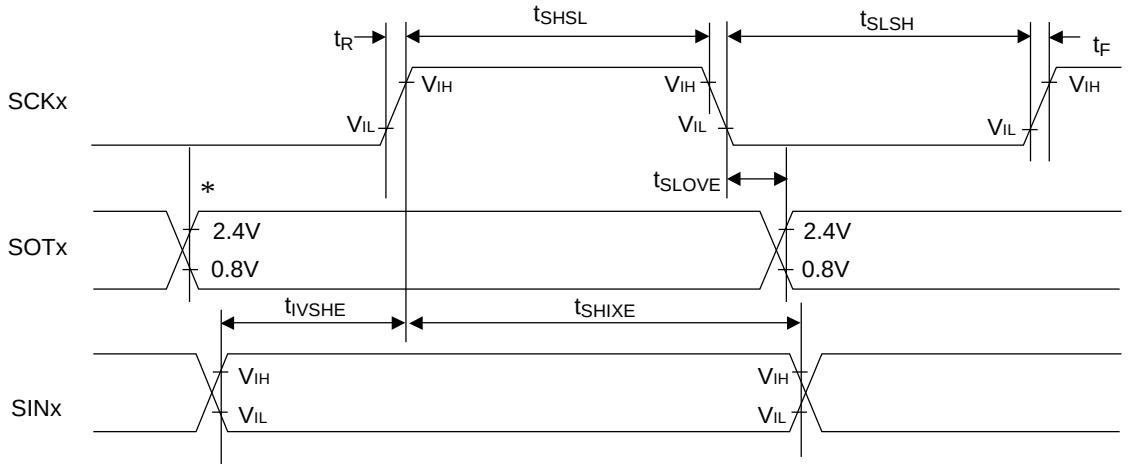
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



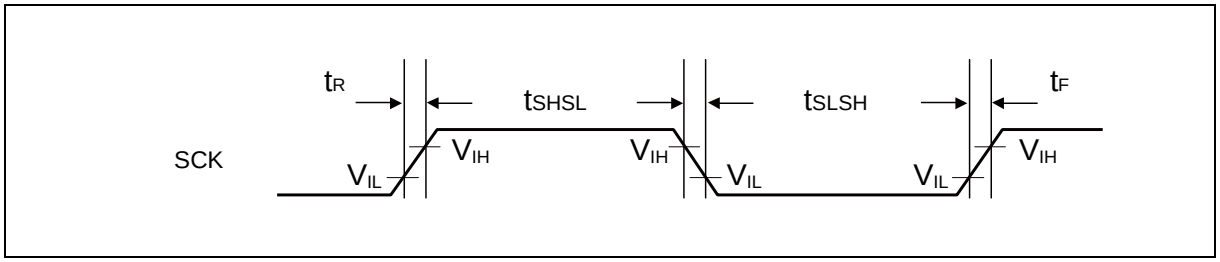
*: Changes when Writing to TDR Register

External Clock (EXT = 1): Asynchronous Only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock "H" pulse width	t_{SHSL}	SCKx	C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA)	t_{CPP}+10	-	ns
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	-	ns
SCK fall time	t_F			-	5	ns
SCK rise time	t_R			-	5	ns

Note: "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.



I²C Timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

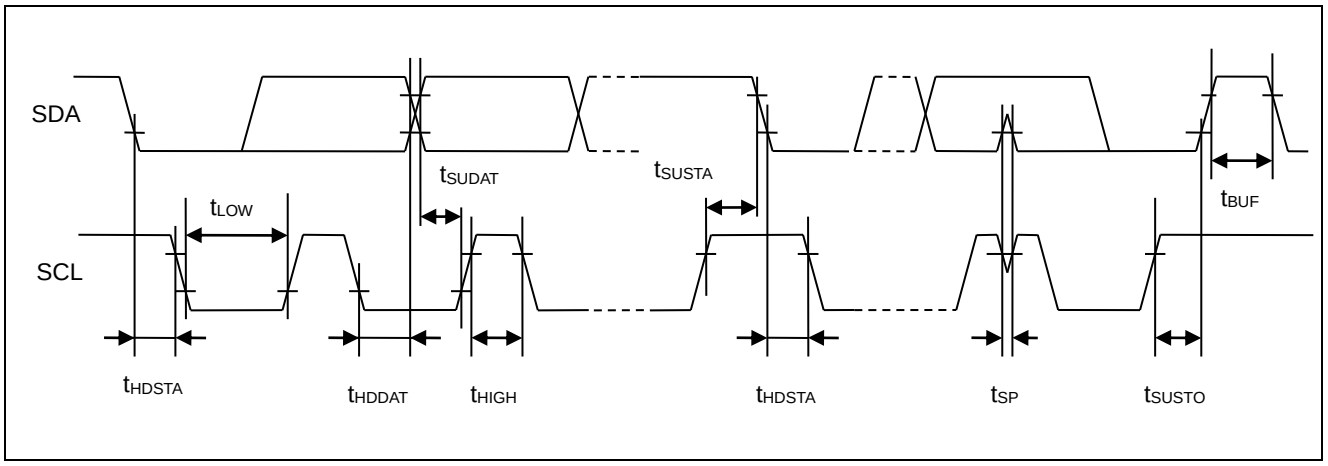
Parameter	Symbol	Pin Name	Conditions	Standard Mode		High-Speed Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0, SCK1	C_L=50 pF (When drive capability is 2 mA or more.) C_L=20 pF (When drive capability is 1 mA) R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK0, SCK1, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0, SCK1, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		0	3.45*2	0	0.9	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		250*3	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	2t_{CPP}*4	–	2t_{CPP}*4	–	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the peripheral clock frequency to 8MHz or more when use I²C.


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

11.4.1.5 LIN-UART timing

■Bit setting: ESCR: SCES=0, ECCR: SCDE=0

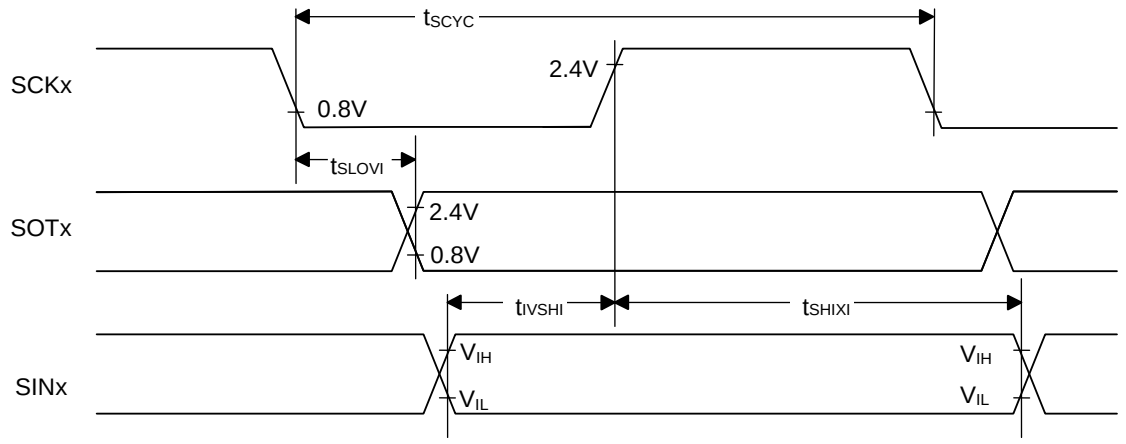
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80 pF + 1 · TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80 pF + 1 · TTL
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	–	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		30	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

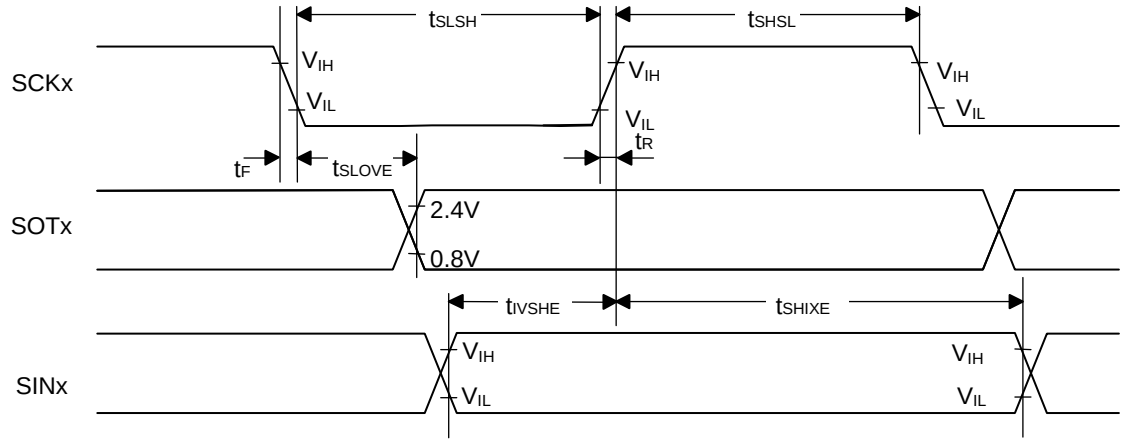
Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



■Bit setting: ESCR: SCES=1, ECCR: SCDE=0

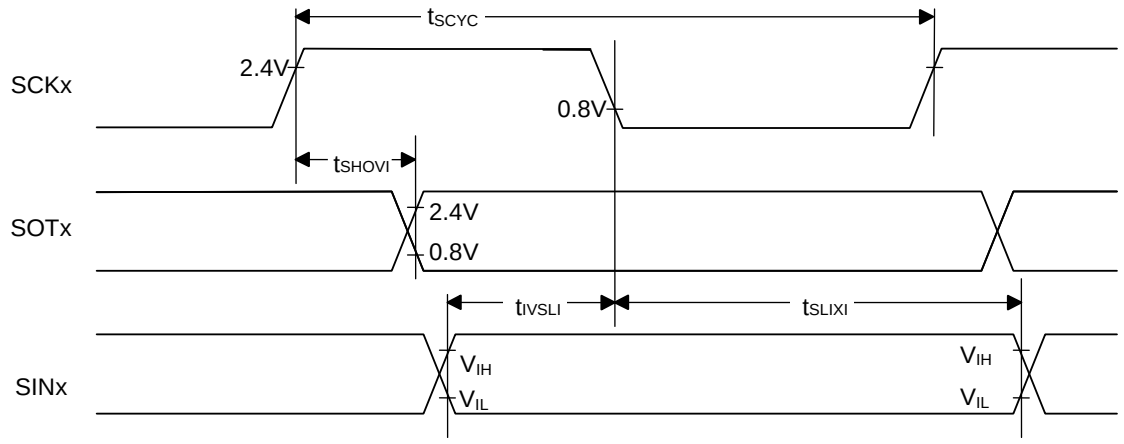
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80 pF+1 • TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80 pF+1 • TTL
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		30	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

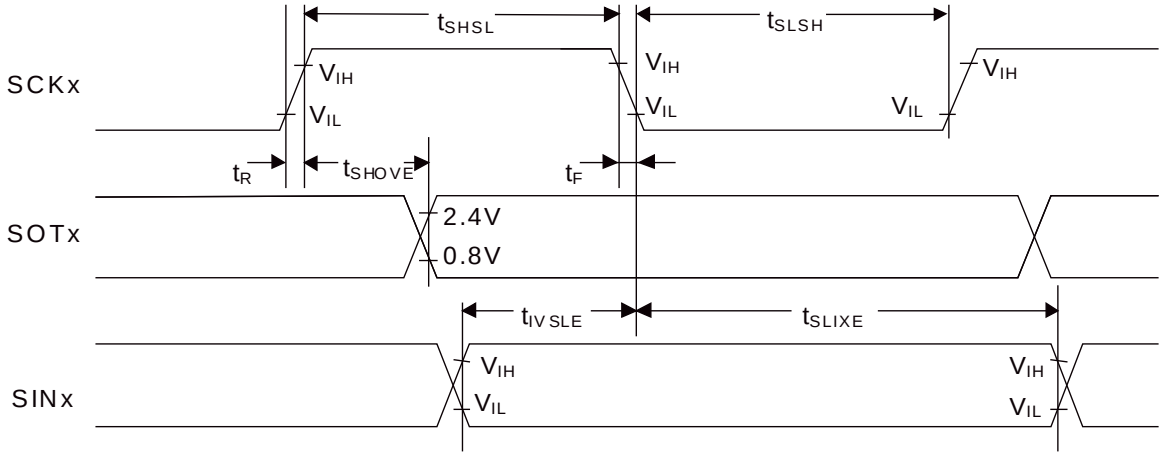
Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



■Bit setting: ESCR: SCES=0, ECCR: SCDE=1

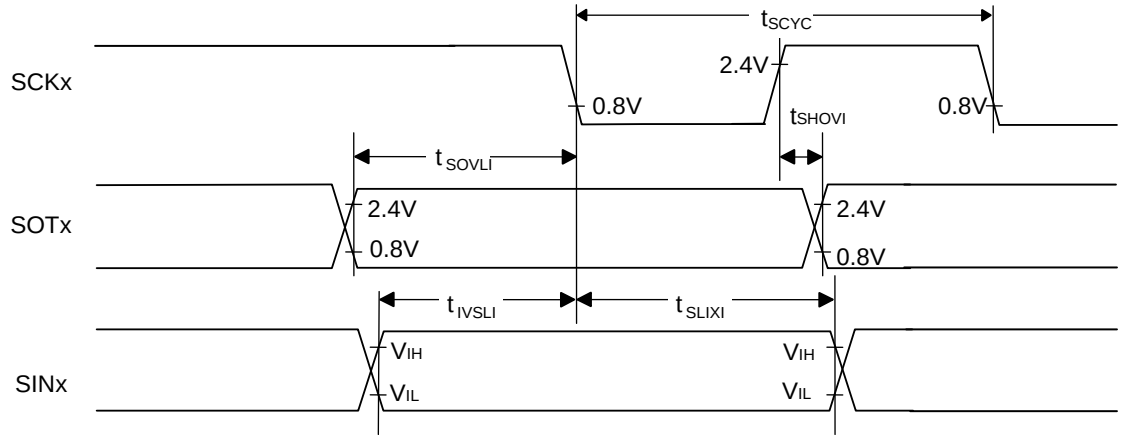
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock Mode: C_L=80 pF + 1 • TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• Internal Shift Clock Mode



■Bit setting: ESCR: SCES=1, ECCR: SCDE=1

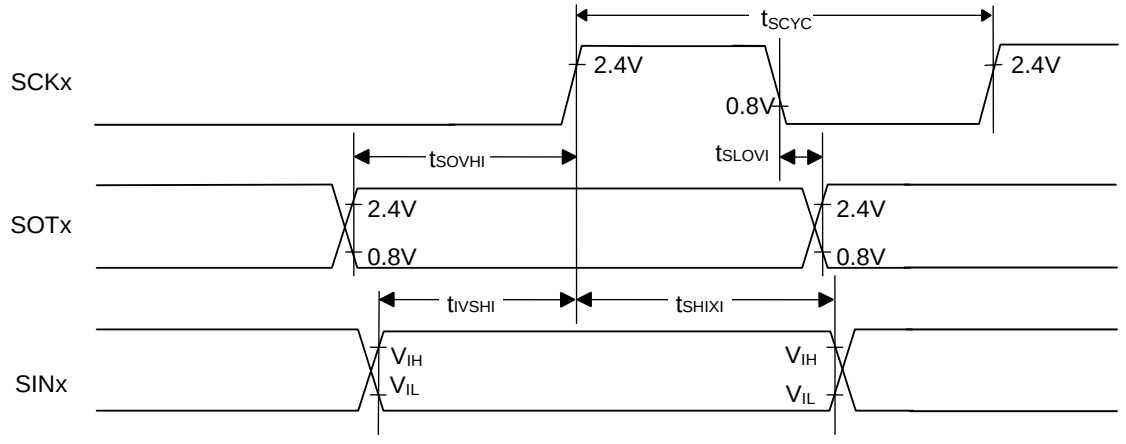
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80 pF+1 • TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		-50	+50	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SIN2, SIN3, SIN4, SIN5, SIN6, SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2, SCK3, SCK4, SCK5, SCK6, SCK7, SOT2, SOT3, SOT4, SOT5, SOT6, SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• Internal Shift Clock Mode

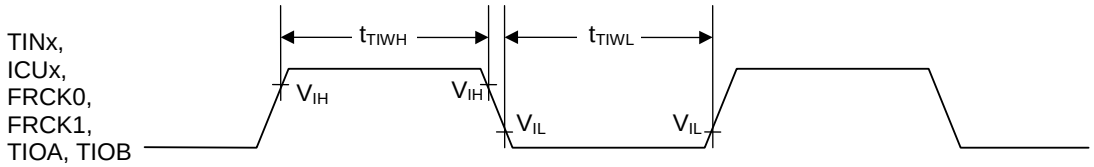


11.4.1.6 Timer input timing

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN3, TIN7 to TIN10, ICU0 to ICU11, FRCK0 to FRCK7, TIOA, TIOB, UDCAIN0 to 2, UDCBIN0 to 2, UDCZIN0 to 2	–	$4t_{CPP}$	–	ns	

• **Timer Input Timing**



Note:

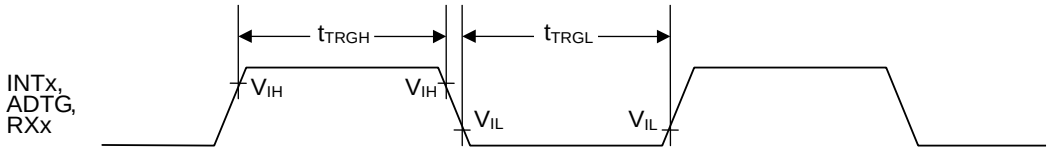
The description can be applied to FRCK2 to 7, UDCAIN0 to 2, UDCBIN0 to 2, and UDCZIN0 to 2 as well.

11.4.1.7 Trigger input timing

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

• **Trigger Input Timing**

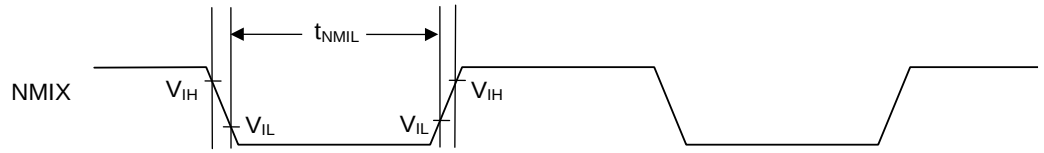


11.4.1.8 NMI input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

• **NMIX Input Timing**



11.4.1.9 Low voltage detection (External low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{CC5}	VCC5	–	–	–	5.5	V	Microcontroller unit
	$V_{CC}3$	VCC3	–	–	–	3.6	V	GDC unit
Detection voltage	V_{DL}	VCC5	*1	3.9	4.1	4.3	V	When power-supply voltage falls at microcontroller unit and detection level is set initially
		VCC3	*1	2.2	2.4	2.6	V	When power-supply voltage falls at GDC unit and detection level is set initially
Hysteresis width	V_{HYS}	VCC5/ VCC3	–	–	–	125	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	
Power supply voltage fluctuation rate	–	VCC5, VCC3	–	-2	–	2	V/ms	*2

*1: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: In order to perform the low-voltage detection at the detection voltage (V_{DL}), be sure to suppress fluctuation of the power supply voltage within the limits of the power supply voltage fluctuation rate.

11.4.1.10 Low voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC	–	–	–	1.3	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		–	–	–	50	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	

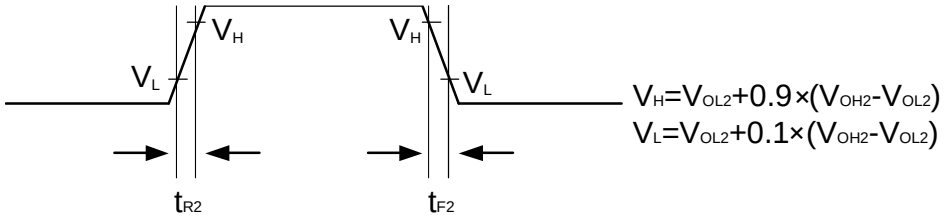
*: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.4.1.11 High current output slew rate

(T_A: Recommended operating conditions, $V_{CC}5=AV_{CC}5=5.0V \pm 10\%$, $V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise /fall time	t_{R2}, t_{F2}	P060 to P067, P070 to P077, P080 to P087	–	15	–	100	ns	load capacitance 85 pF

• **Slew Rate Output Timing**



$V_H=V_{OL2}+0.9\times(V_{OH2}-V_{OL2})$

$V_L=V_{OL2}+0.1\times(V_{OH2}-V_{OL2})$

11.4.1.12 External memory interface

Memory Controller

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

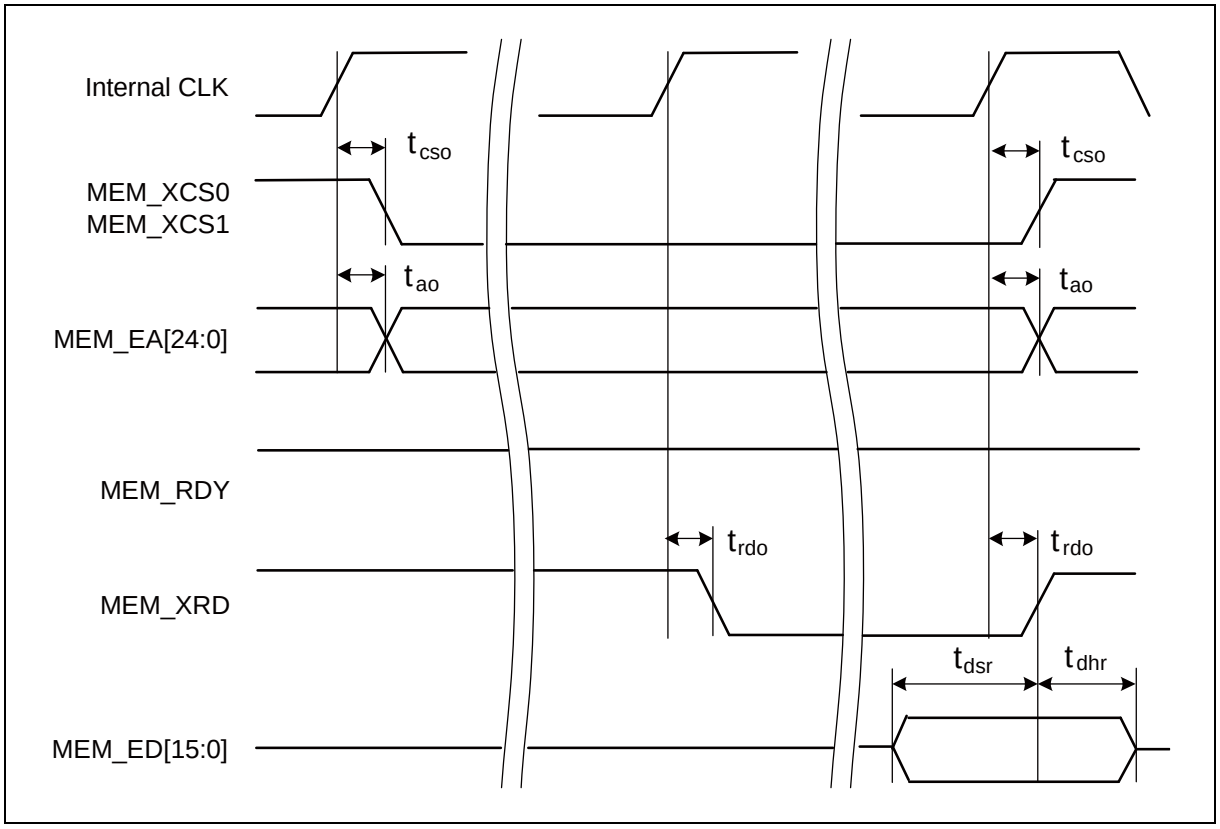
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip Select delay time	t_{cso}	MEM_XCS0, MEM_XCS1	12 pF/10 mA	–	18	ns	*1
				–	14	ns	*2
Address delay time	t_{ao}	MEM_EA[24:0]		–	18	ns	*1
				–	14	ns	*2
Data output delay time	t_{do}	MEM_ED[15:0]		–	18	ns	*1
				–	17	ns	*2
Data output → HiZ time	t_{doz}			–	18	ns	*1
				–	17	ns	*2
NOR Flash data setup time	t_{dsr}			20	–	ns	*1
				11	–	ns	*2
NOR Flash data hold time	t_{dhr}			0	–	ns	*1
				0	–	ns	*2
NOR Flash page Read data setup time	t_{dsp}			20	–	ns	*1
				8.5	–	ns	*2
NOR Flash page Read data hold time	t_{dhp}			0	–	ns	*1
				0	–	ns	*2
XRD delay time	t_{rdo}	MEM_XRD		–	18	ns	*1
				–	14	ns	*2
XWR delay time	t_{wro}	MEM_XWR		–	18	ns	*1
				–	14	ns	*2

Output delay is reference clock is an internal clock. The reference clock of MEM_RDY is an internal clock.

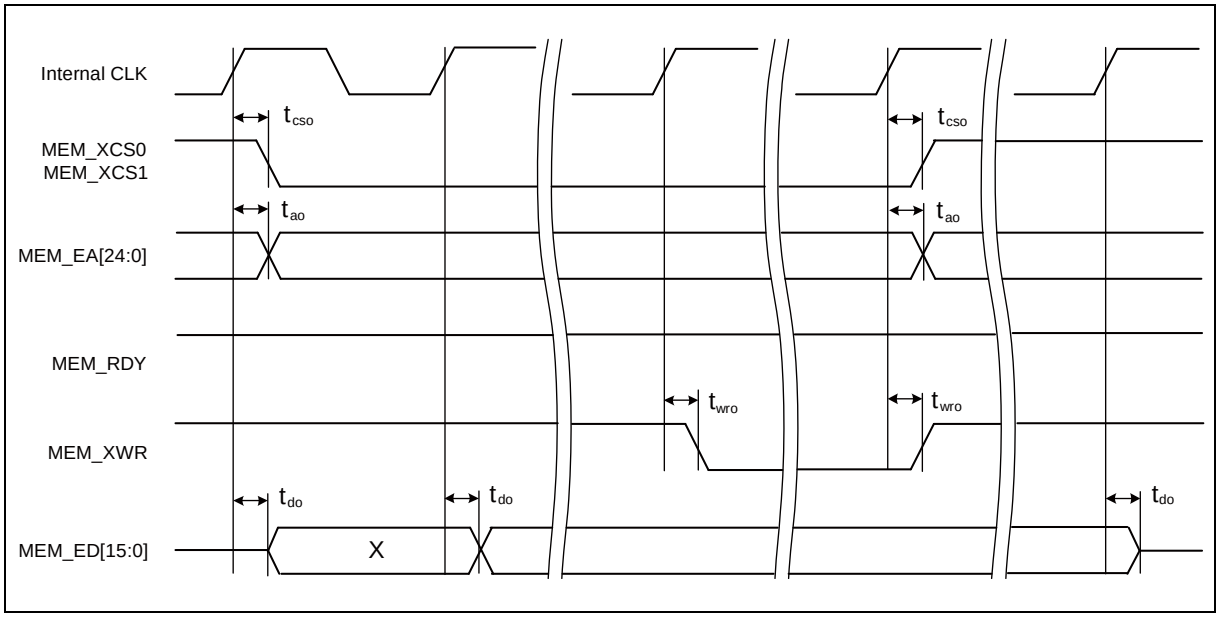
*1: CY91F591/2/4/6/7/9

*2: CY91F59A/B

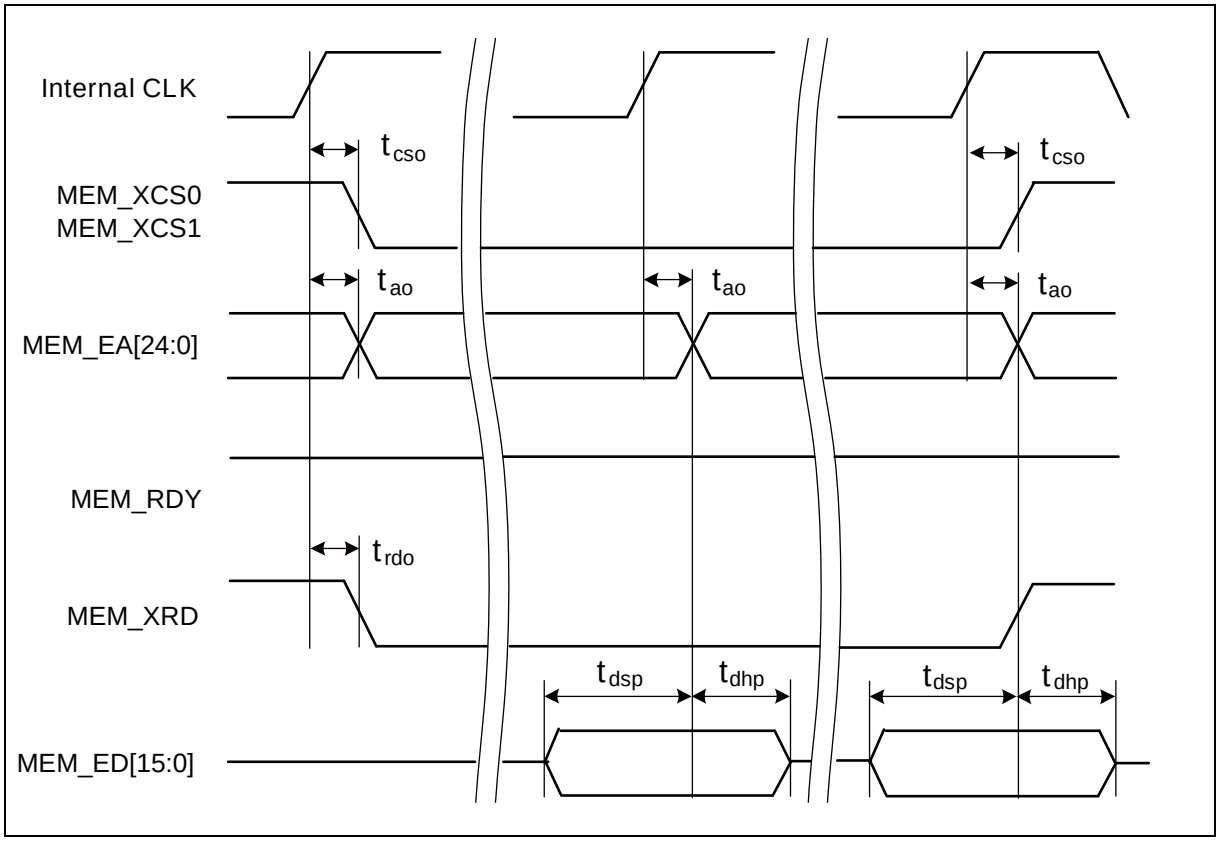
■NOR Flash read timing



■NOR Flash write timing



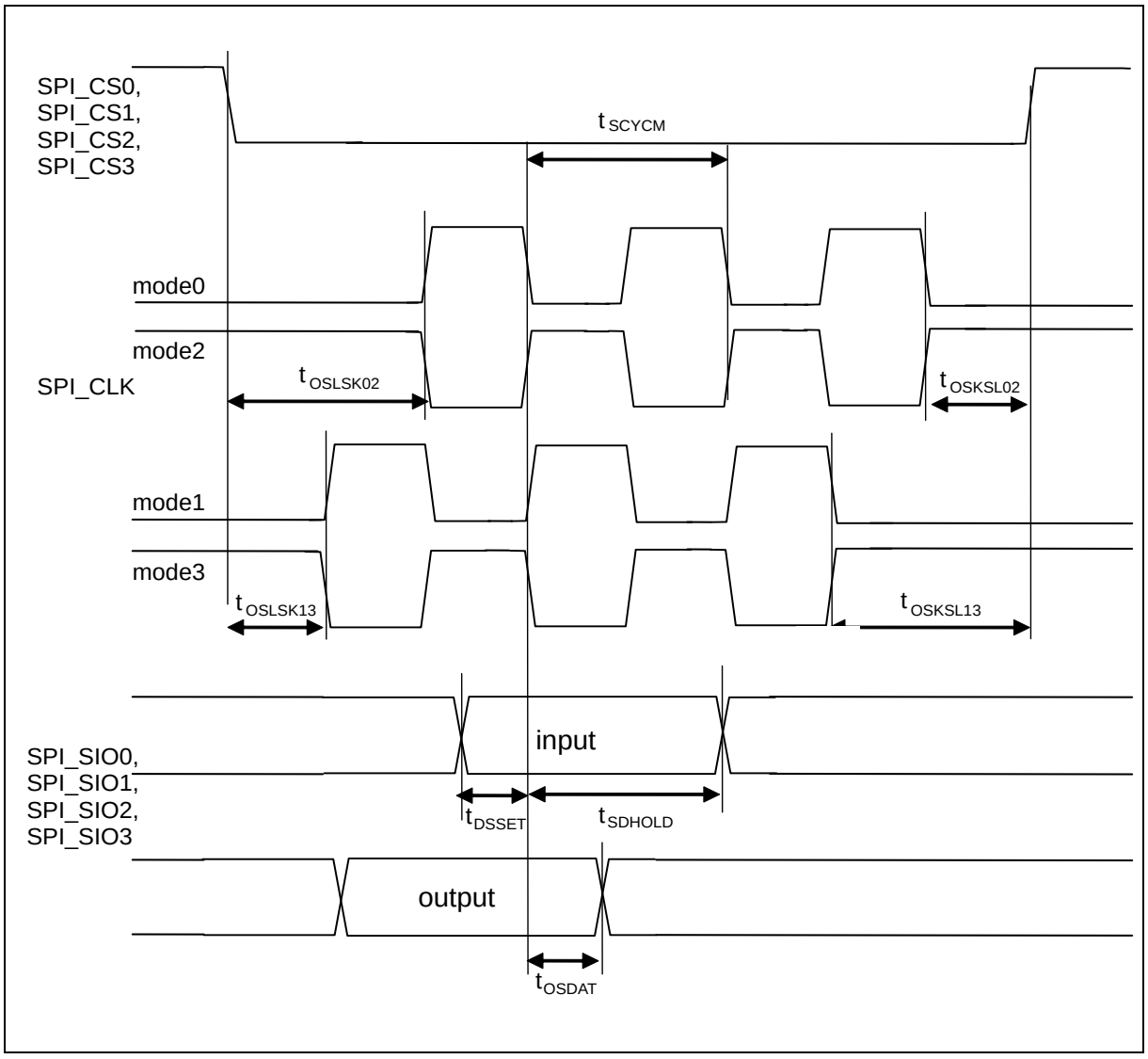
■NOR Flash Page read timing



HS-SPI

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYCM}	SPI_CLK	C_L=12 pF (When drive capability is 10 mA)	25	–	ns	RTM=1, Mode=0,1,3
				50			Other than those above
Valid CS → CLK start time (mode0/mode2)	$t_{OSLSK02}$	SPI_CLK, SPI_CS0, SPI_CS1, SPI_CS2, SPI_CS3		1.5×t_{SCYCM}-5	–	ns	
Valid CS → CLK start time (mode1/mode3)	$t_{OSLSK13}$			t_{SCYCM}-5	–	ns	
CLK end → Invalid CS time (mode0/mode2)	$t_{OSKSL02}$			t_{SCYCM}-3	–	ns	
CLK end → Invalid CS time (mode1/mode3)	$t_{OSKSL13}$			1.5×t_{SCYCM}-3	–	ns	
SIO data output time	t_{OSDAT}	SPI_CLK, SPI_SIO0, SPI_SIO1, SPI_SIO2, SPI_SIO3		-3	5	ns	
SIO setup	t_{DSSET}			7	–	ns	RTM=1 and Mode=0,1,3
				14	–	ns	Other than those above
SIO hold	t_{SDHOLD}			0.5×t_{SCYCM}	–	ns	


SPI_CS0,
SPI_CS1,
SPI_CS2,
SPI_CS3
tSCYCM
mode0
mode2
SPI_CLK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
SPI_SIO0,
SPI_SIO1,
SPI_SIO2,
SPI_SIO3
input
tDSSET
tSDHOLD
output
tOSDAT

11.4.1.13 GDC display signal

Clock

AC timing of video interface clock signal

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
DCLKI frequency	Fdclki0	DCLKI	–	54	MHz	
DCLKI "H"width	Thdclki0		18	–	ns	
DCLKI "L"width	Tldclki0		18	–	ns	
DCLK frequency	Tldclk0	DCLK (internal)	–	54	MHz	*1
DCLKO frequency	Fdclko0	DCLKO	–	54	MHz	*2

*1: The internal display clock of PLL synchronous mode is generated with internal PLL of display clock prescaler.

*2: DCLKI or PLL internal display clock is output.

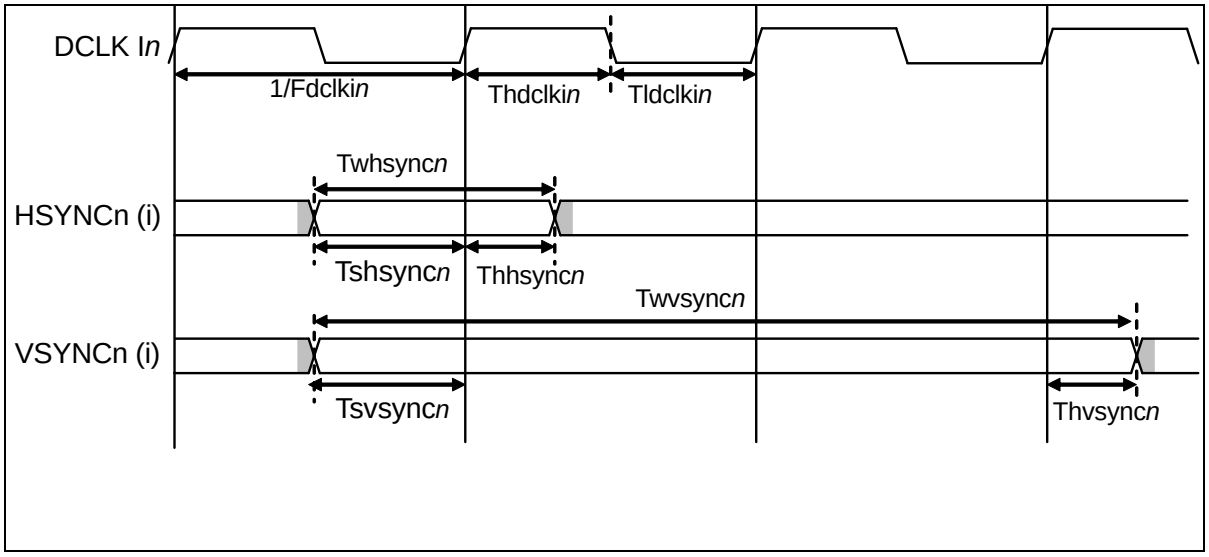
Apply only DCLKI synchronous mode. (reference clock= DCLKI)

- AC timing of video interface input signal

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
HSYNC input setup time	Tshsync0	HSYNC(i)	4	–	–	ns	
HSYNC input hold time	Thhsync0		1	–	–	ns	
VSYNC input pulse width	Twvsync0	VSYNC(i)	1	–	–	HSYNC	

■Display input signal timing



AC Characteristics of Display Output Signal

■Clock Mode

There are multiple clock modes for display output clocks, as shown in Table 1. The AC timing parameters vary depending on modes. The AC timing parameters are specified for each mode.

Table 1. Clock Mode for Display Output

Setting Register Bit Field				Clock Mode Name
DCM1	DCM3			
CKS	DCKed	DCKD	DCKinv	
0	0	0	0	Built-in PLL standard mode
0	0	0	1	Built-in PLL reverse edge mode
0	1	0	0	Cannot be used.
0	1	0	1	
0	0	Other than 0	0	Built-in PLL delay mode
0	0	Other than 0	1	Built-in PLL reverse edge and delay mode
0	1	Other than 0	0	Built-in PLL both edge and delay mode
0	1	Other than 0	1	
1	0	0	0	DCLKI input standard mode
1	0	0	1	DCLKI input reverse edge mode
1	1	0	0	Cannot be used.
1	1	0	1	
1	0	Other than 0	0	
1	0	Other than 0	1	
1	1	Other than 0	0	
1	1	Other than 0	1	

■AC Timing Parameters

This section describes parameters used for AC timing specifications. Select whether you use the DCLKO reverse edge mode, depending on the use/non-use of delay mode.

When the delay mode is not used:
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

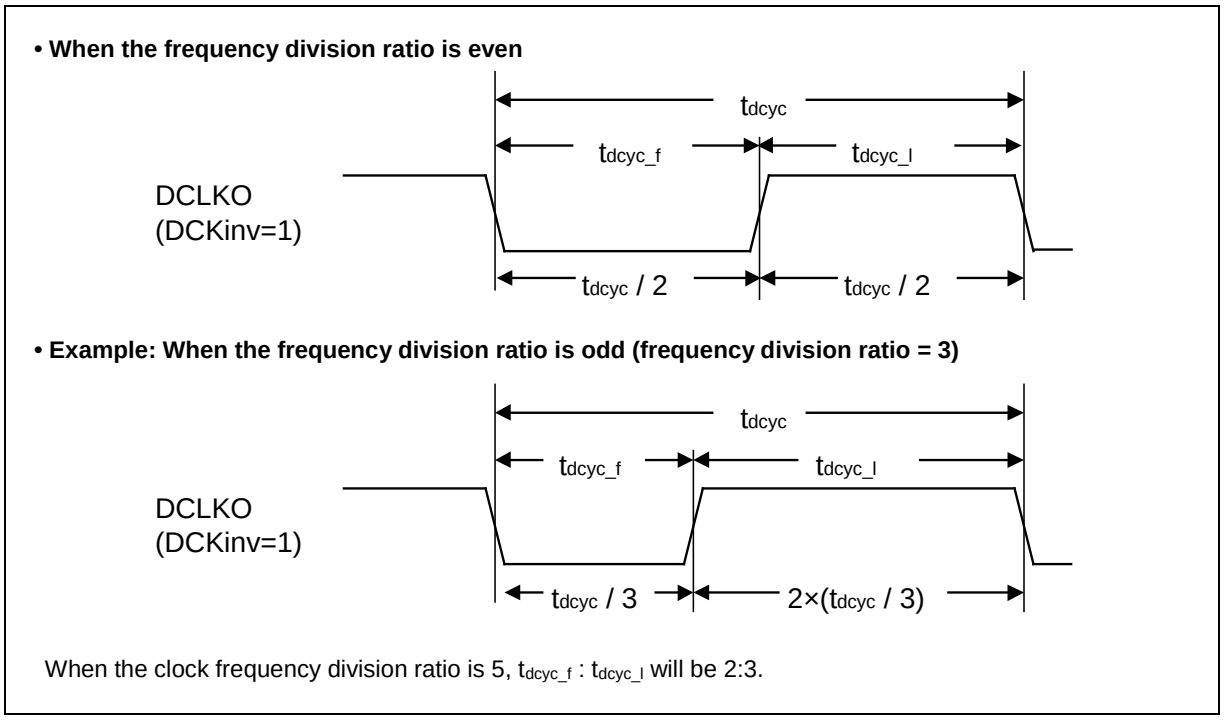
When the delay mode is used:
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

Note: Clock duty ratio when the clock frequency division ratio is even or odd

AC specifications use the half-cycle of the display output clock DCLKO as a parameter. In AC specifications, the first half-cycle is indicated as t_{dcyc_f}, and the second half-cycle is indicated as t_{dcyc_l}.

Note that clock duty ratio will not be 50%:50% when the clock frequency division ratio (specified in SC field of DCM1 register) is odd. If the clock frequency division ratio is odd, the first half-cycle t_{dcyc_f} becomes different from the second half-cycle t_{dcyc_l}.

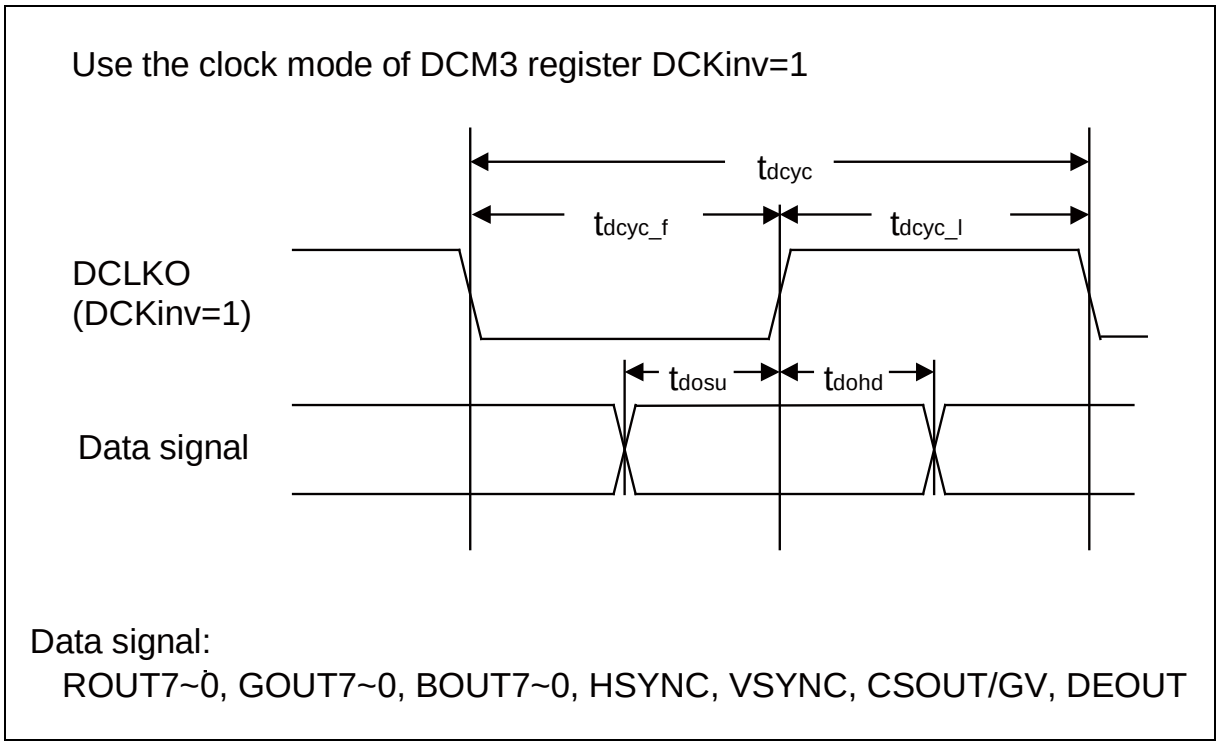
Figure 2. Clock Duty Ratio when the Clock Frequency Division Ratio is even or Odd



Built-in PLL reverse edge mode (DCM3.DCKinv=1)

Figure 3 shows the setup/hold definition when the external display device receives the signal at the rising edge of DCLKO.

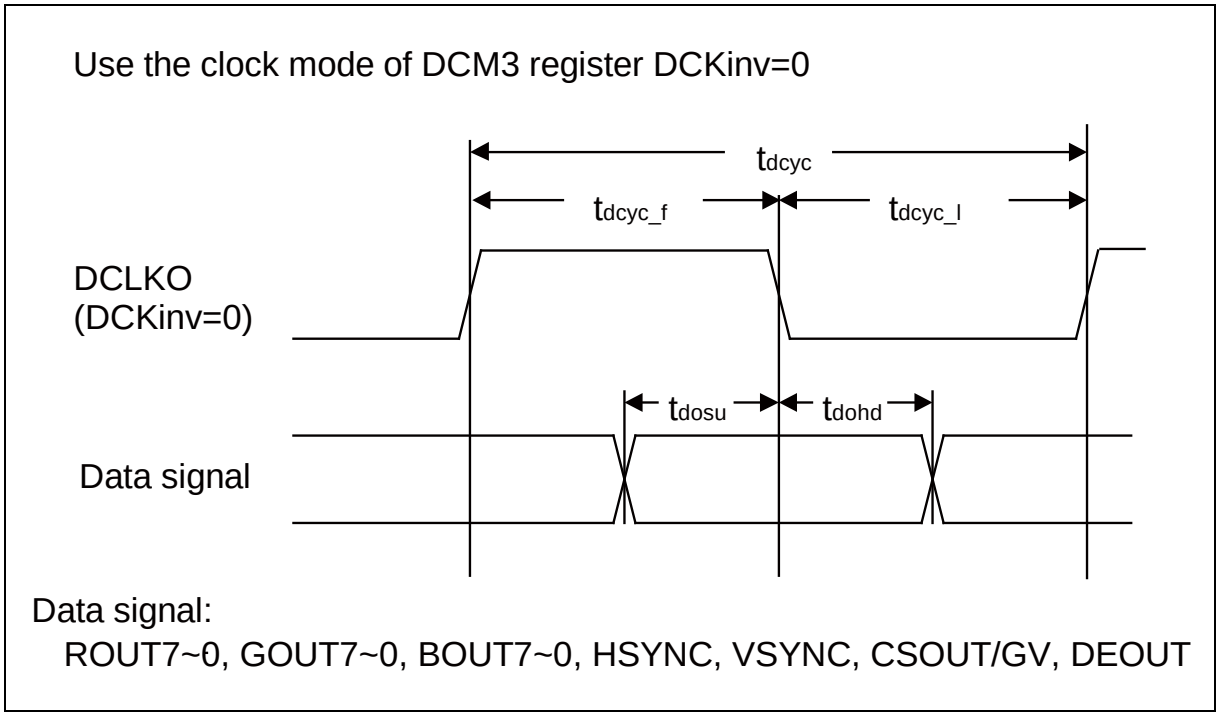
Figure 3. Built-in PLL Reverse Edge Mode Setup/Hold Definition



Built-in PLL standard mode (DCM3.DCKinv=0)

Figure 4 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO.

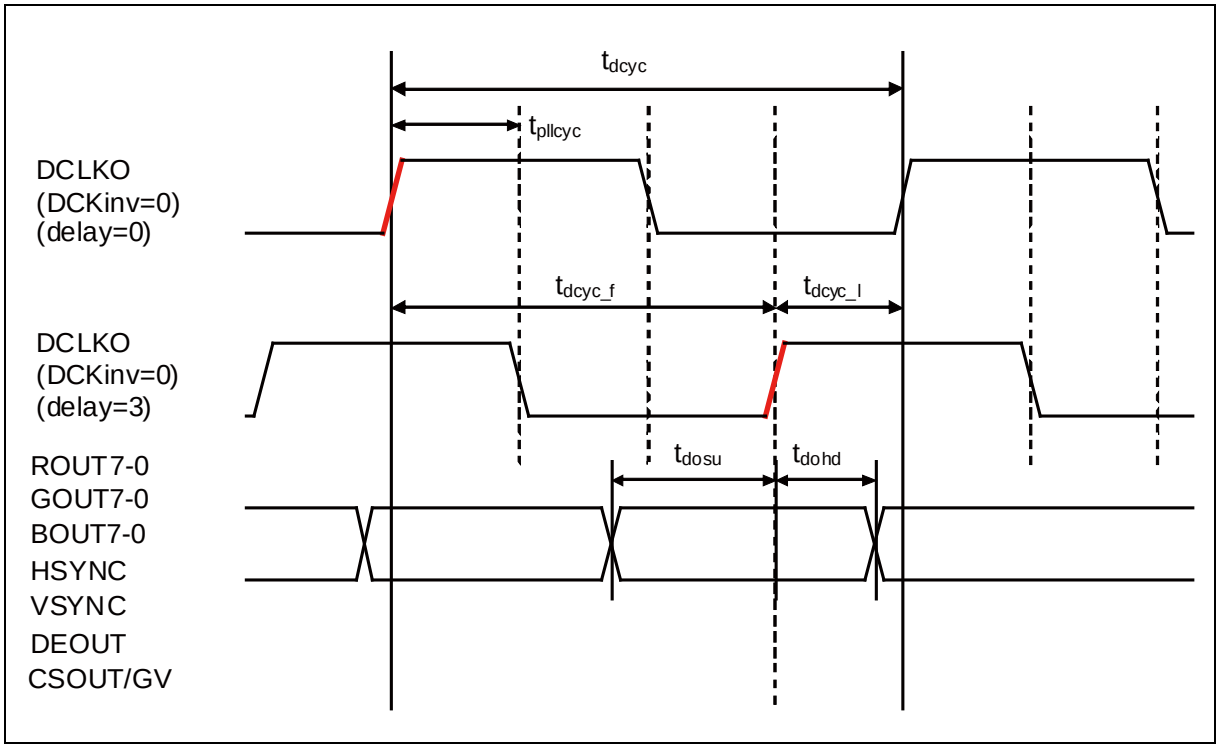
Figure 4. Built-in PLL Standard Mode Setup/Hold Definition



Built-in PLL delay mode (DCM3.DCKinv=0)

Figure 5 shows the setup/hold definition when the external display device receives the signal at the rising edge of DCLKO. (Example: When frequency division ratio = 4)

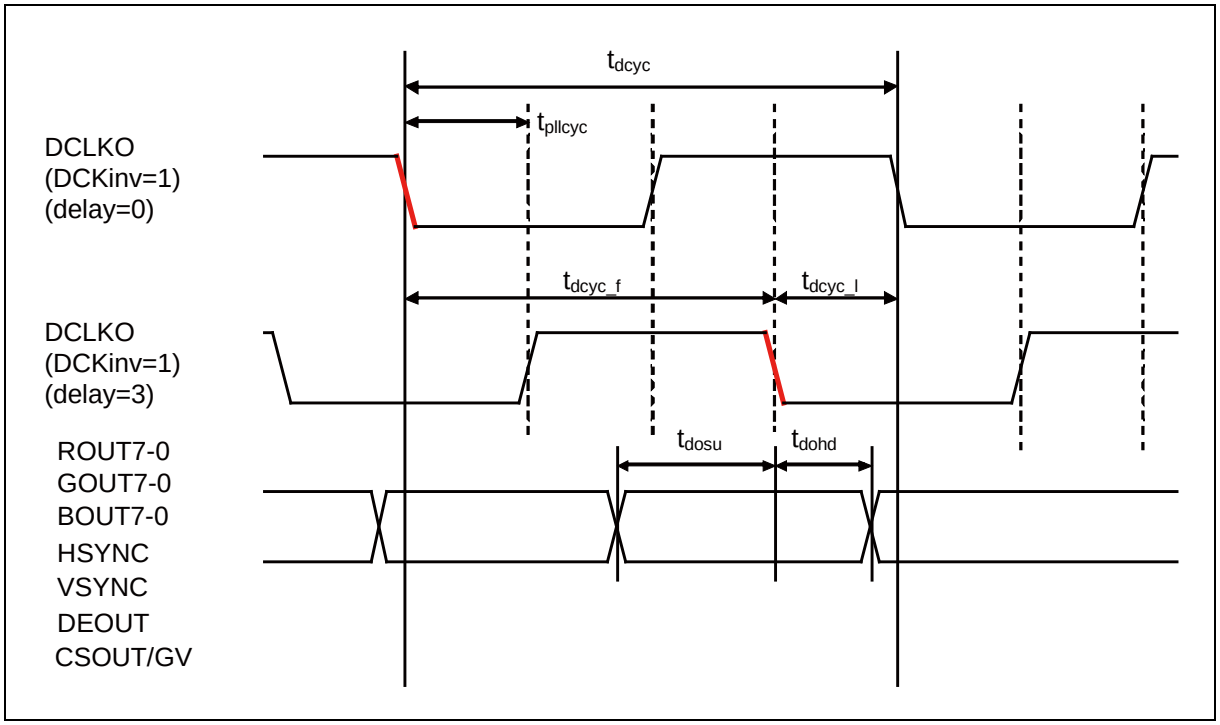
Figure 5. Built-in PLL Delay Mode Setup/Hold Definition



Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

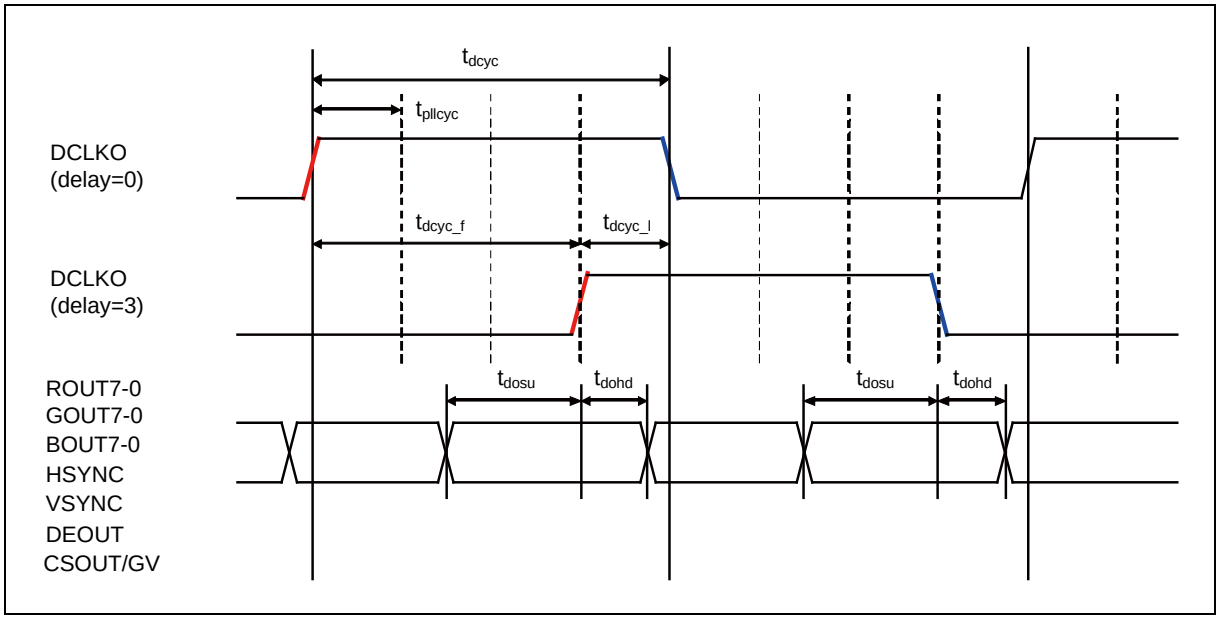
Figure 6. Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



Setup/Hold Definition in Delay Mode

The delay mode is a mode realized with DCLKO delay function, and it can provide delay to DCLKO signal output itself. This can be used when both the following conditions are satisfied.

- The internal PLL is used to generate DCLKO (CKS field of DCM register = 0)
- The frequency division ratio to the internal PLL of DCLKO is 2 or more (SC field of DCM register > 0)

The delay value is set as the unit for internal PLL clock by DCKD field of DCM3 register. The meanings of DCKD setting value are shown below.

When the internal PLL frequency division ratio = 2

DCKD	Delay
000000	No additional delay
000100	+1 PLL clock

When the internal PLL frequency division ratio > 2

DCKD	Delay
000000	No additional delay
000010	+2 PLL clock
000100	+3 PLL clock
000110	+4 PLL clock
:	:
111110	+17 PLL clock

In delay mode, t_{dcyc_f} and t_{dcyc_l} are defined by the delay value above (e.g. "2" of "+2 PLL clock") as shown below.

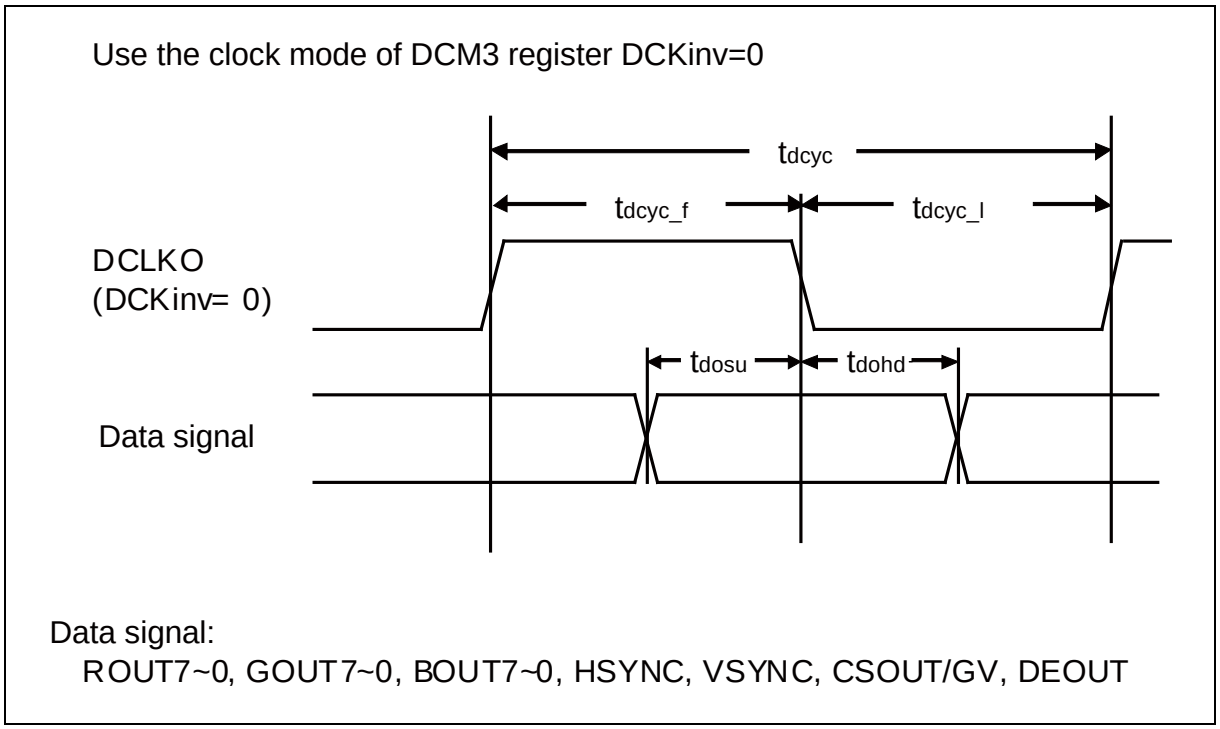
t_{dcyc_f} = Delay value × t_{pllcyc}

$t_{dcyc\_l} = t_{dcyc} - t_{dcyc\_f}$

DCLKI Input Standard Mode (DCM3.DCKinv=0)

Figure 8 shows the setup/hold definition when the external display device (TFT) receives the signal at the falling edge of DCLKO.

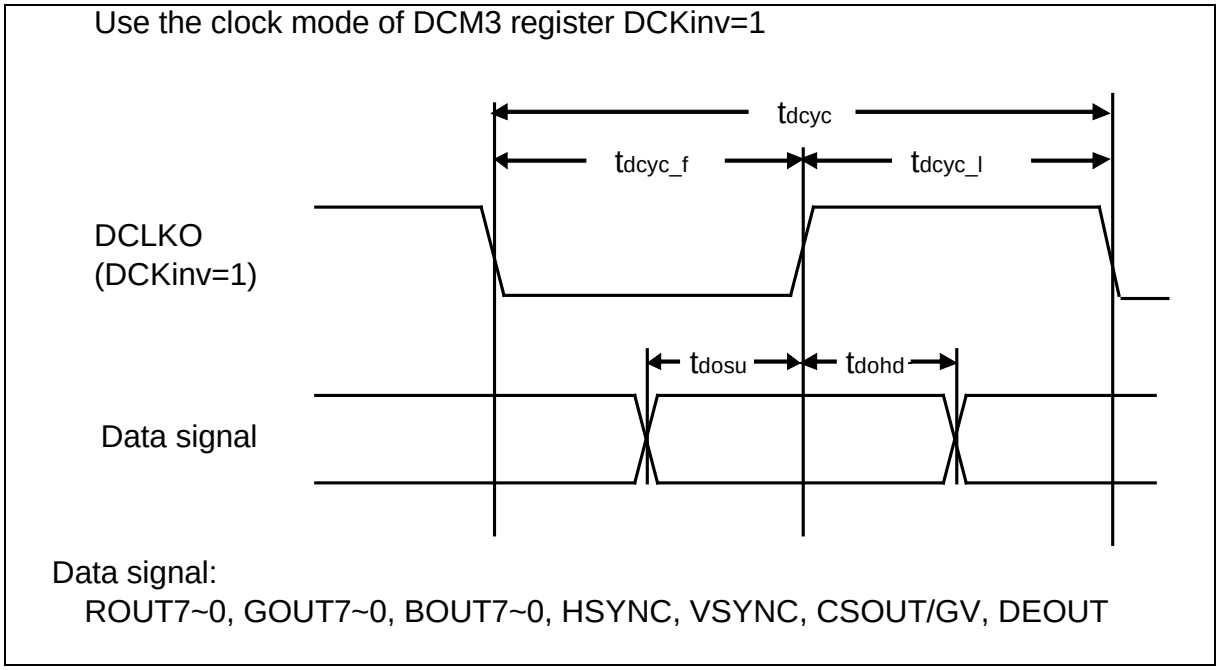
Figure 8. DCLKI Input Standard Mode Setup/Hold Definition



DCLKI Input Reverse Edge Mode (DCM3.DCKinv=1)

Figure 9 shows the setup/hold definition when the external display device (TFT) receives the signal at the rising edge of DCLKO.

Figure 9. DCLKI Input Reverse Edge Mode Setup/Hold Definition



■AC Timing Specifications

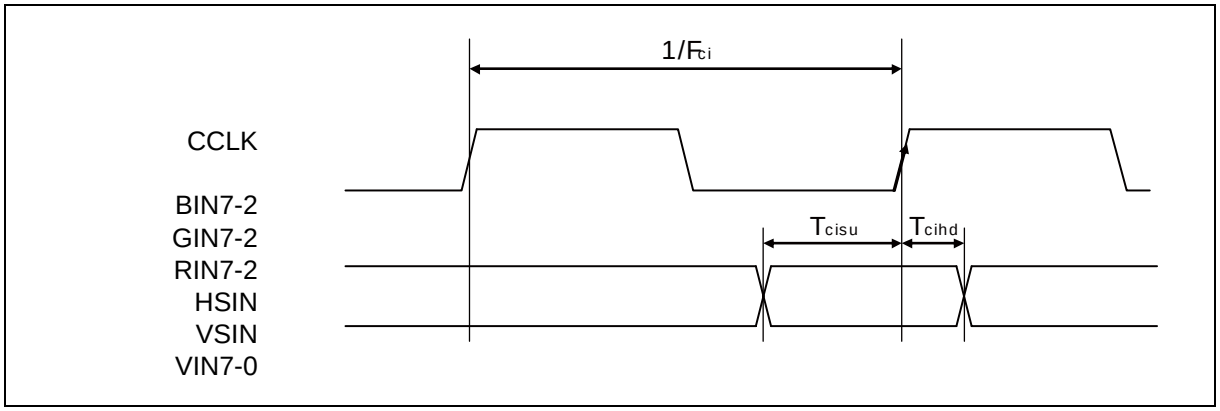
Parameter	Symbol	min.
Display clock cycle time	t_{dcyc}	18.5 ns

External Load Condition 50 pF

Parameter	Symbol	DCLKO Reference Edge	IO Drive Capability Setting		Remark
			10 mA	2 mA	
Setup time	t_{dosu}	neg, pos *1	t_{dcyc}_f - 8.5 ns	t_{dcyc}_f - 10.2 ns	
Hold time	t_{dohd}	-	t_{dcyc}_l - 1.7 ns	t_{dcyc}_l - 3.3 ns	*2
		-	t_{dcyc}_l - 3.2 ns	t_{dcyc}_l – 5.1 ns	*3

*1: DCLKO reference edge: This is the reference clock edge for setup time and hold time.
Pos = The external display device receives the signal at the rising edge of DCLKO.
Neg = The external display device receives the signal at the falling edge of DCLKO.
*2: Should be applied to RGB666.
*3: Should be applied to RGB888.

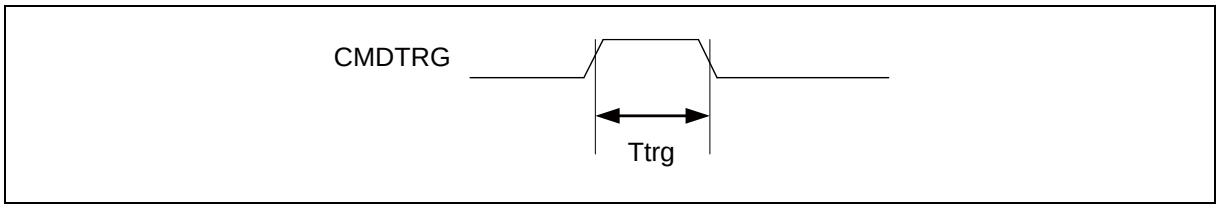
Video Capture Input



Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Capture input frequency	Fci	CCLK	–	81.0	MHz	
Capture input setup time	Tcisu	BIN7-2, GIN7-2, RIN7-2, HSIN, VSIN, VIN7-0	3.0	–	ns	
Capture input hold time	Tcihd		0.0	–	ns	

11.4.1.14 GDC ommand trigger signal

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input trigger pulse width	Ttrg	CMDTRG	160	–	ns	



11.5 A/D Converter

11.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, $V_{CC}5=AV_{CC}5=5.0V \pm 10\%$, $V_{SS}=AV_{SS}=0.0V$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	±3	LSB	
Non linearity error	–	–	–	–	±2.5	LSB	
Differential linearity error	–	–	–	–	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS} - 1.5LSB	–	AV_{SS} + 2.5LSB	V	1LSB = (AV_{CC} - AV_{SS}) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH5 - 3.5LSB	–	AVRH5 + 0.5LSB	V	
Sampling time	t_{SMP}	–	1.2	–	–	µs	*1
Compare time	t_{CMP}	–	1.8	–	–	µs	*1
A/D conversion time	t_{CNV}	–	3.0	–	–	µs	*1
Analog port input current	I_{AIN}	AN0 to AN31	-5	–	+5	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	AV_{SS}	–	AVRH5	V	
Reference voltage	A_{VRH}	AVRH5	4.5	–	5.5	V	AVRH5 ≤ AV_{CC}5
	A_{VRL}	AVSS	–	0.0	–	V	
Power supply current	I_A	AVCC	–	–	4.0	mA	
	I_{AH}		–	–	6.0	µA	*2
	I_R	AVRH5	–	600	900	µA	
	I_{RH}		–	–	5	µA	*2
Variation between channels	–	AN0 to AN31	–	–	4	LSB	

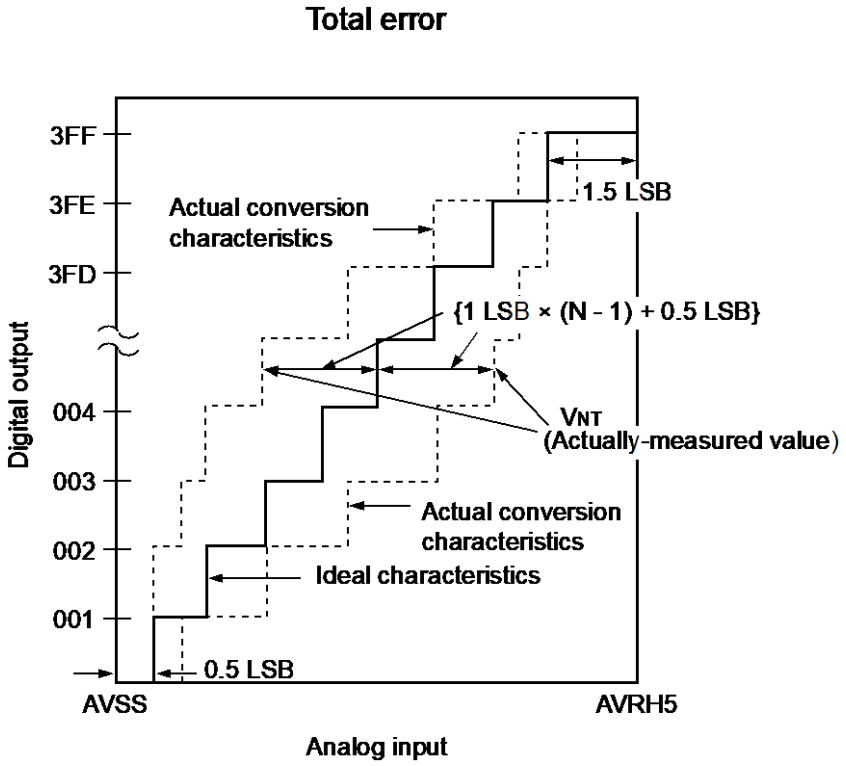
*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

Note:
Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.

11.5.2 Definition of A/D Converter Terms

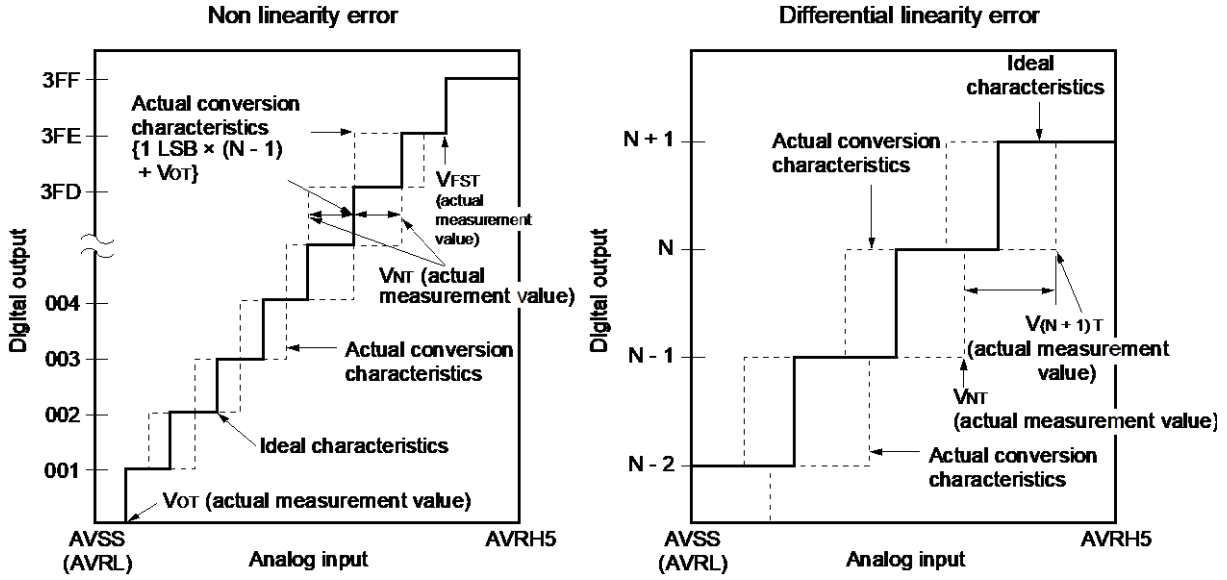
Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("00 0000 0000"← →"00 0000 0001") to the full-scale transition point ("111111 1110"← →"11 1111 1111").
Differential linearity error	:	Deviation of the input voltage from the ideal value that is required to change the output code by LSB.
Total error	:	Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB\} \times (N - 1) + 0.5LSB\}}{1LSB} \text{ [LSB]}$$

$$1LSB \text{ (Ideal value)} = \frac{AVRH5 - AVSS}{1024} \text{ [V]}$$

N: A/D converter digital output value.
V_{OT} (Ideal value) = AVSS + 0.5 LSB[V]
V_{FST} (Ideal value) = AVRH5 - 1.5 LSB[V]
V_{NT}: Voltage at which the digital output changes from (N - 1) to N.



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1LSB\} \times (N - 1) + V_{OT}}{1LSB} \text{ [LSB]}$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022} \text{ [V]}$$

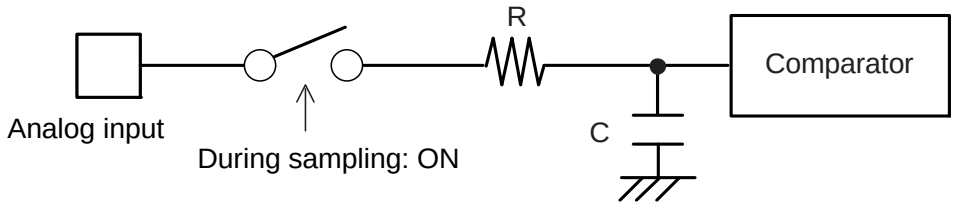
V_{OT} : Voltage at which the digital output changes from "000_H" to "001_H".
V_{FST} : Voltage at which the digital output changes from "$3FE_H$" to "$3FF_H$".

11.5.3 Notes on Using A/D Converter

<About the output impedance of the analog input of external circuit>

- External impedance values of the external input of 4.2 kΩ or lower (sampling time = 1.2 µs@ machine clock of 16 MHz) are recommended. When the external impedance is too high, the sampling time for analog voltages may not be sufficient. In this case, it is recommended to connect the capacitor (approx. 0.1 µF) to the analog input pin.

• Analog Input Circuit model



	R	C
CY91590series	4.0kΩ (Max)	16.1pF (Max)

Note: Listed values must be considered as reference values.

11.6 Flash Memory

11.6.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbyte sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbyte sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbyte sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbyte sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

11.6.2 Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc5) is prohibited.
In the application system where Vcc5 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.
To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc5 at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] x 257) + 50 [µs]

*: See " AC Characteristics Low voltage detection (External low-voltage detection) "

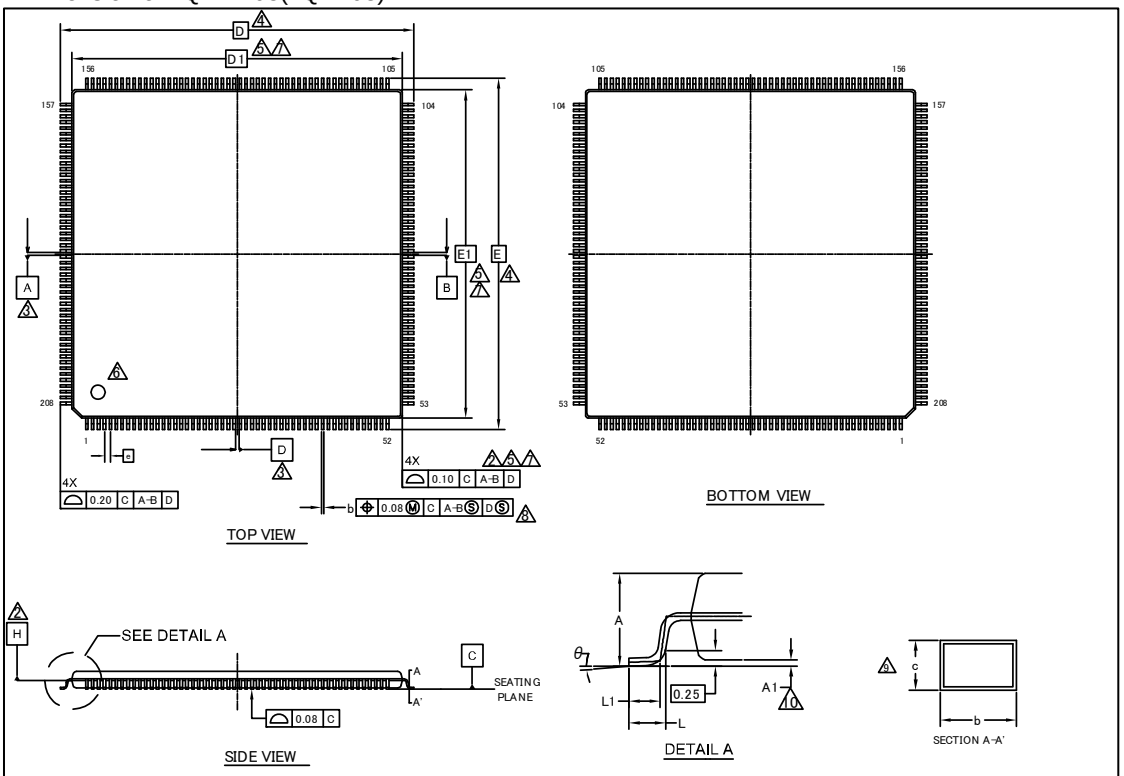
12. Ordering Information

Part Number	Package[*1]
CY91F591BHSPMC-GSE2	208-pin plastic LQFP (LQR208)
CY91F591BSPMC-GSE2	
CY91F592ASPMC-GSE1	
CY91F592BHPMC-GSE1	
CY91F592BHPMC-GSE2	
CY91F592BHSPMC-GSE1	
CY91F592BHSPMC-GSE2	
CY91F592BSPMC-GSE1	
CY91F592BSPMC-GSE2	
CY91F594BHPMC-GSE1	
CY91F594BHSPMC-GSE1	
CY91F594BHSPMC-GSE2	
CY91F594BPMC-GSE1	
CY91F594BSPMC-GSE1	
CY91F594BSPMC-GSE2	
CY91F59BCEQ-GSE1	208-pin plastic TEQFP (LET208)
CY91F59BCPB-GSE1	320-Ball Grid Array Package (BYA320)

[*1]: For details of the package, see "Package Dimensions ".

13. Package Dimensions

■Dimension of LQFP-208(LQR208)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.00 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

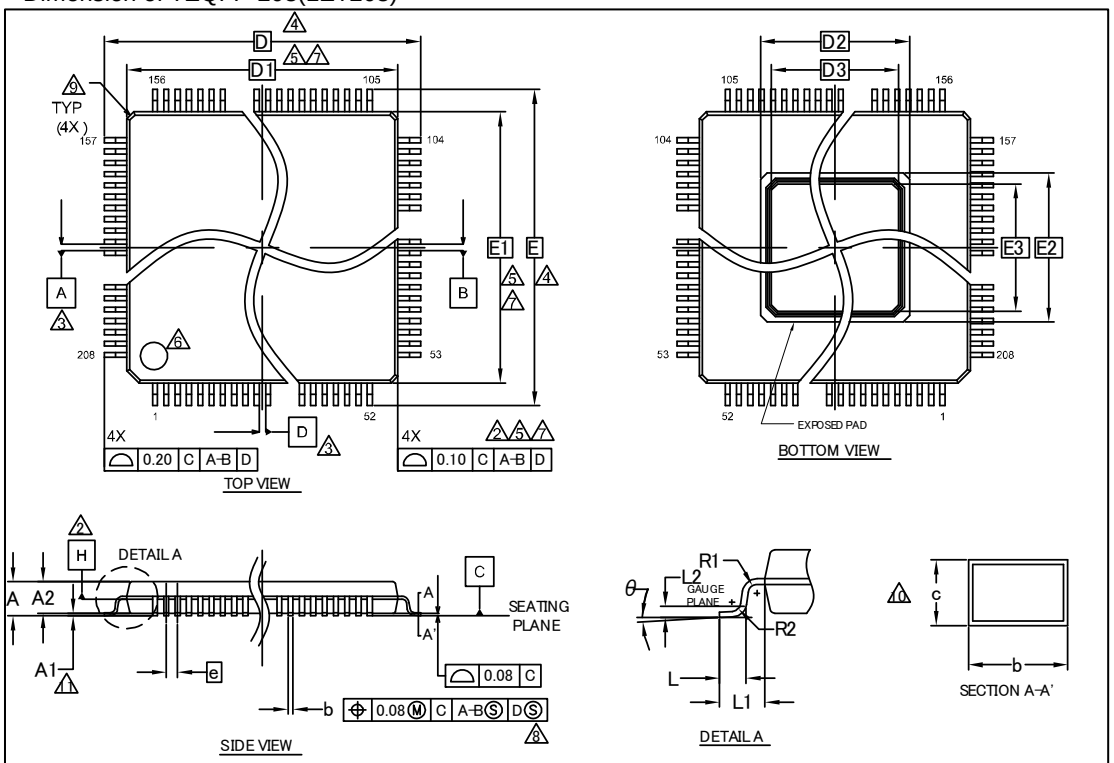
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15151 **

PACKAGE OUTLINE, 208 LEAD LQFP
28.0X28.0X1.7 MM LQR208 REV**

■Dimension of TEQFP-208(LET208)



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D	30.00 BSC		
D1	28.00 BSC		
D2	9.90 REF		
D3	8.71 REF		
E	30.00 BSC		
E1	28.00 BSC		
E2	9.90 REF		
E3	8.71 REF		
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25		
e	0.50 BSC		

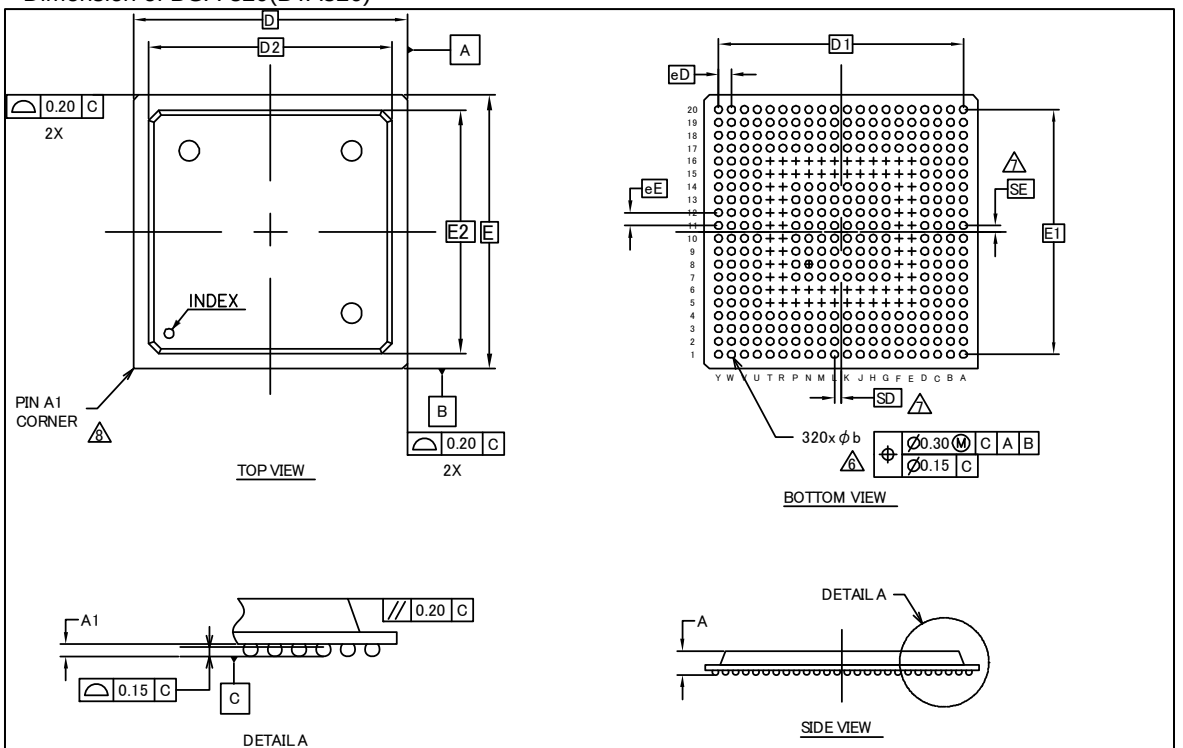
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13651 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LET208 REV*A

■Dimension of BGA-320(BYA320)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	2.46
A1	0.35	——	——
D	27.00 BSC		
E	27.00 BSC		
D1	24.00 BSC		
E1	24.00 BSC		
MD	20		
ME	20		
n	320		
Φb	0.60	0.75	0.90
eD	1.27 BSC		
eE	1.27 BSC		
SD / SE	0.635		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
10. JEDEC SPECIFICATION NO. REF: N/A.

002-16414 **

PACKAGE OUTLINE, 320 BALL FBGA
27.00X27.00X2.46 MM BYA320 REV**

14. Major Changes

Spansion Publication Number: CY91590_DS705-00010

Page	Section	Change Results
Revision 3.1		
-	-	Company name and layout design change

See Supplementary Information as described in Document Definition.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: CY91590 Series FR Family FR81S 32-Bit Microcontroller
Document Number: 002-04727

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NNAS	06/19/2015	Migrated to Cypress and assigned document number 002-04712. No change to document contents or format.
*A	5139796	NNAS	02/19/2016	Updated to Cypress format.
*B	5973870	HMIZ	12/01/2017	12. Ordering Information [Improve] Updated "Ordering Information" [Improve] Delete *2: Under consideration
				13. Package Dimensions [Improve] Updated PKG figure for LQR208, LET208 and BYA320
				Updated Sales page.
*C	6557020	TORS	05/07/2019	Changed series name and part number: MB91590 -> CY91590 Updated Ordering Information.

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