Application Note 370
Using RCLK in a BITS/SSU Application

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OVERVIEW

This application note discusses how to use the recovered clock from a T1 or E1 span in a timing distribution application. The BITS (building integrated timing supply) is one type of clock that is used extensively in network synchronization. It is a master timing supply for all deployed equipment within a network requiring synchronization. The term BITS is used in North America, but the rest of the world refers to this type of clock as a Synchronization Supply Unit (SSU). The Dallas Semiconductor single-chip transceivers (SCTs) and line interface units (LIUs) are excellent candidates for the front end of a BITS/SSU application or other timing distribution models based on DS1 (T1) or E1 traffic.

SYNCHRONIZATION STANDARDS

ITU-T, ANSI, ETSI and Telcordia maintain requirements (Tables 1 and 2) for timing and network synchronization. Within these documents, clocks are divided into different levels, or Stratums, that define the accuracy and stability for the timing. In the ANSI specifications, the most accurate clock level, Stratum 1, is defined as a free-running clock with accuracy of better than $1x10^{-11}$. Cesium clocks are an example of a Stratum 1 clock. Stratum 2 (Type II clocks in ITU-T specs) is the next level of clocks, followed by Stratum 3 (Type IV) and Stratum 4. Stratum 3E (Type III) was introduced as a level of timing between Stratum 2 and 3 and is typically used in SONET and SDH.

Table 1. North American Synchronization Standards

SPEC	TITLE
ANSI T1.101	Synchronization Interface Standards
GR-378-CORE	Generic Requirements for Timing Signal Generators
GR-436-CORE	Digital Network Synchronization
GR-253-CORE	Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria
GR-1244-CORE	Clocks for the Synchronized Network: Common Generic Criteria
GR-2830-CORE	Primary Reference Sources: Common Generic Criteria

Table 2. ITU Synchronization Standards

SPEC	TITLE
G.703	Physical/Electrical Characteristics of Hierarchical Digital Interfaces
G.704	Synchronous Frame Structures Used at 1544, 6312, 2048, 8488, and 44736kbps Hierarchical Levels
G.810	Definitions and Terminology For Synchronized Networks
G.811	Timing Characteristics of Primary Reference Sources
G.812	Timing Requirements for Slave Clocks for use as Node Clocks in Synchronized Networks
G.813	Timing Characteristics of SDH Equipment Slave Clocks
G.824	Control of Jitter and Wander Within Digital Networks That are Based on the 1544kbps Hierarchy

Table 3. Some Parameters from the ANSI/ITU-T Clock Specification

ANSI Clock	Stratum 1 (PRS)	Stratum 2	Stratum 3E	Stratum 3	Stratum 4
ITU-T Clock	PRC	Type II	Type III	Type IV	Not Defined
Accuracy	1×10^{-11}	1.6×10^{-8}	4.6×10^{-6}	4.6×10^{-6}	3.2×10^{-5}
Holdover Stability	Not Defined	1.6×10^{-9}	1.2×10^{-8}	3.9×10^{-7}	Not Required
Pull-in Range	Not Defined	1.6×10^{-8}	4.6×10^{-6}	4.6×10^{-6}	3.2×10^{-5}

Table 3 shows some of the parameters for several types of clocks as defined in T1.101-1999, G.811, and G.812. Included in Table 3 is the holdover stability and pull-in range. Holdover is discussed in the next section (BITS/SSU). The pull-in range refers to the largest offset that the nominal and reference frequencies are allowed so that the clock remains in a locked state.

In addition to the stratum levels, other clock performance levels have been defined. Primary reference sources (PRS) or clocks (PRC), defined in GR-2830-Core and G.811, must maintain the same accuracy as Stratum 1 clocks, but unlike Stratum 1 clocks, a PRS can be steered. Global positioning systems and LORAN-C systems are examples of PRS that are not considered Stratum1 clocks because they steer very accurate oscillators (e.g., rubidium) to produce the timing. Additionally, ANSI specifies a TNC and Stratum 4E clock. ITU-T defines types I through VI in G.812 and two separate options for SDH equipment slave clocks in G.813.

BITS/SSU

Network synchronization is critical to ensure that the quality of transmission is maximized. Without proper synchronization, timing slips can occur between the subnetworks that are timed differently. These slips degrade the quality of the networks. BITS and SSU clocks have been extensively used to achieve network synchronization. These clock distribution methods are based on a hierarchical structure in which timing is passed down from a master timing source, a Stratum I or PRS/PRC clock, to slave clocks (BITS/SSU). The slave clocks can pass timing information down to other slave clocks with the stipulation that the highest performance clocks are at the top of the clock distribution network.

The BITS extracts the timing information from an incoming DS1 signal and typically supply DS1 and/or DS0 timing levels to the network. The incoming DS1 signal can carry traffic or just timing information; but, by using a dedicated timing line, performance, maintenance, and reliability of the BITS clock can be increased. The SSU works in the same manner as the BITS clock except that E1 timing levels are used. The signal that is selected for the primary clocking source of the BITS should provide the best level of clock available. Line length, downtime, and jitter are line characteristics that should be considered when selecting the primary clock.

The BITS/SSU clock is a slave clock and is defined to have three basic modes of operation: locked, free-run, and holdover. In locked mode, the output of the slave clock is considered “synchronized” with the input clock, such that the average frequency of the input and output clocks are identical. This mode of operation is the normal condition for a slave clock.

If the input reference is lost the slave clock can enter a holdover state. The holdover state is achieved by using stored data, acquired during locked mode, to control the frequency and phase of the output clock. In this mode, the output clock is a reproduction of what was the input reference. The specifications vary for this mode of operation in each of the timing levels (Table 3). A transition back to the locked mode would occur when the input reference is available again.

The final mode of operation is called free-run. This output clock in this mode of operation is based on the oscillating element of the slave clock and not the input reference or stored data. This mode is the typical mode of operation when the slave clock is first powered on. It is also achieved when there is no stored data available in which to transition to the holdover state.

The DS2155

In this example, we use the DS2155 to recover the incoming clock and to transmit the BITS to another piece of equipment. The DS2155 is a truly software selectable T1, J1, or E1 single-chip transceiver for short-haul and long-haul applications. (See the DS2155 data sheet on the web at www.maxim-ic.com/DS2155.) In addition to T1/E1/J1 operation from a single MCLK frequency, the DS2155 offers internal software-selectable transmit- and receive-side termination resistors for 75Ω/100Ω/120Ω T1 and E1 interfaces. The LIUs’ receive sensitivity adjusts automatically

to the incoming signal and can be programmed for 0 to 43dB or 0 to 12dB for E1 applications and 0 to 30dB or 0 to 36dB for T1 applications. T1 waveform generation includes DSX-1 line build-outs of -7.5dB, -15dB, and -22.5dB. E1 waveform generation includes G.703 (synchronization signal) waveshapes for both 75Ω coax and 120Ω twisted cables. This synchronization signal is used in timing applications for E1 because of its simple square wave running at 2.048MHz with no performance messages and/or framing information. The DS2155 is capable of transmitting or receiving the G.703 synchronization signal. When receiving, this signal appears as an all-ones pattern with constant bipolar violations.

The framer of the DS2155 locates the frame and multiframe boundaries and monitors the data stream for alarms. It is also used for extracting and inserting signaling data, T1 FDL data, and E1 Si and Sa bit information. The functionality of the DS2155 makes inserting and extracting Synchronization Status Messages (SSM) easy. These messages are used in BITS/SSU applications to pass information about type of clocks timing that is being sent or received. Dual on-board HDLC controllers can be used for the FDL, Sa bit links, or individual or multiple DS0s. Diagnostic capabilities include loopbacks, PRBS pattern generation/detection, and 16-bit loop-up and loop-down code generation and detection.

USING RCLK IN A BITS APPLICATION

In this example, we use the DS2155, but any of the Dallas SCT (e.g., DS21x52, DS21x54, DS2152, DS2154) or LIU (e.g., DS2148, DS21348, DS2149, DS21349) products could be used to recover the clock from the incoming signal. However, to be fully compliant with the Telcordia and ITU recommendations, a framer and LIU are needed for performance and status information. For example, the DS2148 (T1/E1/J1 LIU) could be used to recover the clock and any of framers (e.g., DS2141, DS21Q41, DS2143, DS21Q44) could be used to receive and transmit the additional information required by the BITS specifications.

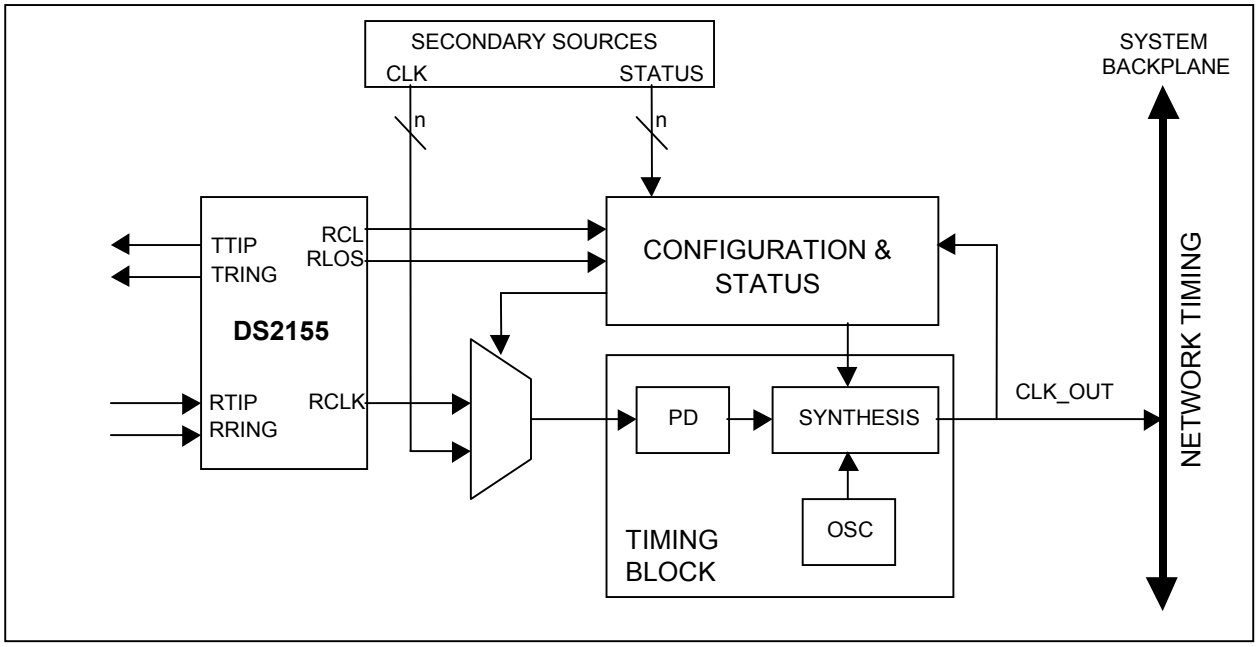
Figure 1 shows one method for creating a BITS clock. The recovered clock (RCLK) from the DS2155 is used as an input to a timing block that distributes the clock to the network. When possible, one or more secondary clock sources should be made available to the timing module. The secondary clock could be another RCLK from a different DS2155 or the output clock from a different timing block. For cases where one wishes to create a Stratum 4 backplane, the timing module would not be needed and the recovered clock (RCLK) would be sufficient.

If the primary timing reference is lost and a secondary source of timing is available, the secondary source is switched into the timing block through a multiplexer. The timing block's function is to lock to the incoming timing source and generate a clock. If a carrier loss condition occurs, meaning that no timing source is available, the timing block must be capable of entering a holdover state clock in which timing data stored while a timing reference was available is used to control the output clock frequency. In addition to the holdover requirement, if no external references to the timing block are available and no timing history has been collected, the timing block would enter free-run mode. In this mode of operation, the output clock frequency would be generated from the oscillator located within the timing block.

All of Dallas' transceivers have an internal PLL that reduces the need for holdover and free-run operation within the timing block. In the event of a receive carrier loss (RCL) condition, also referred to as an LOS (loss of signal), which occurs when there is no signal present on the analog inputs (RTIP, RRING) of the clock recovery circuitry, the DS2155's PLL gradually transitions from the incoming span's recovered clock to a 1.544MHz (or 2.048MHz in E1 operation) that is derived from the MCLK input. Therefore, in this mode of operation the holdover stability of RCLK would be dependent upon the clock supplied at MCLK. Also, to avoid introducing wander into the network, the transceivers' jitter attenuator should be disabled (LICR.1 = 1).

The status and configuration block is used to monitor the RCL (receive carrier loss) and RLOS (receive loss of sync) output pins of the DS2155 and status information from the secondary sources. The RCL pin goes high when an RCL condition occurs and the RLOS pin goes high when the synchronizer is searching for the frame and multiframe. These pins can be used as an indicator when to switch over to a secondary transceiver, another source of timing, or place the BITS into holdover mode. In the event that no external references are available and no timing history has been collected, the timing block would enter free-run mode. In this mode of operation, the output clock frequency would be generated from the oscillator located within the timing block.

Figure 1. Block Diagram



SYNCHRONIZATION STATUS MESSAGES (SSM)

In addition to timing, the incoming line can carry synchronization status messages, or SSM. These messages, defined in ANSI (T1.105) and ITU-T (G.703) recommendations, identify the quality level of the incoming clock. Information on when and how to produce these messages and what actions to take when receiving them can be found in TR-33, GR-253-Core, and GR-378-CORE for T1 operation, and G.781 and ETSI 300 417-6-1 for E1. These code words are transmitted as bit oriented code words (BOCs) in the data link bits (DS1 ESF) or by using one of the 5 Sa bits (E1). The DS2155's HDLC controllers could be used to transmit and receive the SSMs in both T1 and E1 mode, but easier ways are available.

In T1 mode, the DS2155 contains a BOC generator on the transmit side and a BOC detector on the receive side that makes transmitting and receiving these messages simple. Table 1 shows the codes defined for SSMs in T1 operation. A SSM is valid when 7 of 10 messages are alike. The HDLC controllers of the DS2155 are also available to transmit and receive messages using the FDL, but the use of the BOC engine of the DS2155 is the recommended method. For information on using the HDLC controllers to pass SSMs, please contact the factory at https://support.maximintegrated.com/.

To transmit a BOC message, bits 0 through 5 in the TFDL register should be loaded with the message to be transmitted. The message is transmitted as 0xxxxxx0 11111111, where the x's represent the actual SSM. The transmit BOC controller automatically handles the surrounding zeros and the abort sequence (FFh). In Table 4, the six bits that are bold and italicized in the FDL Code Word column are the bits that will be loaded into the TFDL register. Setting bit 0 of the BOCC register to 1 causes the transmit BOC controller to immediately begin inserting the BOC sequence into the FDL bit position. BOC messages are transmitted as long as this bit is set.

The receive BOC function is enabled by setting bit 4 in the BOCC register to 1. The RFDL register will then operate as the receive BOC message and information register. The lower six bits of the RFDL register (BOC message bits) are preset to all ones. When the BOC bits change state, the BOC change of state indicator, located in bit position 0 of status register 8 (SR8.0), alerts the host. The host can then read the RFDL register to get the BOC message. A change of state occurs when either a new BOC code has been present for time determined by the receive BOC filter bits, RBF0 and RBF1, in the BOCC register.

Table 4. Synchronization Status Message Codes for T1 Operation

QUALITY LEVEL	DESCRIPTION	FDL CODE WORD (DS1 ESF)
1	Stratum 1 Traceable	0 ***000010*** 0 11111111
2	Synchronized Traceability Unknown	0 ***000100*** 0 11111111
3	Stratum 2 Traceable	0 ***000110*** 0 11111111
4	Stratum 3 Traceable	0 ***001000*** 0 11111111
5	SONET Minimum Clock Traceable	0 ***010001*** 0 11111111
6	Stratum 4 Traceable	0 ***010100*** 0 11111111
7	Do not Use for Synchronization	0 ***011000*** 0 11111111
User Assignable	Reserved for Network Synchronization Use	0 ***100000*** 0 11111111

Table 5. Summary of Procedures to Transmit and Receive BOC Messages

To transmit a SSM:
1) Write 6-bit code into the TFDL register. 2) Set SBOC bit in BOCC register to 1.
To receive a SSM:
1) Set integration time via BOCC.1 and BOCC.2. 2) Enable the receive BOC function (BOCC.4 = 1). 3) Enable BOC change of state interrupt (IMR8.0 = 1) 4) Wait for interrupt to occur. Read status register to verify event. (SR8.0 = 1) 5) Read the RFDL register. The lower six bits of the RFDL register is the message.

Note: The registers shown below are used when transmitting and receiving SSMs are done via the BOC controller. These register descriptions can also be found in the DS2155 data sheet.

Register Name: BOCC, BOC Control Register, Address 37h

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	RBOCE	RBR	RBF1	RBF0	SBOC

Bit 0: Send BOC

0 = Do not send BOC code.
1 = Transmit the BOC code placed in bits 0 to 5 of the TFDL register.

Bits 1 and 2: Receive BOC Filter Bits (RBF0, RBF1). The BOC filter sets the number of consecutive patterns that must be received without error prior to an indication of a valid message.

RBF1	RBF0	Consecutive BOC codes for valid sequence identification
0	0	None
0	1	3
1	0	5
1	1	7

Bit 3: Receive BOC Reset (RBR). A 0-to-1 transition resets the BOC circuitry. This bit must be cleared and set again for a subsequent reset.

Bit 4: Receive BOC Enabled (RBOCE). Enables the receive BOC function. The RFDL register reports the received BOC code and two information bits when this bit is set.

0 = Receive BOC function disabled.
1 = Receive BOC function enabled. The RFDL register reports BOC messages and information.

Bit 5: Unused, must be set to zero for proper operation.

Bit 6: Unused, must be set to zero for proper operation.

Bit 7: Unused, must be set to zero for proper operation.

Register Name: TFDL, Transmit FDL Register, Address C1h

(*Note: This shows the TFDL register bit usage when SBOC (BOCC Register, Bit 0) is set to 1.)*

Bit #	7	6	5	4	3	2	1	0
Name	—	—	TBOC5	TBOC4	TBOC3	TBOC2	TBOC1	TBOC0

Bits 0 to 5: Transmit BOC bits 0 through 5 (TBOC0-TBOC5).

Bits 6, 7: This bit position is unused when BOCC.0 (SBOC) = 1.

Register Name: RFDL, Receive FDL Register, Address C0h

(*Note: This shows the RFDL register bit usage when RBOCE (BOCC Register, Bit 4) is set to 1.)*

Bit #	7	6	5	4	3	2	1	0
Name	—	—	RBOC5	RBOC4	RBOC3	RBOC2	RBOC1	RBOC0

Bits 0 to 5: Received BOC bits 0 through 5 (RBOC0-RBOC5).

Bits 6, 7: This bit position is unused when BOCC.4 (RBOCE) = 1.

Register Name: SR8, Status Register 8, Address 24h

Bit #	7	6	5	4	3	2	1	0
Name	—	—	BOCC	RFDLAD	RFDLF	TFDLE	RMTCH	RBOC

Bit 0: Receive BOC Detector Change of State Event (RBOC). Set whenever the BOC detector sees a change of state to a valid BOC. The setting of this bit prompts the user to read the RFDL register.

Bit 1: Receive FDL Match Event (RBOC). Set whenever the contents of the RFDL register matches the RFDLM1 or RFDLM2 registers.

Bit 2: TFDL Register Empty Event (TFDLE). Set whenever the transmit FDL buffer (TFDL) empties.

Bit 3: RFDL Register Full Event (RFDLF). Set when the receive FDL buffer (RFDL) fills to capacity.

Bit 4: RFDL Abort Detect Event (RFDLAD). Set when 8 consecutive ones are received on the FDL.

Bit 5: BOC Clear Event (BOCC). Set when 30 FDL bits occur without an abort sequence.

Bits 6, 7: Unused.

Register Name: **IMR8, Interrupt Mask Register 4,** Address **25h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	BOCC	RFDLAD	RFDLF	TFDLE	RMTCH	RBOC

Bit 0: Receive BOC Detector Change of State Event (RBOC)
0 = interrupt masked
1 = interrupt enabled

Bit 1: Receive FDL Match Event (RBOC)
0 = interrupt masked
1 = interrupt enabled

Bit 2: TFDL Register Empty Event (TFDLE)
0 = interrupt masked
1 = interrupt enabled

Bit 3: RFDL Register Full Event (RFDLF)
0 = interrupt masked
1 = interrupt enabled

Bit 4: RFDL Abort Detect Event (RFDLAD)
0 = interrupt masked
1 = interrupt enabled

Bit 5: BOC Clear Event (BOCC)
0 = interrupt masked
1 = interrupt enabled

Bits 6–7: Unused. Set to 0 for proper operation.

Table 6. Synchronization Status Message Codes for E1 Operation

QUALITY LEVEL	DESCRIPTION	S_{an1}, S_{an2}, S_{an3}, S_{an4} Where n = bit number 4, 5, 6, 7, or 8
0	Quality unknown (existing sync. network)	0000
1	Reserved	0001
2	Rec. G.811 (Traceable to PRS)	0010
3	Reserved	0011
4	SSU-A (Traceable to SSU type A, see G.812)	0100
5	Reserved	0101
6	Reserved	0110
7	Reserved	0111
8	SSU-B (Traceable to SSU type B, see G.812)	1000
9	Reserved	1001
10	Reserved	1010
11	Synchronous Equipment Timing Source (SETS)	1011
12	Reserved	1100
13	Reserved	1101
14	Reserved	1110
15	Do not use for synchronization	1111

In E1 operation, SSMs are transmitted using one and only one of the Sa bits (4, 5, 6, 7, or 8). Table 4 shows the SSMs for E1 operation. The most significant bit, S_{an1} (where n is either 4, 5, 6, 7, or 8), is transmitted first and must be aligned with frame 1 of the E1 multiframe to avoid ambiguous codes from being transmitted or received. Therefore, an SSM is transmitted twice during a full multiframe. An SSM is declared valid when the messages in three consecutive submultiframes are alike.

The DS2155, when operated in E1 mode, provides for access to the Sa bits through four different methods. The first method, which is the simplest for this application and the only one presented here, involves using internal registers based on the CRC4 multiframe. The second method uses the RNAF and TNAF registers and requires more intervention from the host controller. The third method is through a hardware scheme using the RLINK/RLCLK and TLINK/TLCLK pins. Additionally, the internal HDLC controllers can be used.

Method 1 (Recommended) *Internal Register Scheme Based on CRC4 Multiframe:*
On the receive side, there is a set of eight registers (RSiAF, RSiNAF, RRA, RSa4 to RSa8) that report the Si and Sa bits as they are received. These registers are updated with the setting of the receive CRC4 multiframe bit, RCMF, in status register 4. Registers RSa4 to RSa8 hold the Sa bits as received. The host can use the RCMF bit and/or the interrupt to know when to read these registers. The user has 2ms to retrieve the data before it is lost. The MSB of each register is the first received. Please see the following register descriptions for more details.

On the transmit side, there is also a set of eight registers (TSiAF, TSiNAF, TRA, TSa4–TSa8) that can be programmed to insert both Si and Sa data by setting the appropriate bits in the transmit Sa bit control register (TSaCR). Data is sampled from these registers with the setting of the Transmit Multiframe bit, TMF, in status register 4. The host can use the TMF bit to know when to update these registers. The host has 2ms to update the data or else the old data is retransmitted. The MSB of each register is the first bit to be transmitted. See the register descriptions that follow for more details.

Method 2 *Internal Register Scheme based on Double-Frame 7*: On the receive side, the RNAF registers always report the data as it is received in the Sa bit locations. The RNAF registers are updated on align frame boundaries. The setting of the receive-align frame bit in status register 4 (SR4.0) indicates that the contents of the RNAF registers have been updated. The host can use the SR4.0 bit to know when to read the RNAF register. The host has 250μs to retrieve the data before it is lost. On the transmit side, data is sampled from the TNAF registers with the setting of the transmit align frame bit in status register 4 (SR4.3). The host can use the SR4.3 bit to know when to update the TNAF register. It has 250μs to update the data or else the old data is retransmitted. Data in the Sa bit position is overwritten if any of the E1TCR2.3 to E1TCR2.7 bits is set to one.

Method 3 *Hardware Scheme:* On the receive side, all of the received data is reported at the RLINK pin. Using the E1RCR2 register, the user can control the RLCLK pin to pulse during any combination of Sa bits. This allows the user to create a clock that can be used to capture the needed Sa bits. On the transmit side, the individual Sa bits can be either sourced from the TNAF register or externally from the TLINK pin. Using the E1TCR2 register, the framer can be programmed to source any combination of the Sa bits from the TLINK pin.

Method 4 *HDLC Controllers:* The HDLC controllers of the DS2155 are also available to transmit and receive messages using the Sa bits. For information on using the HDLC controllers to pass SSMs, please contact the factory at https://support.maximintegrated.com/.

Note: The registers shown below are used for transmitting and receiving SSMs (E1) via the recommended method (method 1) outlined above. These register descriptions can also be found in the DS2155 data sheet.

Register Name: SR4, Status Register 4, Address 1Ch

Bit #	7	6	5	4	3	2	1	0
Name	—	RSA1	RSA0	TMF	TAF	RMF	RCMF	RAF

Bit 0: Receive Align Frame Event. Set every 250µs at the beginning of align frames. Used to alert the host that Si and Sa bits are available in the RAF and RNAF registers.

Bit 1: Receive CRC4 Multiframe Event (RCMF). Set on CRC4 multiframe boundaries. This bit continues to be set every 2ms on an arbitrary boundary if CRC4 is disabled.

Bit 2: Receive Multiframe Event (RMF). In E1, sets every 2ms (regardless if CAS signaling is enabled or not) on receive multiframe boundaries. Used to alert the host that signaling data is available.

Bit 3: Transmit Align Frame Event (TAF). Set every 250µs at the beginning of align frames. Used to alert the host that the TAF and TNAF registers need to be updated.

Bit 4: Transmit Multiframe Event (TMF). In E1, set every 2ms (regardless if CRC is enabled) on the transmit multiframe boundaries. Used to alert the host that signaling data needs to be updated.

Bit 5: Receive Signaling All Zeros Event (RSA0). Set when over a full MF, timeslot 16 contains all zeros.

Bit 6: Receive Signaling All Ones Event (RSA1). Set when the contents of timeslot 16 contain less than 3 zeros over 16 consecutive frames. This alarm is not disabled in the CCS signaling mode.

Bit 7: Unused. Set to 0 for proper operation.

Register Name: IMR4, Interrupt Mask Register 4, Address 1Dh

Bit #	7	6	5	4	3	2	1	0
Name	—	RSA1	RSA0	TMF	TAF	RMF	RCMF	RAF

Bit 0: Receive Align Frame Event
0 = interrupt masked
1 = interrupt enabled

Bit 1: Receive CRC4 Multiframe Event (RCMF)
0 = interrupt masked
1 = interrupt enabled

Bit 2: Receive Multiframe Event (RMF)
0 = interrupt masked
1 = interrupt enabled

Bit 3: Transmit Align Frame Event (TAF)
0 = interrupt masked
1 = interrupt enabled

Bit 4: Transmit Multiframe Event (TMF)
0 = interrupt masked
1 = interrupt enabled

Bit 5: Receive Signaling All Zeros Event (RSA0)
0 = interrupt masked
1 = interrupt enabled

Bit 6: Receive Signaling All Ones Event (RSA1)
0 = interrupt masked
1 = interrupt enabled

Bit 7: Unused. Set to 0 for proper operation.

Register Name: RSa*n*, Received Sa*n* Bits, Addresses CBh to CFh (where *n* is either 4, 5, 6, 7, or 8)

Bit #	7	6	5	4	3	2	1	0
Name	RSa*n*F1	RSa*n*F3	RSa*n*F5	RSa*n*F7	RSa*n*F9	RSa*n*F11	RSa*n*F13	RSa*n*F15

Bit 0: Received Sa*n* Bit of Frame 15

Bit 1: Received Sa*n* Bit of Frame 13

Bit 2: Received Sa*n* Bit of Frame 11

Bit 3: Received Sa*n* Bit of Frame 9

Bit 4: Received Sa*n* Bit of Frame 7

Bit 5: Received Sa*n* Bit of Frame 5

Bit 6: Received Sa*n* Bit of Frame 3

Bit 7: Received Sa*n* Bit of Frame 1

Register Name: TSa*n*, Transmit Sa*n* Bits, Addresses D5h to D9h (where *n* is either 4, 5, 6, 7, or 8)

Bit #	7	6	5	4	3	2	1	0
Name	Tsa*n*F1	TSa*n*F3	TSa*n*F5	TSa*n*F7	TSa*n*F9	TSa*n*F11	TSa*n*F13	TSa*n*F15

Bit 0: Sa*n* Bit to transmit in Frame 15

Bit 1: Sa*n* Bit to transmit in Frame 13

Bit 2: Sa*n* Bit to transmit in Frame 11

Bit 3: Sa*n* Bit to transmit in Frame 9

Bit 4: Sa*n* Bit to transmit in Frame 7

Bit 5: Sa*n* Bit to transmit in Frame 5

Bit 6: Sa*n* Bit to transmit in Frame 3

Bit 7: Sa*n* Bit to transmit in Frame 1

Register Name: TSACR, Transmit Sa Bit Control Register, Address DAh

Bit #	7	6	5	4	3	2	1	0
Name	SiAF	SiNAF	RA	Sa4	Sa5	Sa6	Sa7	Sa8

Bit 0: Additional Bit 8 Insertion Control Bit (Sa8):
0 = do not insert data from the TSa8 register into the transmit data stream
1 = insert data from the TSa8 register into the transmit data stream

Bit 1: Additional Bit 7 Insertion Control Bit (Sa7):
0 = do not insert data from the TSa7 register into the transmit data stream
1 = insert data from the TSa7 register into the transmit data stream

Bit 2: Additional Bit 6 Insertion Control Bit (Sa6):
0 = do not insert data from the TSa6 register into the transmit data stream
1 = insert data from the TSa6 register into the transmit data stream

Bit 3: Additional Bit 5 Insertion Control Bit (Sa5):
0 = do not insert data from the TSa5 register into the transmit data stream
1 = insert data from the TSa5 register into the transmit data stream

Bit 4: Additional Bit 4 Insertion Control Bit (Sa4):
0 = do not insert data from the TSa4 register into the transmit data stream
1 = insert data from the TSa4 register into the transmit data stream

Bit 5: Remote Alarm Insertion Control (RA):
0 = do not insert data from the TRA register into the transmit data stream
1 = insert data from the TRA register into the transmit data stream

Bit 6: International Bit in Nonalign Frame Insertion Control Bit (SiNAF):
0 = do not insert data from the TSiNAF register into the transmit data stream
1 = insert data from the TSiNAF register into the transmit data stream

Bit 7: International Bit in Align Frame Insertion Control (SiAF):
0 = do not insert data from the TSiAF register into the transmit data stream
1 = insert data from the TSiAF register into the transmit data stream

CONFIGURATION AND CONNECTIONS

Depending on the design of the BITS clock (i.e., framing format, will the payload carry live traffic, etc.), the DS2155 can be configured in many different ways. A typical configuration for T1 operation might look like the following: (Registers not listed are set to 00h.)

- Transmit and receive ESF framing mode.
  - ✓ T1 Receive Control Register 2 (T1RCR2, address 04h) = 60h
  - ✓ T1 Transmit Control Register 2 (T1CR2, address 06h) = 20h
  - ✓ T1 Common Control Register 1 (T1CCR, address 07h) = 04h
- Jitter attenuator disabled, LIU configured to proper termination.
  - ✓ Line Interface Control Register 1, (LIC1, address 78h) = 03h
  - ✓ Line Interface Control Register 2, (LIC2, address 79h) = 10h
  - ✓ Line Interface Control Register 3, (LIC3, address 7A) = 00h, or if G.703 synchronization signal is desired then set this register to 06h
  - ✓ Line Interface Control Register 4, (LIC4, address 7Bh) = varies depending upon the desired internal or external termination mode
- BERT enabled to transmit QRSS in payload.
  - ✓ BERT Control Register (BC1, address E0h) = 0Ch
  - ✓ BERT Interface Control Register (BIC, address EAh) = 01h
  - ✓ Per-Channel Pointer Register (PCPR, address 28h) = 11h
  - ✓ Per-Channel Data Registers 1-4 (PCDR1–PCDR4, address 29h–2Ch) = FFh
- BOC controller used to transmit and receive SSMs. (See SSM section for register usage.)

An E1 configuration might look like the following: (Registers not listed are set to 00h.)

- Set E1 mode, transmit and receive CRC4 multiframe mode.
  - ✓ Master Mode Register (address 00h) = 02h
  - ✓ E1 Receive Control Register 1 (E1RCR1, address 33h) = 48h
  - ✓ E1 Transmit Control Register 1 (E1TCR1, address 35h) = 11h
  - ✓ Transmit Align Frame Register (TAF, address D0h) = 1Bh
  - ✓ Transmit Nonalign Frame Register (TNAF, address D1h) = 40h
- Jitter attenuator disabled, LIU configured for E1 operation and proper termination.
  - ✓ Line Interface Control Register 1, (LIC1, address 78h) = 03h
  - ✓ Line Interface Control Register 2, (LIC2, address 79h) = 90h
  - ✓ Line Interface Control Register 3, (LIC3, address 7A) = 00h, or if G.703 synchronization signal is desired then set this register to 06h
  - ✓ Line Interface Control Register 4, (LIC4, address 7Bh) = varies depending upon the desired termination
- BERT enabled to transmit QRSS in payload.
  - ✓ BERT Control Register (BC1, address E0h) = 0Ch
  - ✓ BERT Interface Control Register (BIC, address EAh) = 01h
  - ✓ Per-Channel Pointer Register (PCPR, address 28h) = 11h
  - ✓ Per-Channel Data Registers 1–4 (PCDR1–PCDR4, address 29h–2Ch) = FFh
- Sa bit configured to carry SSMs using method 1 as outlined above in the SSM section.

Please contact the communication products application group at https://support.maximintegrated.com/ for questions regarding any configuration questions. In addition to timing specifications, over-voltage and over-current conditions in accordance to the appropriate specifications must be met. For information about the protected network interface circuitry, refer to *Application Note 324*, which provides information and recommendations for the design of the network interface.

SUMMARY

The BITS and SSU methods for network synchronization are used extensively throughout interoffice and intraoffice systems. For systems that need to meet higher clock level requirements, the incoming DS1/E1 clock steers an oscillator located in a timing block. The timing block should be designed to meet the holdover, free run, and accuracy requirements of the system in which the BITS clock will be used. Dallas Semiconductor offers a wide variety of transceivers, framers, and LIUs that can be used in numerous clock distribution applications. The method in which these devices handle BOC messages and Sa bit information make inserting and extracting SSMs simple. Additionally, the DS2155 offers additional features such as G.703 synchronization signal, software-selectable termination that simplify the development of a BITS/SSU board.