SEPTEMBER 2022

8Mb LOW VOLTAGE,

ULTRA LOW POWER PSEUDO CMOS STATIC RAM

Features

- High-Speed access time :
  - 70ns (IS66WV51216EALL)
  - 60ns (IS66/67WV51216EBLL)
- CMOS Lower Power Operation
- Single Power Supply
  - VDD =1.7V~1.95V(IS66WV51216EALL)
  - VDD =2.5V~3.6V (IS66/67WV51216EBLL)
- Three State Outputs
- Data Control for Upper and Lower bytes
- Lead-free Available

DESCRIPTION

The *ISSI* IS66WV51216EALL and IS66/67WV51216EBLL are high-speed,8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high performance CMOS technology.

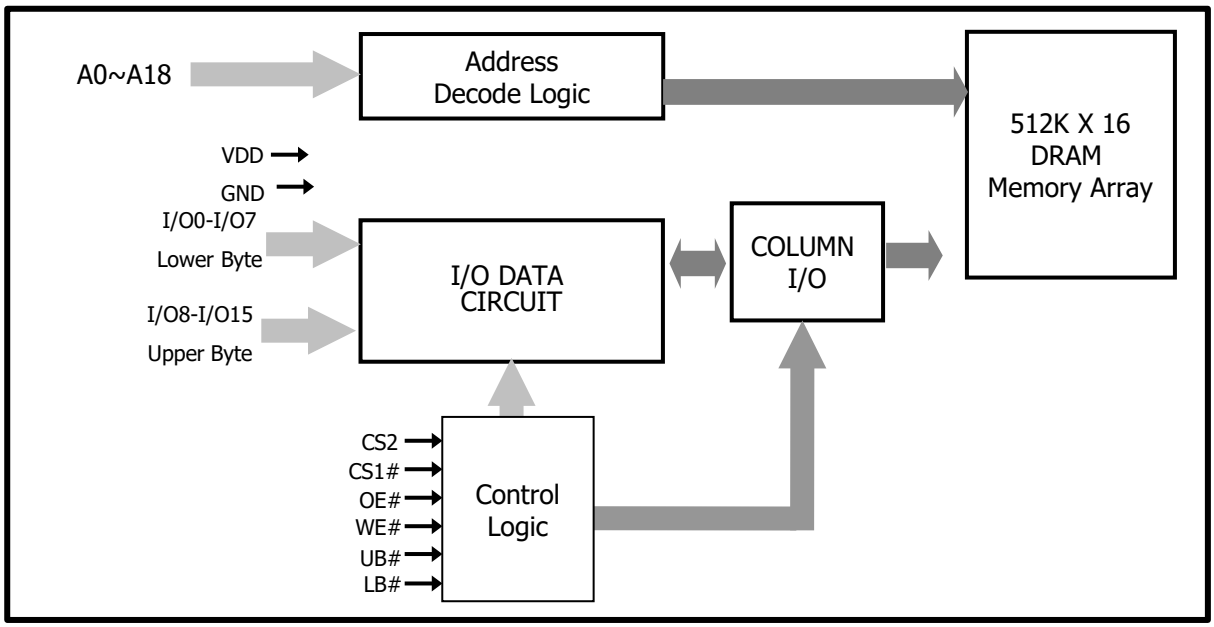
This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When CS1# is HIGH (deselected) or when CS2 is LOW (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable (WE#) controls both writing and reading of the memory. A data byte allows Upper Byte (UB#) and Lower Byte (LB#) access.

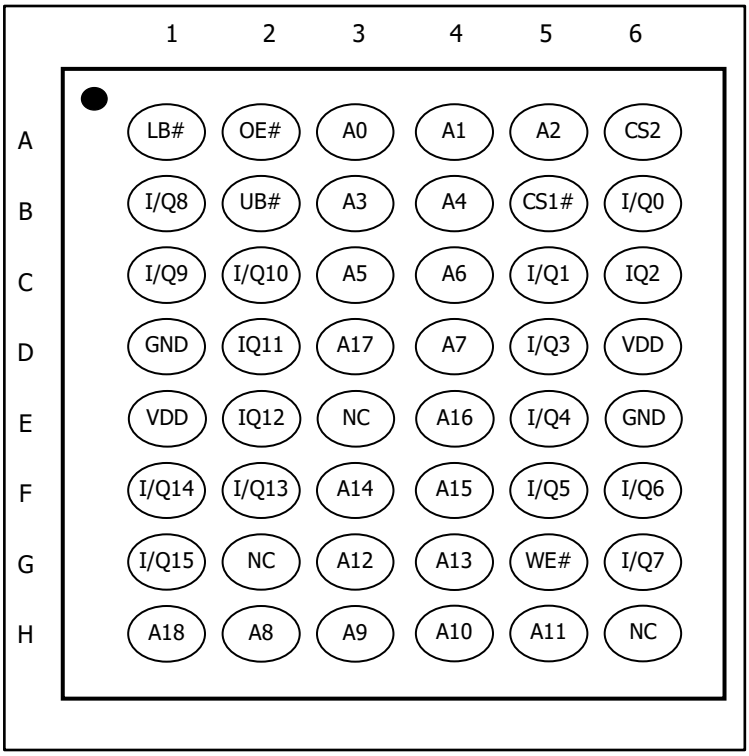
The IS66WV51216 EALL and IS66/67WV51216EBLL are packaged in the JEDEC standard 48-ball mini BGA (6mm x 8mm) and 44-Pin TSOP(TYPE-II). The device is also available for die sales.

FUNCTIONAL BLOCK DIAGRAM

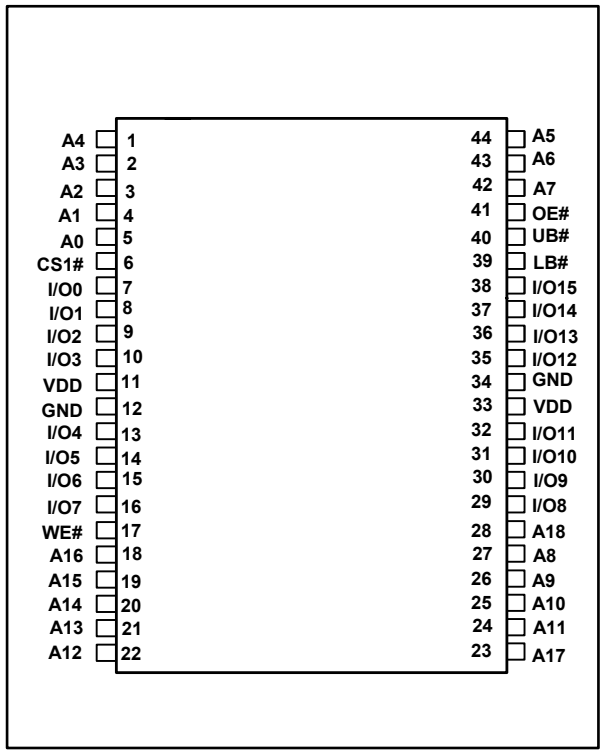


PIN CONFIGURATIONS

48-Ball miniBGA (6mm x 8mm) Ball Assignment



44-pin TSOP (Type II)

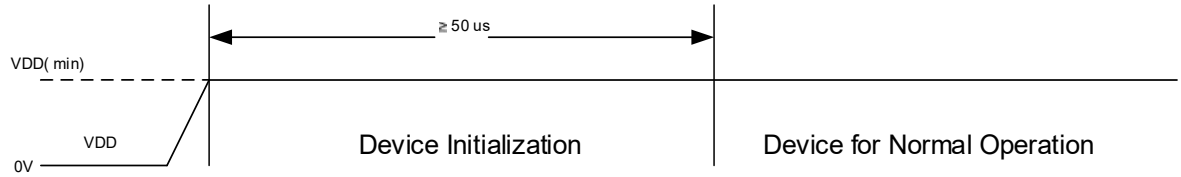


PIN DESCRIPTIONS

Symbol	Type	Description
A0~A18	Input	Address Inputs
I/Q0~I/Q15	Input / Output	Data Inputs/Outputs
CS1#, CS2	Input	Chip Enable
OE#	Input	Output Enable
WE#	Input	Write Enable
UB#	Input	Upper Byte select
LB#	Input	Lower Byte select
VDD	Power Supply	Power
GND	Power Supply	Ground

POWER UP INITIALIZATION

IS66WV51216EALL and IS66/67WV51216EBLL include an on-chip voltage sensor used to launch the power-up initialization process. When VDD reaches a stable level at or above the VDD (min) the device will require 50µs to complete its self-initialization process. During the initialization period, CS1# should remain HIGH. When initialization is complete, the device is ready for normal operation.



TRUTH TABLE

Mode	WE#	CS1#	CS2	OE#	LB#	UB#	I/O0 – I/O7	I/O8 – I/O15	VDD Current
Not Selected	X X	H X	X L	X X	X X	H X	High-Z High-Z	High-Z High-Z	ISB1,ISB2 ISB1,ISB2
Output Disabled	H H	L L	H H	H H	L X	X L	High-Z High-Z	High-Z High-Z	ICC ICC
Read	H H H	L L L	H H H	L L L	L H L	H L L	DOUT High-Z DOUT	High-Z DOUT DOUT	ICC ICC ICC
Write	L L L	L L L	H H H	X X X	L H L	H L L	Din High-Z Din	High-Z Din Din	ICC ICC ICC

Notes:

CS2 input signal pin is only available for 48-ball mini BGA package part. CS2 input is internally enabled for 44-pin TSOP II package part.

OPERATING RANGE (VDD)

Range	Ambient Temperature	IS66WV51216EALL (70ns)	IS66WV51216EBLL (55ns, 70ns)	IS66WV51216EBLL (55ns, 70ns)
Industrial	–40°C to +85°C	1.7V – 1.95V	2.5V – 3.6V	–
Automotive , A1	–40°C to +85°C	–	–	2.5V – 3.6V
Automotive , A2	–40°C to +105°C	–	–	2.5V – 3.6V

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.2 to V_{DD} + 0.3	V
T_{BIAS}	Temperature Under BIAS	-40 to +85	°C
V_{DD}	VDD Related to GND	-0.2 to +3.8	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	1.0	W

Notes:

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

VDD = 2.5V-3.6V (IS66/67WV51216EBLL)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage(1)		2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage(1)		2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:

1. V_{ILL} (min.) = –2.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max.) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% test

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

VDD = 1.7V-1.95V(IS66WV51216EALL)

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.7-1.95V	1.4	—	V
V_{OL}	Output LOw Voltage	I_{OL} = 0.1 mA	1.7-1.95V	—	0.2	V
V_{IH}	Input HIGH Voltage(1)		1.7-1.95V	1.4	V_{DD} + 0.2	V
V_{IL}	Input LOw Voltage(1)		1.7-1.95V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:

1. V_{ILL} (min.) = –1.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max.) = V_{DD} + 1.0V AC (pulse width < 10ns). Not 100% test

CAPACITANCE

Symbol	Description	Conditions	MIN	MAX	Unit
C_{IN}	Input Capacitance	VIN = 0V	-	8	pF
C_{IO}	Input/Output Capacitance (DQ)	Vout = 0V	-	10	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	1.7V – 1.95V (Unit)	2.5V – 3.6V (Unit)
Input Pulse Level	0.4V to VDD – 0.2V	0.4V to VDD – 0.3V
Input Rise and Fall Time	5ns	5ns
Input and Output Timing and Reference Level	VREF	VREF
Output Load	See Figures 1 and 2	See Figures 1 and 2

Symbol	1.7V – 1.95V	2.5V – 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
VREF	0.9V	1.4V
VTM	1.8V	2.8V

AC TEST LOADS

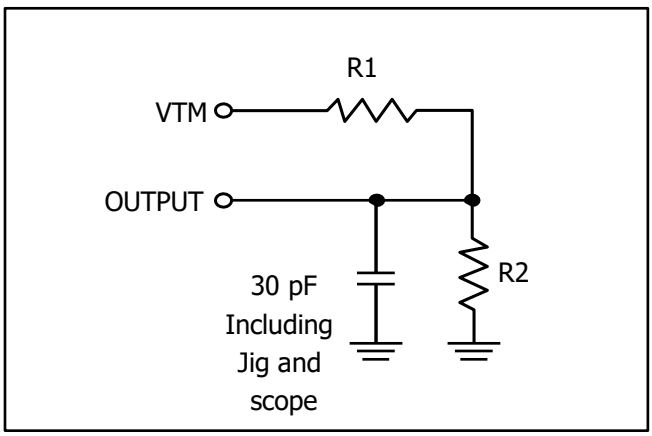


Figure 1

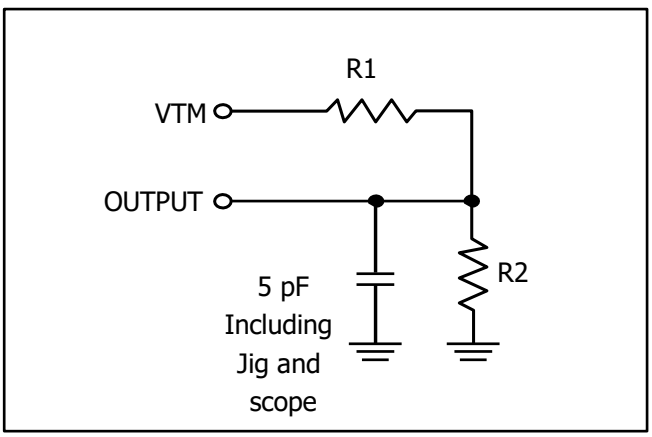


Figure 2

1.7V-1.95V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Conditions	Device	TYP.	MAX. 70ns	Unit
I_{CC}	VDD Dynamic Operating Supply Current	V_{DD}=Max.,I_{OUT}=0mA, f=f_{MAX}, All inputs = 0.4V or VDD – 0.2V	Com. Ind. Auto	- - -	20 25 30	mA
I_{CC1}	Operating Supply Current	V_{DD}=Max.,CS1#=0.2V, WE#= V_{DD} – 0.2V, f=1MHz	Com. Ind. Auto	- - -	8 8 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD}=Max.,V_{IN}=V_{IH} or V_{IL}, CS1# = V_{IH}, CS2=V_{IL} , f=1MHz	Com. Ind. Auto	- - -	0.6 0.6 1	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD}=Max., CS1# ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} > V_{DD} – 0.2V or V_{IN} < 0.2V, f=0	Com. Ind. Auto	- - -	100 120 150	uA

Notes:
1. Atf=f_{MAX}, address and data inputs are cycling at the maximum frequency , f = 0 means no input lines change.

2.5V-3.6V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Conditions	Device	TYP	MAX 55ns	Unit
I_{CC}	VDD Dynamic Operating Supply Current	V_{DD}=Max.,I_{OUT}=0mA, f=f_{MAX}, All inputs = 0.4V or V_{DD} – 0.3V	Com. Ind. Auto A2 Typ.(2)	- - - 	25 28 35 15	mA
I_{CC1}	Operating Supply Current	V_{DD}=Max.,CS1#=0.2V, WE#= V_{DD} – 0.2V, f=1MHz	Com. Ind. Auto A2	- - -	8 8 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD}=Max.,V_{IN}=V_{IH} or V_{IL}, CS1# = V_{IH}, CS2=V_{IL} , f=1MHz	Com. Ind. Auto A2	- - -	0.6 0.6 1	mA
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD}=Max., CS1# ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} > V_{DD} – 0.2V or V_{IN} < 0.2V ,f=0	Com. Ind. Auto A2 Typ.(2)	- - - 	100 130 150 75	uA

Notes:
1. At f=fMAX, address and data inputs are cycling at the maximum frequency , f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, Ta = 25 ºC , and not 100% tested.

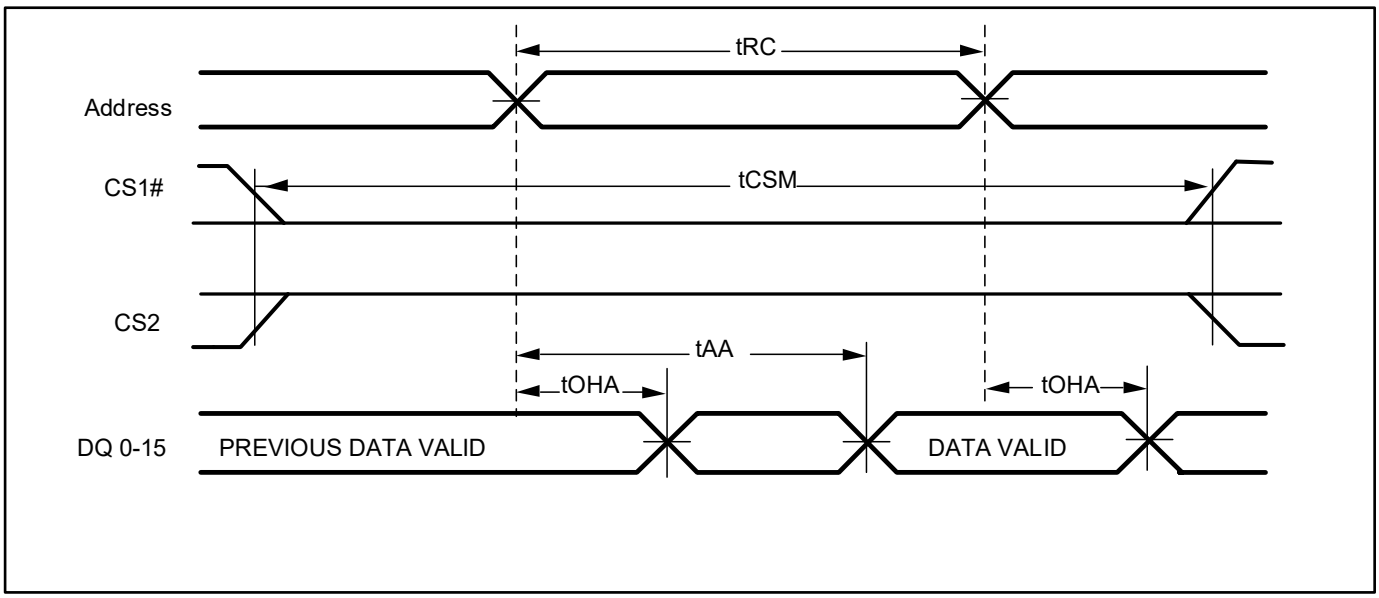
READ CYCLE SWITCHING CHARACTERISTICS(1)(Over Operating Range)

Symbol	Parameter	-55		-70		Unit	Notes
		Min	Max	Min	Max		
t_{RC}	Read cycle time	60	-	70	-	ns	
t_{AA}	Address Acess Time	-	60	-	70	ns	1
t_{OHA}	Output Hold Time	10	-	10	-	ns	
$t_{ACS1/ACS2}$	CS1#/CS2 Acess Time	-	60	-	70	ns	
t_{DOE}	OE# Access Time	-	25	-	35	ns	1
t_{HZOE}	OE# to High-Z output	-	20	-	25	ns	2
t_{LZOE}	OE# to Low-Z output	5	-	5	-	ns	2
t_{CSM}	Maximum CS1#/CS2 pulse width	-	15	-	15	us	
$t_{HZCS1/HZCS2}$	CS1#/CS2 to High-Z output	0	20	0	25	ns	2
$t_{LZCS1/HZCS2}$	CS1#/CS2 to Low-Z output	10	-	10	-	ns	2
t_{BA}	UB#/LB# Acess Time	-	60	-	70	ns	1
t_{HZB}	UB#/LB# to High-Z output	0	20	0	25	ns	2
t_{LZB}	UB#/LB# to Low-Z output	0	-	0	-	ns	2
t_{CPH}	CS1# HIGH (CS2 LOW) time	5	-	5	-	ns	

Notes:
1. Test conditions and output loading are specified in the AC Test Conditions and AC Test Loads (Figure 1) on page 5.
2. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.

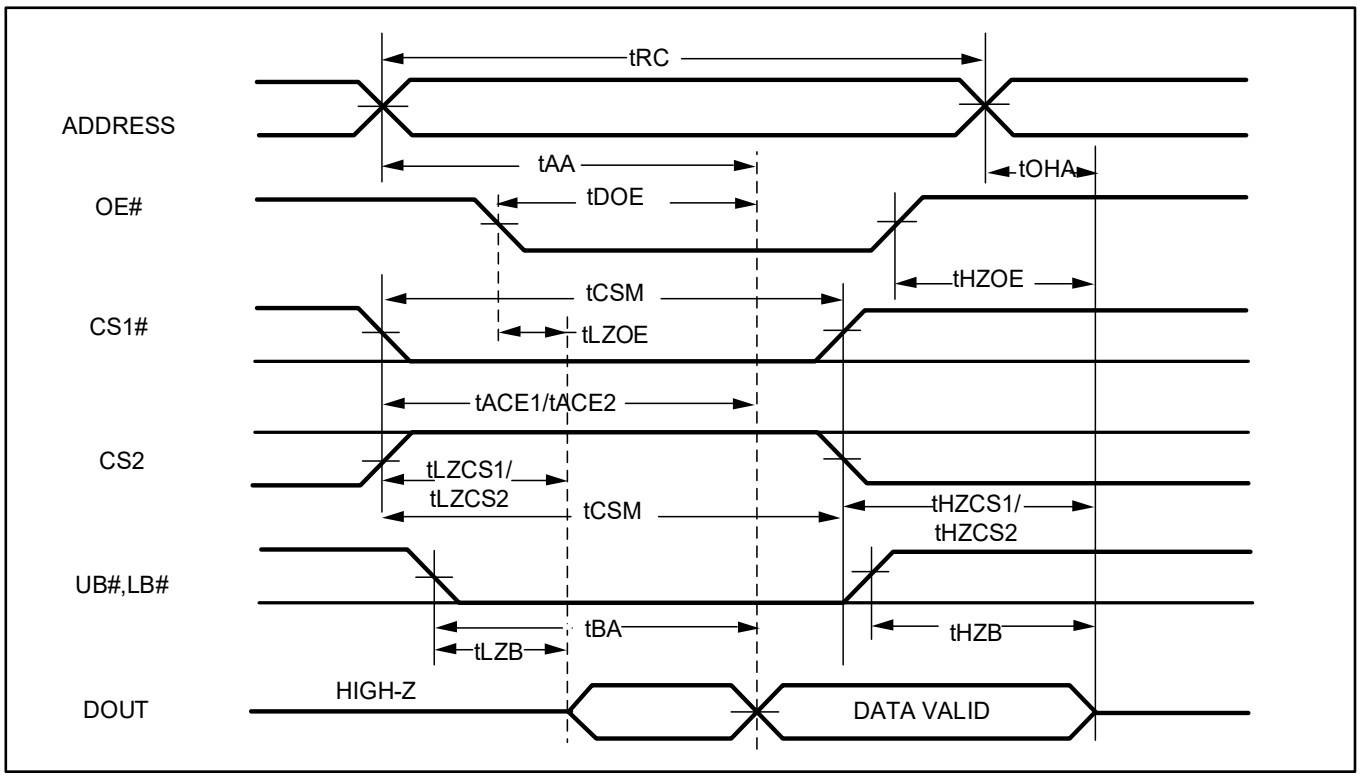
AC WAVEFORMS

READ CYCLE NO. 1(1) (Address Controlled, OE#= V_{IL}, WE#=V_{IH}, UB# or LB# = V_{IL})



Notes:
1. WE# is HIGH for a Read Cycle.

READ CYCLE NO. 2[1] (CS1#, CS2, OE# and UB#/LB# Controlled)



Notes:
1. Address is valid prior to or coincident with CS1# LOW (CS2 HIGH) transition, and is valid after or coincident with CS1# HIGH (CS2 LOW) transition.

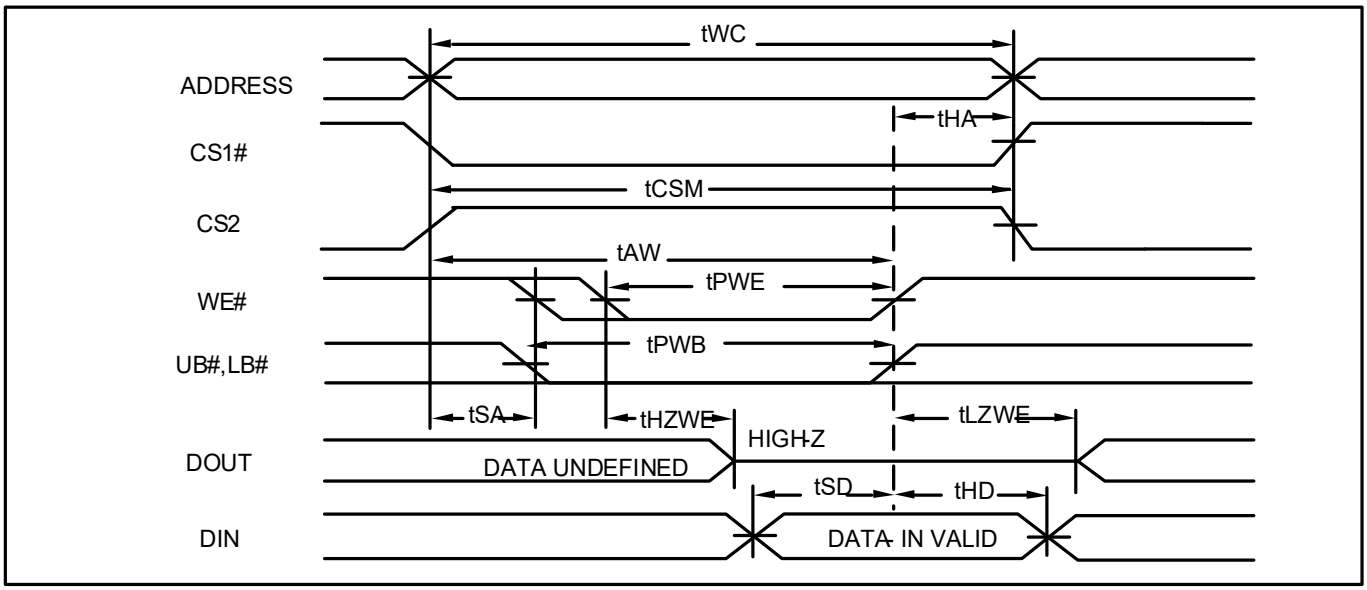
WRITE CYCLE SWITCHING CHARACTERISTICS(1) (Over Operating Range)

Symbol	Parameter	-55		-70		Unit	Notes
		Min	Max	Min	Max		
t_{WC}	Write Cycle Time	55	-	70	-	ns	
$t_{SCS1/SCS2}$	CS1#/CS2 to Write End	45	-	60	-	ns	
t_{CSM}	Maximum CS1#/CS2 pulse width	-	15	-	15	us	
t_{AW}	Address Setup to Write Time	45	-	60	-	ns	
t_{HA}	Address Hold to End of Write	0	-	0	-	ns	
t_{SA}	Address Setup Time	0	-	0	-	ns	
t_{PWB}	UB#/LB# Valid to End of Write	45	-	60	-	ns	
t_{PWE}	WE# Pulse Width	45	-	60	-	ns	
t_{SD}	Data Setup Time	25	-	30	-	ns	
t_{HZWE}	WE# LOW to High-Z output	-	20	-	30	ns	3
t_{LZWE}	WE# HIGH to Low-Z output	5	-	5	-	ns	3
t_{CPH}	CS1# HIGH (CS2 LOW) time	5	-	5	-	ns	

Notes:
1. Test conditions and output loading are specified in the AC Test Conditions and AC Test Loads (Figure 1) on page 5.
2. The internal write time is defined by the overlap of CS1#, UB#, LB# and WE# LOW, CS2 HIGH . All signals must be in valid states to initiate a Write, but anyone can go inactive to terminate Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signals that terminates the Write.
3. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HzWE} + t_{SD}$ when OE# is LOW.
5. Chip Select Active Time (both CS1# LOW and CS2 HIGH) must not be longer than tCMS of 15 us.

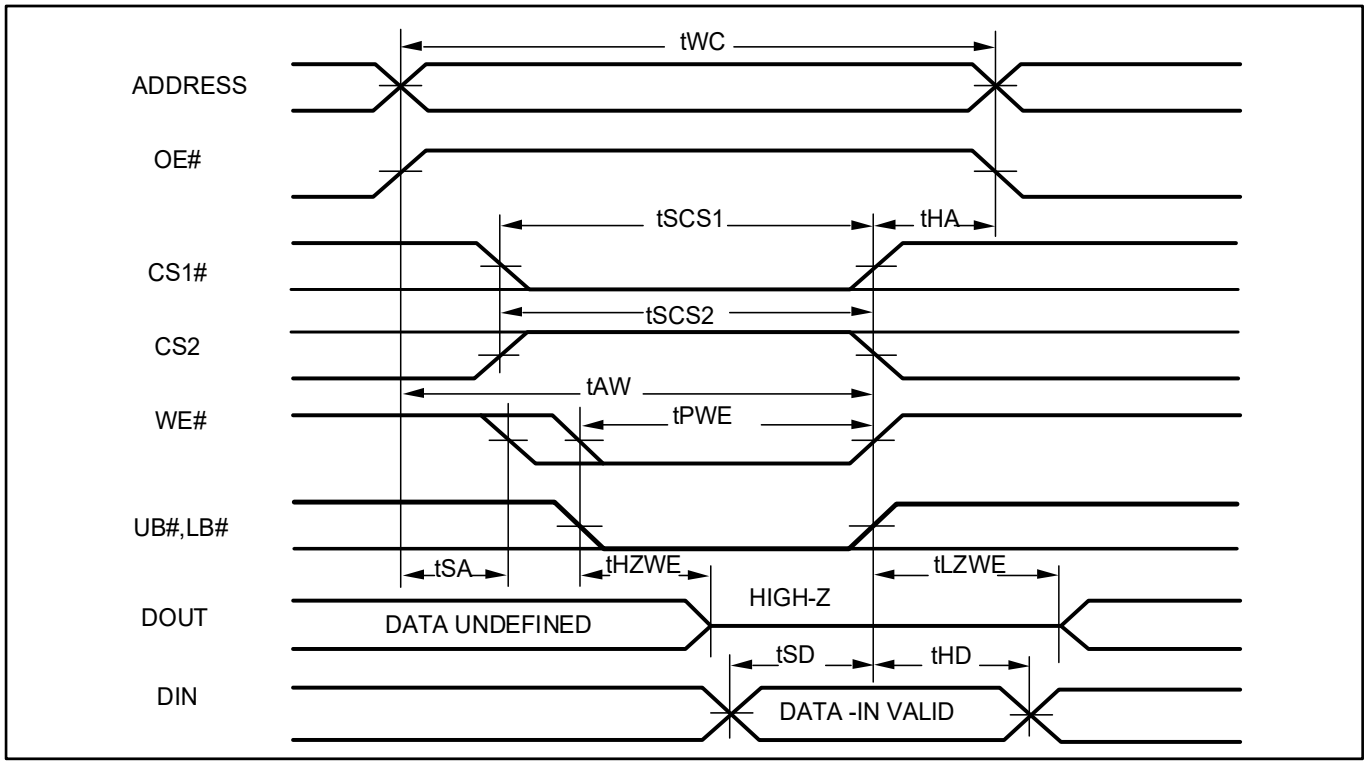
AC WAVEFORMS

WRITE CYCLE NO. 1[1] (CS1# Controlled, OE#= HIGH or LOW)

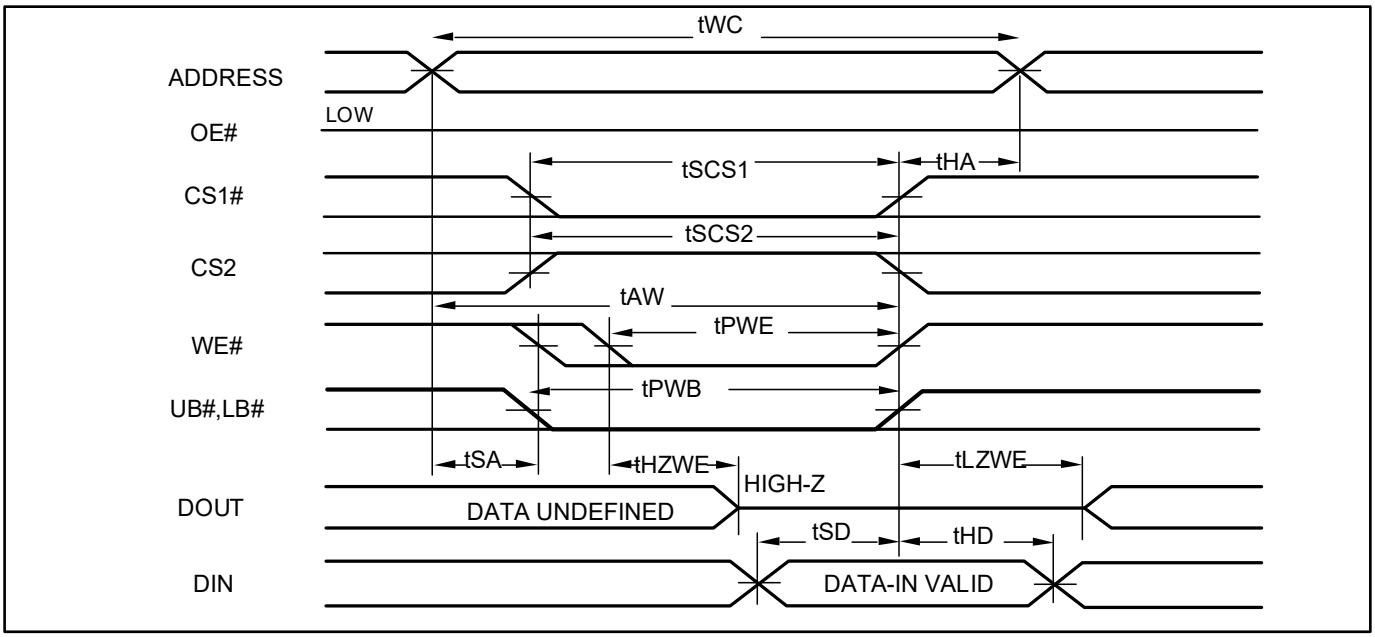


Notes:
1. Write address is valid prior to or coincident with CS1# LOW (CS2 HIGH) transition, and is valid after or coincident with C S1# HIGH (CS2 LOW) transition.

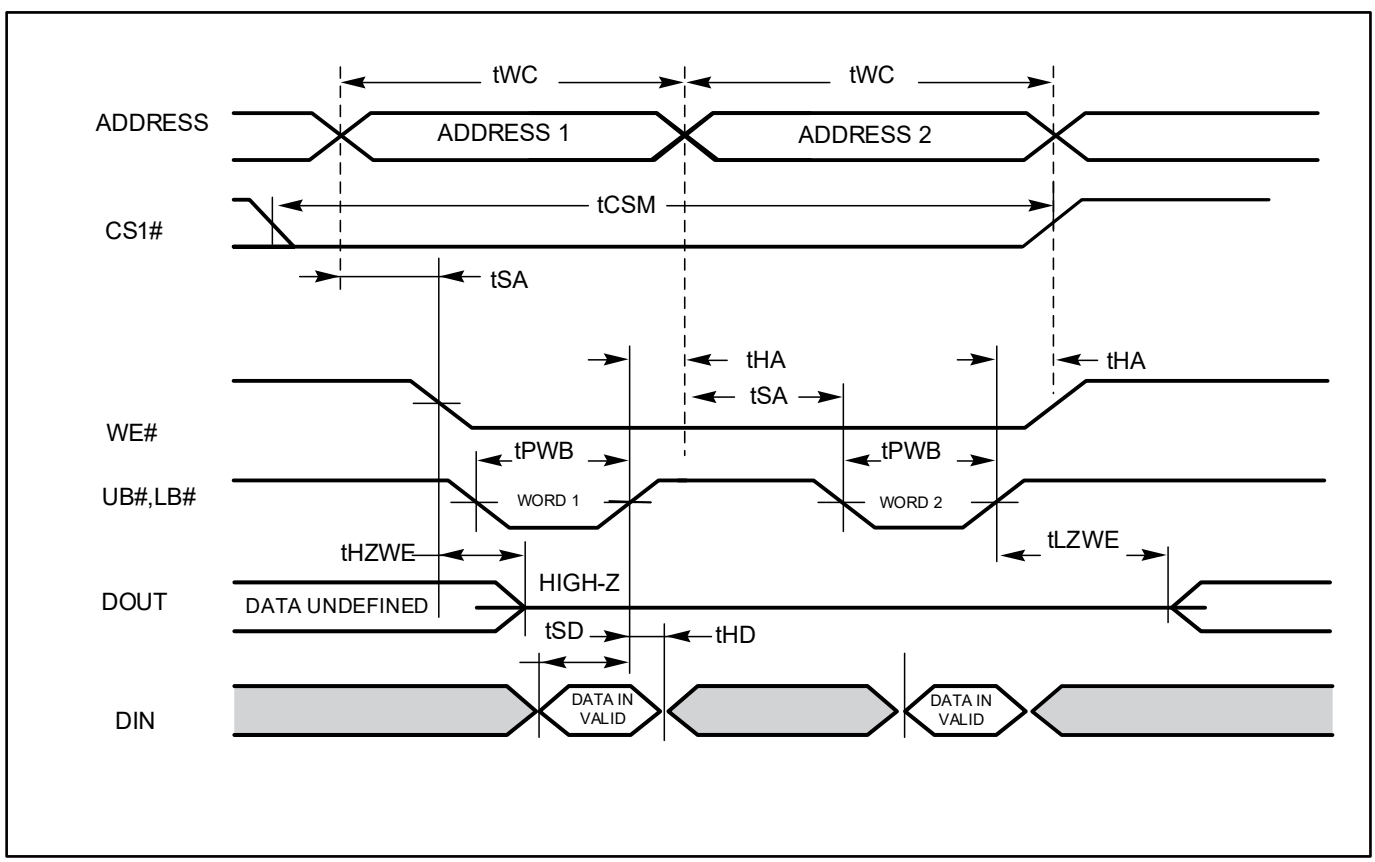
WRITE CYCLE NO. 2 (WE# Controlled, OE#= HIGH during Write Cycle)



WRITE CYCLE NO. 3 (WE# Controlled, OE#= LOW during Write Cycle)



WRITE CYCLE NO. 4 (UB# / LB# Controlled, CS2 is HIGH during Write Cycle)



AVOIDABLE TIMING and RECOMMENDATIONS

Figure 3a : tCSM Violation

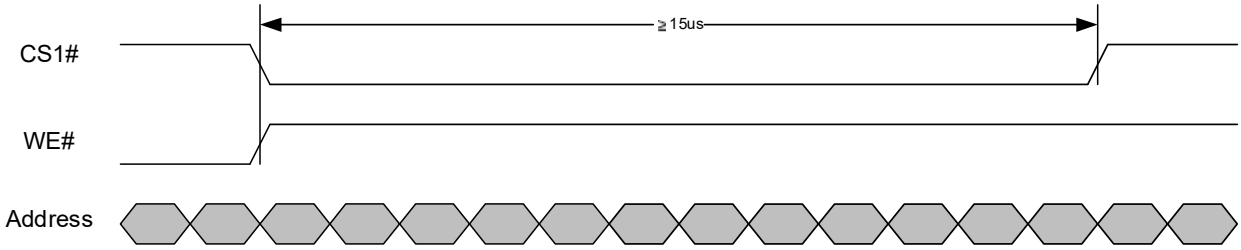
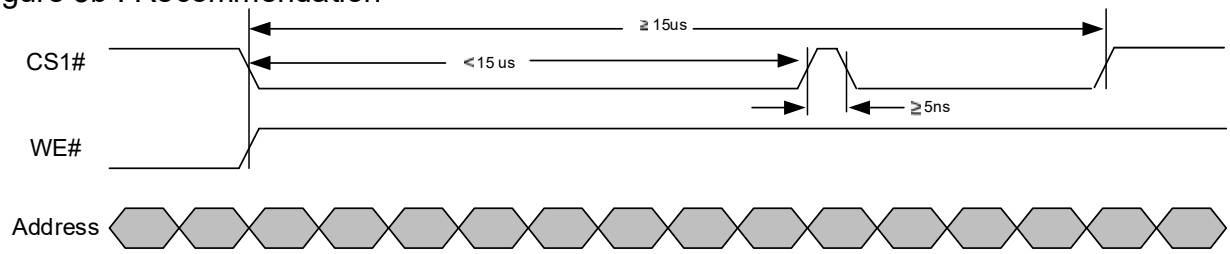


Figure 3b : Recommendation



AVOIDABLE TIMING and RECOMMENDATIONS

Figure 4a : tCSM Violation

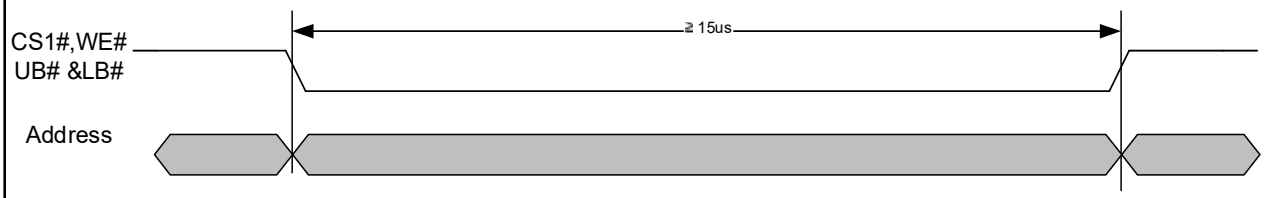
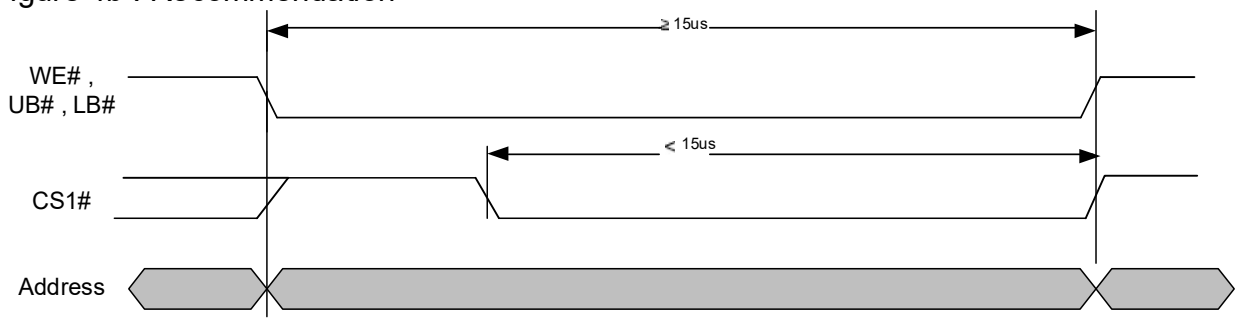


Figure 4b : Recommendation



Notes:

1. PSRAM uses DRAM cell which needs a REFRESH action periodically to retain the information. This REFRESH action is performed only when the device is not selected (Chip Select Pins are Disabled). A hidden REFRESH action has to be executed by the device at least once every 15 µs of tCSM.

2. Figure 3a shows a timing example in which consecutive READ cycles for more than 15 us . This timing should be avoided for proper REFRESH operation.
   REFRESH operation can begin only during Chip Select pins are Disabled (CS1# is High and CS2 is Low) for more than 5ns.
   Example on how to avoid tCSM violation in Figure 3a is shown in Figure 3b.

3. Figure 4a shows a timing example in which a single WRITE operation is maintained for a period greater than 15 µs. Since a proper REFRESH action cannot be performed during device is selected by Chip Select pins, information stored in the device will not be retained if this timing occurs.

   Figure 4b is a timing example of using CS1# signal toggling for proper the WRITE operation

IS66WV51216EALL

Industrial Temperature Range: (-40°C to +85°C)

Voltage Range : 1.7V to 1.95V

Config.	Speed (ns)	Order Part No.	Package
512K x16	70	IS66WV51216EALL-70TLI IS66WV51216EALL-70BLI	TSOP-II, Lead-free mini BGA(6mm x 8mm), Lead-free

IS66WV51216EBLL

Industrial Temperature Range: (-40°C to +85°C)

Voltage Range : 2.5V to 3.6V

Config.	Speed (ns)	Order Part No.	Package
512K x16	55	IS66WV51216EBLL-55TLI IS66WV51216EBLL-55BLI	TSOP-II, Lead-free mini BGA(6mm x 8mm), Lead-free
	70	IS66WV51216EBLL-70TLI IS66WV51216EBLL-70BLI	TSOP-II, Lead-free mini BGA(6mm x 8mm), Lead-free

IS67WV51216EBLL

Automotive (A1) Temperature Range: (-40°C to +85°C)

Voltage Range : 2.5V to 3.6V

Config.	Speed (ns)	Order Part No.	Package
512K x16	55	IS67WV51216EBLL-55TLA1 IS67WV51216EBLL-55BLA1	TSOP-II, Lead-free mini BGA(6mm x 8mm), Lead-free
	70	IS67WV51216EBLL-70TLA1 IS67WV51216EBLL-70BLA1	TSOP-II, Lead-free mini BGA(6mm x 8mm), Lead-free

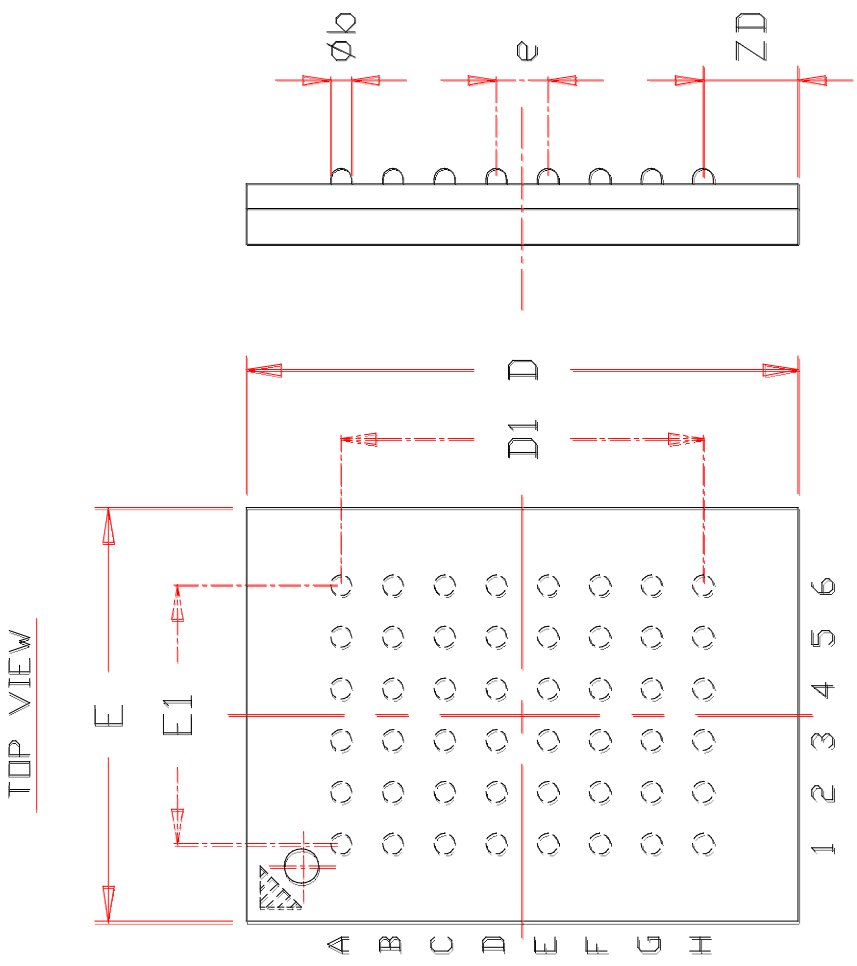
Notes :

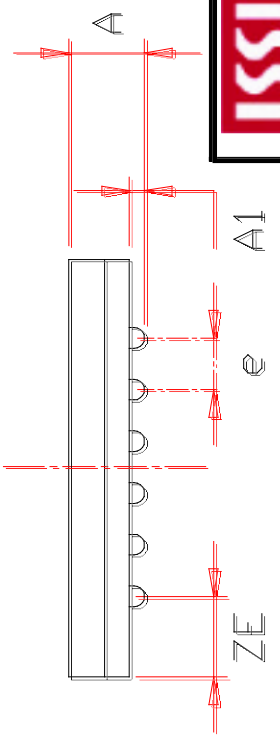
1. Please contact ISSI SRAM marketing at sram@issi.com if you need -40 **°C** to +105 **°C** product.

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.20		0.30	0.008		0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1		5.25 BSC			0.207 BSC	
E	5.90	6.00	6.10	0.232	0.236	0.240
E1		3.75 BSC			0.148 BSC	
e		0.75 BSC,			0.030 BSC,	
ZD		1.375 REF,			0.054 REF,	
ZE		1.125 REF,			0.044 REF,	

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207





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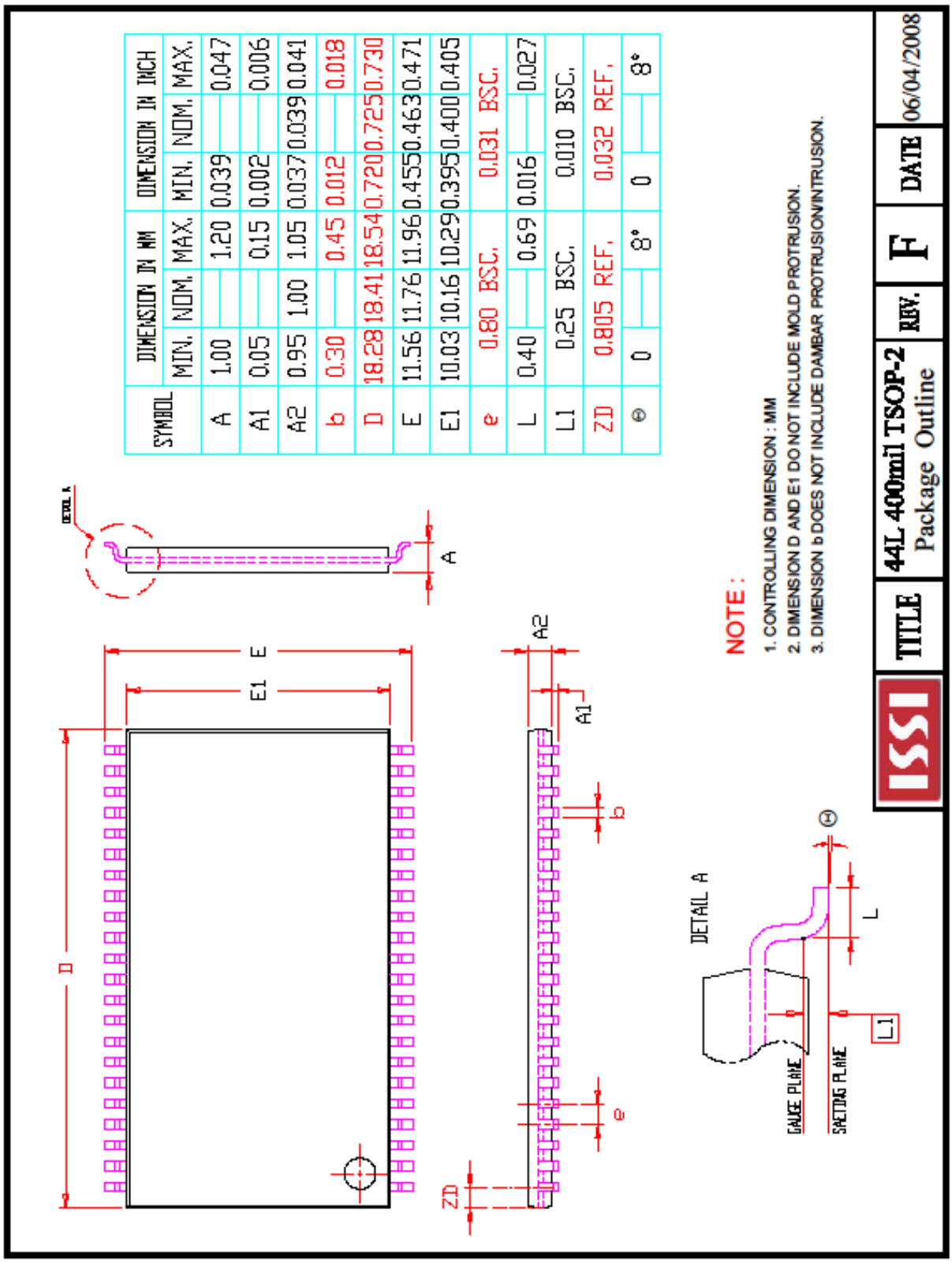
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DIMENSION IN MM
MIN. NOM. MAX.
DIMENSION IN INCH
MIN. NOM. MAX.
A 1.00 — 1.20 0.039 — 0.047
A1 0.05 — 0.15 0.002 — 0.006
A2 0.95 1.00 1.05 0.037 0.039 0.041
b 0.30 — 0.45 0.012 — 0.018
D 18.28 18.41 18.54 0.720 0.725 0.730
E 11.56 11.76 11.96 0.455 0.463 0.471
E1 10.03 10.16 10.29 0.395 0.400 0.405
e 0.80 BSC. 0.031 BSC.
L 0.40 — 0.69 0.016 — 0.027
L1 0.25 BSC. 0.010 BSC.
ZD 0.805 REF. 0.032 REF.
θ 0 — 8° 0 — 8°
NOTE :
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.
TITLE
44L 400mil TSOP-2
Package Outline
REV.
F
DATE
06/04/2008
DETAIL A
GAUGE PLANE
SEATING PLANE
L1
L
θ
A
A2
A1
b
e
ZD
D
E
E1