IQS269A DATASHEET

8 Channel capacitive touch and proximity controller
with additional Hall-effect and inductive sensing abilities.

1 Device Overview

The **IQS269A** ProxFusion® IC is an 8-channel self/mutual-capacitive proximity and touch controller with best in class sensitivity, signal to noise ratio and power consumption. In addition, the device offers mixed sensing abilities such as Hall- and inductive sensing. Other features include automatic tuning and differential offset compensation for sense electrodes.

1.1 Main Features

- Highly flexible 8-channel ProxFusion® controller
- Each channel can be configured with connections to up to 8 external connections OR one internal option
- **8 external** sensor pad connections:
  - Self/Mutual-Capacitive sensors
  - Self/Mutual Inductive sensors
  - Dedicated reference sensor mode for environmental / mechanically sensitive designs
- **Internal** sensor option:
  - Hall-sensor
- Serial scanning (Single ProxFusion® engine) – up to 8 time-slots
- Built-in basic functions:
  - Automatic tuning
  - Noise filtering
  - Differential measurements (reference channels)
  - Debounce & hysteresis
  - Dual direction trigger indication
- Built-in user-interface options
  - Slider (up to 8 elements each) with co-ordinate output, flick/swipe/tap detection
  - Up to two sliders may be defined
  - Integrated measurement set for capacitance calculation
- Wide Range of Capacitance Detection, Wide Electrode Range of 0 to 200 pF
- Multiple custom signal level event triggers (e.g. proximity, touch, deep touch)
- Capacitive resolution: down to 0.02fF
- Automatic reference channel UIs for temperature and mechanical effects. Assign a reference channel to any single or group of sensing channels
- Options for reduced RF emissions for integration in RF sensitive environments (wide range of charge transfer frequency options)
- I^2C Interface with RDY interrupt line
- Event mode (including reduced interrupt options: blocking & hysteresis)
- Assign a touch flag state of any channel to a dedicated GPIO (default: active low, open drain)

- Dedicated address selection pin
- Special pre-programmed options:
  - Standalone operation on power-up (low-power single button touch)
  - Active high output (push-pull)
  - Timed long-press output (pulse after 5 second touch)
- Supply voltage: 1.8V (-2%) to 3.6V
- **Package options:** QFN16 (3 x 3 x 0.8mm), WLCSP-16 (1.62 x 1.62 x 0.5mm)

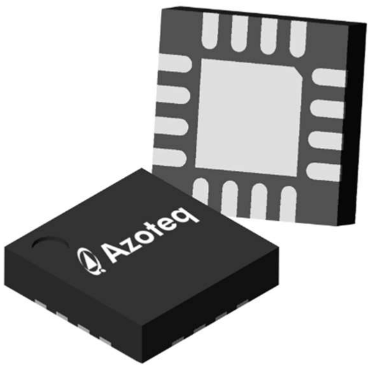
1.2 Applications

- SAR compliance in mobile devices
- Wear detection
- Multi-slider & button designs
- Low power wake-up buttons / proximity
- HALL dock detection

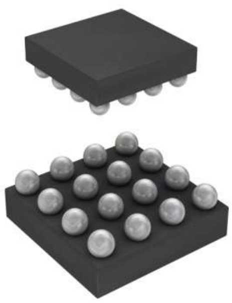
1.3 Description

The IQS269A is a low-power microcontroller that features ProxFusion® technology for high-end proximity and touch applications. The IQS269A provides a highly integrated capacitive-touch solution with flexibility, unique combination sensing and long-term stability. The solution is specifically aimed at providing an accurate output to ensure safety and performance in mobile electronics.

RoHS compliant



QFN(3x3)-16 package
Representation only



WLCSP (1.62x1.62)-16 package
Representation only

1.4 Block Diagram

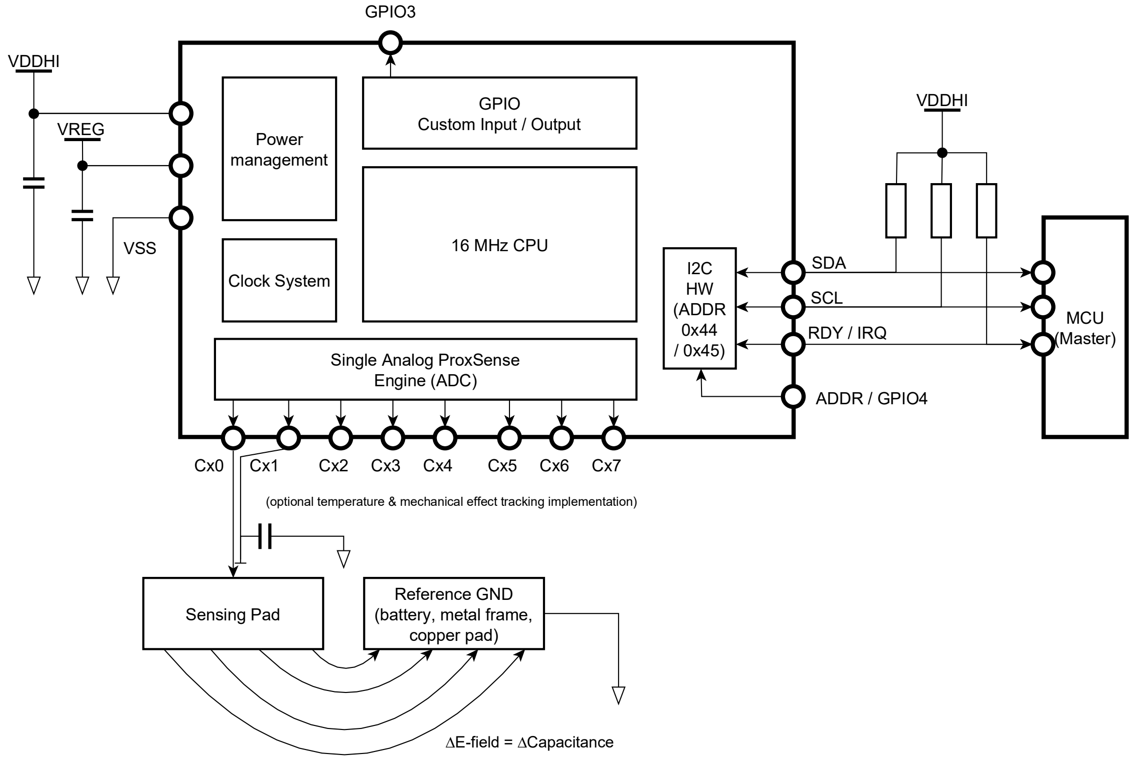


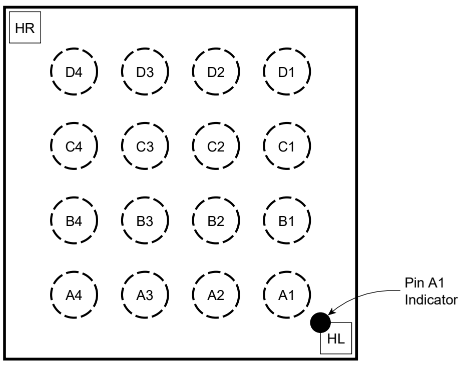
Figure 1.1 Functional Block Diagram

- The IQS269A has one main power pair of VDDHI and VSS that supplies digital and analog modules. Recommended bypass and decoupling capacitors are shown in Table 7.1
- VREG is the decoupling capacitor of the ProxFusion® regulator. The recommended value for the required decoupling capacitor is 4.7 µF, with a maximum ESR of ≤200 mΩ. Recommended VDDHI and VREG capacitor pairing is shown in section 7.3.5
- Add 100nF and 100pF to both VDDHI and VREG as required to ensure immunity against high frequency interference.
- See schematic diagram (section 7.2) for further and precise recommended circuit details.

Contents

2 Terminal Configuration and Function

2.1 WLCSP16 Pin Diagram

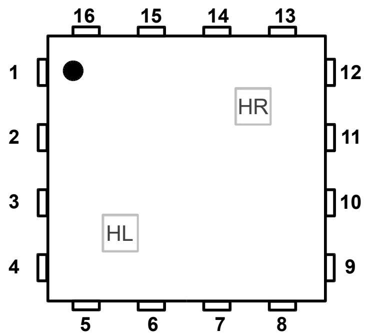


Pin no.	Signal name	Pin no.	Signal name
A1	CRX6	C1	VDDHI
A2	CRX2	C2	GPIO3
A3	CRX0	C3	SDA
A4	CRX5	C4	VSS
B1	CRX4	D1	ADDR / GPIO4
B2	CRX1	D2	SCL
B3	CRX3	D3	RDY
B4	CRX7	D4	VREG

Area name	Signal name	Area name	Signal name
HR (internal)	HALL RIGHT (FW setting: CRX0)	HL (internal)	HALL LEFT (FW setting: CRX1)

Figure 2.1 16-pin WLCSP Package (Top view)

2.2 QFN16 Pin Diagram



Pin no.	Signal name	Pin no.	Signal name
1	GPIO3	9	CRX3
2	ADDR / GPIO4	10	CRX5
3	VDDHI	11	CRX7
4	CRX6	12	VSS
5	CRX4	13	VREG
6	CRX2	14	RDY
7	CRX1	15	SDA
8	CRX0	16	SCL
		17	TAB - floating

Area name	Signal name	Area name	Signal name
HR (internal)	HALL RIGHT (FW setting: CRX0)	HL (internal)	HALL LEFT (FW setting: CRX1)

Figure 2.2 16-pin QFN Package (Top view)

2.3 Pin Attributes

Table 2.1 Pin Attributes

Pin no.		Signal name	Signal type[1]	Buffer type	Power source	Reset state after BOR[2]
WLCSP16	QFN16					
A1	4	CRX6	Analog	LVCMOS	VREG	High-Z
A2	6	CRX2	Analog	LVCMOS	VREG	High-Z
A3	8	CRX0	Analog	LVCMOS	VREG	High-Z
A4	10	CRX5	Analog	Analog	VREG	High-Z
B1	5	CRX4	Analog	LVCMOS	VREG	High-Z
B2	7	CRX1	Analog	LVCMOS	VREG	High-Z
B3	9	CRX3	Analog	LVCMOS	VREG	High-Z
B4	11	CRX7	Analog	Analog	VREG	High-Z
C1	3	VDDHI	P	Power	N/A	High-Z
C2	1	GPIO3	I/O	LVCMOS	VDDHI	High-Z
C3	15	SDA	I/O	LVCMOS	VDDHI	High-Z
C4	12	VSS	P	Power	N/A	High-Z
D1	2	ADDR / GPIO4	I/O	LVCMOS	VDDHI	High-Z
D2	16	SCL	I/O	LVCMOS	VDDHI	High-Z
D3	14	RDY	O	LVCMOS	VDDHI	High-Z
D4	13	VREG	O	Power	VDDHI	High-Z
	17	TAB	Floating	N/A	N/A	N/A

2.4 Signal Descriptions

Table 2.2 Signal Descriptions

Function	Signal name	Pin no.		Pin type	Description
		WLCSP16	QFN16		
ProxFusion®	CRX6	A1	4	I/O	ProxFusion® channel
	CRX2	A2	6	I/O	
	CRX0	A3	8	I/O	
	CRX5	A4	10	I/O	
	CRX4	B1	5	I/O	
	CRX1	B2	7	I/O	
	CRX3	B3	9	I/O	
	CRX7	B4	11	I/O	
GPIO	ADDR / GPIO4	D1	2	I/O	I²C address selection (0x44 default, 0x45 with GPIO4 to VSS) / CH0 touch and hold PULSE
	GPIO3	C2	1	I/O	Custom Touch Out / Sync In
I²C	SCL	D2	16	I/O	I²C clock
	SDA	C3	15	I/O	I²C data
	RDY (IRQ)	D3	14	O	I²C event mode interrupt
Power	VDDHI	C1	3	P	Power supply
	VREG	D4	13	O	ProxFusion® regulator external decoupling capacitor
	VSS	C4	12	P	Power ground

[1] Signal Types: I = Input, O = Output, I/O = Input or Output

[2] High-Z = High-impedance with Schmitt trigger and pullup or pulldown (if available) disabled

3 Specifications

3.1 Absolute Maximum Ratings

	Min	Max	Unit
Voltage applied at VDDHI pin to VSS	-0.3	+3.6	V
Voltage applied to any ProxFusion® pin	-0.3	VREG	V
Voltage applied to any other pin (referenced to VSS)	-0.3	VDDHI + 0.3 (3.6V max)	V
Storage temperature, T_{stg}	-40	125	°C

3.1.1 ESD Ratings

			Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

3.1.2 Recommended Operating Conditions

		min	nom	max	Unit
V_{VDDHI_IN}	Supply voltage applied at VDDHI pin	1.764		3.6	V
V_{VREG_OUT}	Regulator output at VREG	1.62		1.7	V
VSS	Supply voltage applied at VSS pin		0		V
T_A	Operating free-air temperature	-40		85	°C
C_{VDDHI}	Recommended capacitor at VDDHI [3]	1[4]	2.2	10	µF
C_{VREG}	Recommended external buffer capacitor at VREG, ESR≤ 200mΩ	0.8	4.7	10	µF
$C_{ELECTRODE}$	Maximum capacitance of all external electrodes on all ProxFusion® blocks	N/A		200	pF

3.1.3 Current Consumption

Table 3.1 Power Consumption for a Multi-channel Application (TWS)

Device setup: f_{SYS} = 16MHz CH0 [wake-up] = self (500kHz, 512 target); CH1 [wear] = self (500kHz, 512 target); CH2 [reference] = self (500kHz, 512 target); CH7 [unipolar] = Hall (4MHz; 512 target)			
Event mode: No activation	**uA**		Report timing:
Operating voltage:	**3.3V**	**1.8V**	
Normal Power Mode	185	184	16ms
Low Power Mode	21	19	160ms
Ultra-Low Power Mode	8.8	6.5	CH0: 160ms (ULP update rate = 16*160ms = 2,56s)
Halt Mode	2.9	1.3	No sampling / Sleep

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±4000 V may actually have higher performance.

[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

[3] A capacitor tolerance of ±20% or better is required

[4] See section 7.3.5 to select an appropriate value for your application. Select 2.2uF for general use and evaluation

Table 3.2 Power Consumption for a Multi-channel Application (TWS) and Optimized Touch Wake-up

Device setup: f_{SYS} = 16MHz CH0 [wake-up] = self (500kHz, 192 target); CH1 [wear] = self (500kHz, 512 target); CH2 [reference] = self (500kHz, 512 target); CH7 [unipolar] = Hall (4MHz; 320 target)			
Event mode: No activation	**uA**		Report timing:
Operating voltage:	**3.3V**	**1.8V**	
Normal Power Mode	162	161	16ms
Low Power Mode	18	17	160ms
Ultra-Low Power Mode	6.5	4.9	CH0: 160ms (ULP update rate = 16*160ms = 2,56s)
Halt Mode	2.9	1.3	No sampling / Sleep

Table 3.3 Power Consumption for a Multi-channel Application (TWS) with Optimized Touch and Lower System Frequency

Device setup: f_{SYS} = 4MHz CH0 [wake-up] = self (500kHz, 192 target); CH1 [wear] = self (500kHz, 512 target); CH2 [reference] = self (500kHz, 512 target); CH7 [unipolar] = Hall (1MHz; 320 target)			
Event mode: No activation	**uA**		Report timing:
Operating voltage:	**3.3V**	**1.8V**	
Normal Power Mode	174	172	16ms
Low Power Mode	21	19	160ms
Ultra-Low Power Mode	5.5	3.9	CH0: 160ms (ULP update rate = 16*160ms = 2,56s)
Halt Mode	2.9	1.3	No sampling / Sleep

3.1.4 Timing and Switching Characteristics

3.1.5 Reset Levels

		Min	Typ	Max	Unit
$V_{BOR, safe}$	Safe BOR power down level[1]	0.6			V
V_{VDDHI_BOD}	Power-up/down level (Reset trigger) – slope > 100V/s			1.7	V
V_{VREG_BOD}	Power-up/down level (Reset trigger) – slope > 100V/s			1.55	V

3.1.6 Miscellaneous Timings and Parameters

		Min	Typ	Max	Unit
f_{xfer}	Charge transfer frequency (derived from f_{SYS})	-2%		+2%	N/A
I_{sleep}	Sleep mode current			1	uA
t_{WDT16}	Watchdog timer for f_{SYS}=16MHz	30	33	36	ms
t_{WDT4}	Watchdog timer for f_{SYS}=4MHz	118	131	145	ms

[1] A safe BOR can be correctly generated only if VDDHI drops below this voltage before it rises.

3.1.7 Digital I/O Characteristics

		min	nom	max	Unit
V_{IL}	Input low level voltage	VSS – 0.3		0.3 * VDDHI	V
V_{IH}	Input high level voltage	0.7 * VDDHI		VDDHI +0.3	
V_{OL}	Output low level voltage (@10mA)			0.3	V
V_{OH}	Output low level voltage (@5mA)	VDDHI-0.3			V

3.1.8 I²C Characteristics

Specified over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted).

PARAMETER		TEST CONDITIONS	VDDHI	MIN	TYP	MAX	UNIT
f_{SYS}	System clock frequency			15.68	16	16.32	MHz
f_{SCL}	SCL clock frequency		1.8 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	1.8 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	1.8 V, 3 V	4.7			µs
		f_{SCL} > 100 kHz		0.6			
$t_{HD,DAT}$	Data hold time		1.8 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		1.8 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	1.8 V, 3 V	4.0			µs
		f_{SCL} > 100 kHz		0.6			
t_{SP}	Pulse duration of spikes suppressed by input filter	N/A	1.8 V, 3 V	No pulse suppression filter			ns

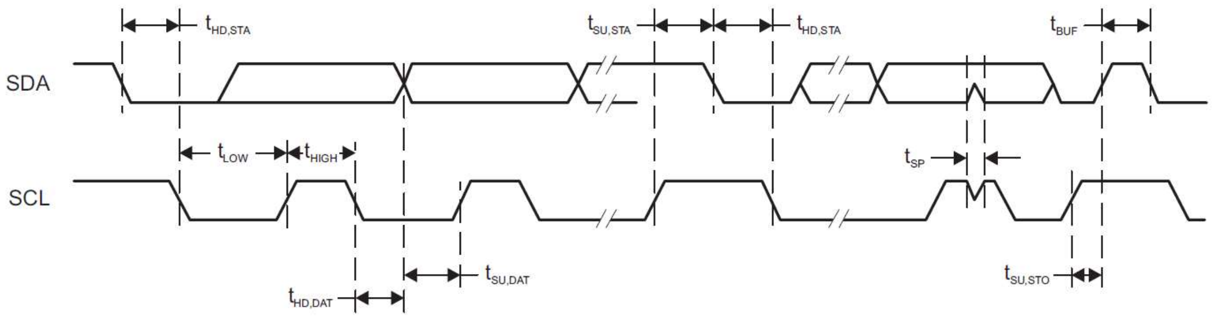


Figure 3.1 I²C Mode Timing

4 Detailed Description

4.1 Overview

The IQS269A solution boasts an integrated charge-transfer ProxFusion® technology coupled a low-power flexible MCU. The IQS269A features up to 8 self/projected-capacitance channels with proximity sensing (down to 0.02-fF resolution). This flexible solution offers custom combinations of sensing channels including dedicated tracking channels for environmental and material effects.

4.2 Peripherals

4.2.1 ProxFusion®

The ProxFusion® module detects the capacitance changed with a charge-transfer method. In lowest power modes, the ProxFusion® module can periodically wake the CPU based on a ProxFusion® timer source. The ProxFusion® module supports the following proximity-sensing capability:

- Up to 8 ProxFusion® individual sensors composed of a single analogue ProxFusion® block. This block consists of 8 I/Os, and sensing is executed sequentially in 8 time-slots.
- Each timeslot (channel) can be configured to do self-capacitance measurements on a single I/O or projected capacitance measurement on a pair of I/Os
- Each channel can be configured to be a self-contained measurement channel or pair with other channels as a reference measurement for mechanical or temperature effects.
- Supports a wake-on-proximity state machine.
- Processing logic to perform normal filter calculation and optimized threshold detection for mobile device SoCs (multiple levels and interrupt frequency limiting).
- Automated processing for custom differential pairs (reference measurement channels) when sensor traces are exposed to temperature sensitive materials or mechanical variation.

4.3 User Interface Options

User interface options refer to "pre-programmed" OTP (one-time-programmable) options for the IQS269A. See ordering information. These options will cause the IC to power-up in a specific state.

4.3.1 Default Option ('00')

In default, the IQS269A will start with:

- No sensing active (All Cx sensor pins will be inactive)
- Sensor processor will be waiting for initialization
- The IRQ (RDY) pin will indicate windows for communication from master
- GPIO3 will be touch output for CH0 (once IC reset is acknowledged – ACK_RESET)
- and GPIO4 will be an input to adjust the I^2C address.

4.3.2 TWS Option ('D0')

In the TWS option, the IQS269A will start with:

- Sensing active on CRX0, assigned to CH0, 160ms sampling rate (All other CRX sensor pins will be inactive)
- Sensor processor will be sensing while waiting for initialization
- The RDY pin will indicate windows for communication from master
- GPIO3 will be touch output for CH0 from the POR event
- and GPIO4 will output a single pulse for indication of a prolonged touch (>5seconds) on CH0
- Known issue and workaround: see in appendix

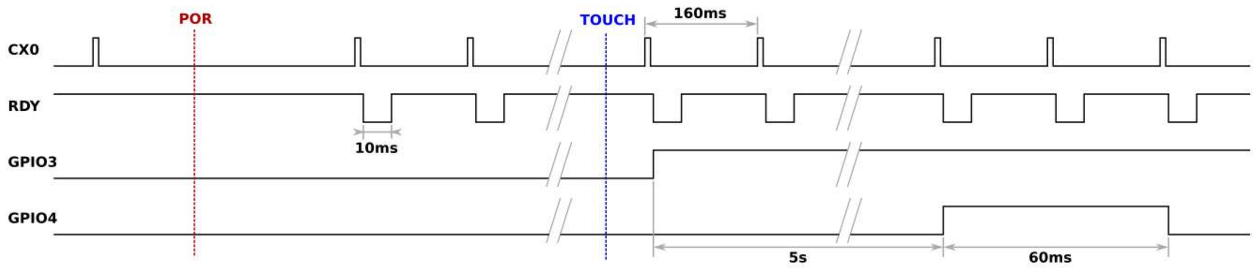


Figure 4.1 Alternative Standalone POR Protocol

GPIO3 will give a direct, active high output of the touch response on the CRX0 pin. GPIO4 will serve as a delayed single output pulse, only sending an active high pulse when the touch condition lasts for 5 seconds.

With this user interface running on CRX0, the IC is still fully usable in the I^2C mode with RDY indications for IC initialization and normal runtime use.

4.3.3 Additional Non-standard Programmable Options

- Ordering code example: IQS269AzzCSR (special order – MOQs apply)
- First "z" (right side): Bank0 bits 7,6,1,0 [IQS269Az**z**CSR]
- Second "z" (left side): Bank5 bits 3,2,1,0 [IQS269A**z**zCSR]
- Bank 1-4 is accessible for custom calibration data

OTP Bank	**Bit 7**	**6**	**5**	**4**	**3**	**2**	**1**	**Bit 0**
Bank 0	f_{SYS}=4MHz not 16MHz	Sleep during RDY low	I^{2}C address (reserved)				I^{2}C address	
Bank 1 (loaded to 0x35 offset 0)	HALL bin (Left – Cx1)				HALL bin (Right – Cx0)			
Bank 2 (loaded to 0x35 offset 1)	Reserved							
Bank 3 (loaded to 0x36 offset 0)	Reserved							
Bank 4 (loaded to 0x36 offset 1)	Reserved							
Bank 5	Reserved				GPIO4 output not ADDR	GPIOs PP not OD	Startup type	
Bank 6	Reserved				Reserved			
Bank 7	Reserved				Reserved			

General options (special order):

Bank0 [1:0]:

- 00: 0x44 (if Bank5 [3] cleared: GPIO4 pull-down = address 0x45)
- 01: 0x45 (if Bank5 [3] cleared: GPIO4 pull-down = address 0x44)
- 10: 0x46 (if Bank5 [3] cleared: GPIO4 pull-down = address 0x47)
- 11: 0x47 (if Bank5 [3] cleared: GPIO4 pull-down = address 0x46)

Start-up type (special order):

Bank5 [1:0]:

- 00: No conversions wait for host to setup
- 01: One touch channel active (most sensitive)
- 10: One touch channel active (less sensitive)
- 11: One touch channel active (least sensitive)

Bank5 [2]:

- 0: Open drain (active low)
- 1: Push-pull (active high)

Bank5 [3]:

- 0: GPIO4 for address
- 1: GPIO4 for touch and hold output

4.4 Identification

4.4.1 Revision Identification

The device revision information is included as part of the top-side marking on the device package as shown below. The hardware revision is also stored as shown in the table below:

Description	Address	offset 0	offset 1
Product number, Version number (2 bytes)	00h	0x4F – IQS269A	0x01 – device version 0 (pre-production) 0x02 – device version 1 (production - obsolete) 0x03 – device version 2 and 3 (production)
Hardware revision, Minor FW revision (2 bytes)	01h	0x0D or 0x4D – device version 2 0x2D or 0x6D – device version 3	0x03 – device version 2 0x10 – device version 3

4.4.2 WLCSP16 Device Identification

The device type can be identified from the top-side marking on the device package as shown below:

269A = device name (IQS269)

zz = configuration / xx = batch code (AA, AB …. ZZ)

v = IC version number (0 – Pre-production, 1 – Production obsolete, 2 – Production, 3,4 – Production; see PCNs)

ppp = product code

● = Pin A1 indicator

4.4.3 QFN16 Device Identification

The device type can be identified from the top-side marking on the device package as shown below:

IQS269A = device name

zz = configuration

xx = batch code

v = IC version number (e – Engineering, 0 – Pre-production, 1 – Production – obsolete, 2 – Production, 3 – Production; see PCNs)

ppp = Product code

● = Pin A1 indicator

5 I²C Interface

5.1 I²C Module Specification

The device supports a standard two wire I²C interface with the addition of an RDY (ready interrupt) line. The communications interface of the IQS269A supports the following:

- *Fast-mode (Fm)* standard I²C up to 400kHz.
- Streaming data as well as event mode.
- The master may address the device at any time. If the IQS269A is not in a communication window, address polling will be acknowledged immediately with minimal clock stretching.
- The provided interrupt line (RDY) is an open-drain active low implementation and indicates a communication window.

The IQS269A implements 8bit addressing with 2 bytes at each address. Two consecutive read/writes are required in this memory map structure. The two bytes at each address will be referred to as "byte 0" and "byte 1".

5.2 I²C Address

The IQS269A (order code: IQS269A00CSR / IQS269A00QNR) offers 2 address options:

- Default: 0x44
    - Float GPIO4 (Internal pull-up defined)
- Alternate: 0x45
    - GND GPIO4

Other address options exist on special request. Please contact Azoteq.

The order codes: IQS269AD0CSR / IQS269AD0QNR have a fixed I²C address of 0x44 with no alternate option.

5.3 I³C Compatibility

This device is not compatible with an I³C bus due to clock stretching allowed for data retrieval.

5.4 I²C Read

To read from the device a *current address read* can be performed. This assumes that the address-command is already setup as desired.

Current Address Read

Start	Control byte		Data n		Data n+1		Stop
S	**Addr + READ**	**ACK**		**ACK**		**NACK**	**S**

Figure 5.1 Current Address Read

If the address-command must first be specified, then a *random read* must be performed. In this case, a WRITE is initially performed to setup the address-command, and then a repeated start is used to initiate the READ section.

Random Read

Start	Control byte		Address-command		Start	Control byte		Data n		Stop
S	Addr + WRITE	ACK		ACK	S	Addr + READ	ACK		NACK	S

Figure 5.2 Random Read

5.5 I^{2}C Write

To write settings to the device a *Data Write* is performed. Here the Address-Command is always required, followed by the relevant data bytes to write to the device.

Data Write

Start	Control byte		Address-Command		Data n		Data n+1		Stop
S	Addr + WRITE	ACK		ACK		ACK		ACK	S

Figure 5.3 I^{2}C Data Write

5.6 Stop-bit Disable Option

For specific I^{2}C master limitations, the IQS269A offers the following:

- I^{2}C settings register (0xF2) for stop-bit disable functionality,
- The "stop bit disable" bit for ignoring the I^{2}C stop condition from the master. This "ignore" will keep the communication window open.
- The "I^{2}C end window" condition bit making it possible to set the "stop-bit enable" only once.
  - The command will cause the communication window to close only at the next stop-bit sent from the master.
  - The benefit from using this command is that the "stop-bit disable" does not need to be enabled again at the next communication window.
  - All settings written before and after setting this bit will be applied as long as it is written before any stop bit is sent from the master.
- The RDY timeout period register (0x85, offset 0) can be used for an automatic time-out. The timer will start from the last byte on the bus. In this case no intervention from the master is required to end the communications window.

Customers using an MCU with a binary serial-encoder peripheral which is not fully I^{2}C compatible (but provide some crude serial communication functions) can use this option to configure the IQS269A so that any auto generated stop command from the serial peripheral can be ignored by the IQS269A I^{2}C hardware. This will restrict the IQS269A from immediately exiting a communication window during event mode (reduced communication only for events) until all required communication has been completed and a stop command can correctly be transmitted. Please refer to the figures below for serial data transmission examples.

Please note:

1. Stop-bit disable and I^{2}C end window condition clearing must be performed at the beginning and of a communication window. The first I^{2}C register to be written to ensure no unwanted communication window termination.
2. Leaving the Stop-bit disabled will result in successful reading and writing of registers but will not execute any commands written over I^{2}C in a communication window being terminated after a RDY timeout and with no IQS recognised stop command.

3. The default RDY timeout period for IQS269A is purposefully long (10.24ms) for slow responding MCU hardware architectures. Please set this register according to your requirements/preference.
4. Use the I²C end window condition (0xF2, bit7) to purposefully terminate at the next stop-bit condition generated by the master.
5. For any following I²C communication windows, repeat the sequence of first clearing the I²C end window condition (0xF2, bit7) to prevent exit of the communication window before reading data from applicable event and channel registers.

Stop-bit disable and clear I²C end window condition (bit7)

Communication window open	Start	Control byte		Address-Command		Disable stop-bit		Ignored stop	Continue with reads / writes
RDY = ↓LOW	S	Addr + WRITE	ACK	0xF2	ACK	0x40	ACK	S	...

Figure 5.4 I²C Stop-bit disable and clear I²C end window condition

Read data of register 0xF2

Reads / Writes finished	Start	Control byte		Address-Command		Start	Control byte	Read data		Ignored stop	Communication window still open
...	S	Addr + WRITE	ACK	0xF2	ACK	S	Addr + READ	0x??	NACK	S	RDY = _LOW

Figure 5.5 Read and retain data of register 0xF2

Modify-write register 0xF2

Continue	Start	Control byte		Address-Command		Retain 0xF2 & set end I²C window (bit7)		Stop	Communication window closed
...	S	Addr + WRITE	ACK	0xF2	ACK	0x?? | 0x80	ACK	S	RDY = ↑HIGH

Figure 5.6 Modify-write register 0xF2 to end the communication window

5.6.1 RDY Line Behaviour for Different Device Versions

The IQS269A RDY line behaviour will differ for device version 2 and 3.

- In IQS269A v2, the RDY signal will remain low (even if Stop conditions is issued and ignored by IQS269A) and will only go high after an *I2C end window* command have been issued (or RDY timeout is reached).
- In IQS269A v3, the RDY signal will toggle high immediately when a Stop condition is issued (regardless of using stop condition handling active) but the communication window (internally at IQS269A) will remain open. The I2C end comms command (0xF2 = 0xC1) will close the communication window (or the window will also close if the RDY timeout is reached).

5.7 Watchdog Time-out

The IQS269A is designed to do a watchdog reset if:

- I²C stuck during transmission (number of clock pulses is not a multiple of 9)
- IQS269A was addressed but no further communication initiated, ie, no I²C events happen (no data, no stop or no start)
- I²C bus remain low shortly after POR

- I²C reset command is called.
- Program flow does not execute as expected (or goes wrong due to something like damaged ROM memory)

The IQS269A program flow waits and does NOT reset in the following cases:

- If VREG does not stabilize
- If the zero-cross sync UI is running and there is no sync signal
- If the IC is in test mode (for IC testing or IC OTP programming)

5.8 Clock Stretching and Forcing Communications

Communications with the IQS269A can be forced by addressing the IQS269A and waiting for an acknowledgement (ACK) to be returned after clock stretching the host. The following situations will result in forced communications:

5.8.1 IQS269A Clock Stretching During a Communication Window (RDY Low)

When the RDY signal is already low, to report periodic sampled data (streaming mode) or to indicate an event occurrence (event mode), the IQS269A will stretch the clock line (SCL) after the master has written the address command byte to the device. The clock stretch can be attributed to the IQS269A loading data from the buffer. Clock stretching will be induced each time configuring a new address command byte occurs. The timing diagram for this occurrence is shown below in Figure 5.7.

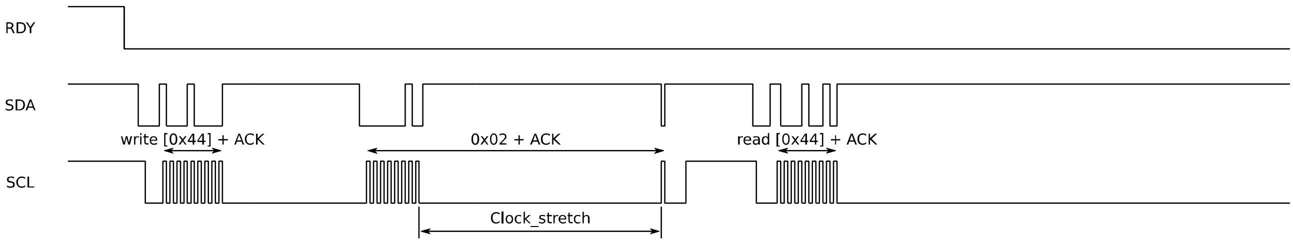


Figure 5.7 Clock Stretching During a Communication Window (RDY Low)

Table 5.1 Clock Stretching Periods During Active Communications (RDY low)

	Minimum	Maximum	Unit
Clock_stretch	60	128	µs

5.8.2 Clock Stretching When MCU Polls IQS269A Without Waiting for RDY Event

The IQS269A will stretch the clock if the master addresses the device outside of a communication window (RDY high). Interrupting the device during ongoing sensor conversions, data processing or inactive (sleep) states will result in slightly longer clock stretching while the IQS269A terminates the task at hand and prepares the communication peripheral to respond. The timing diagram for the event is shown in Figure 5.8 below.

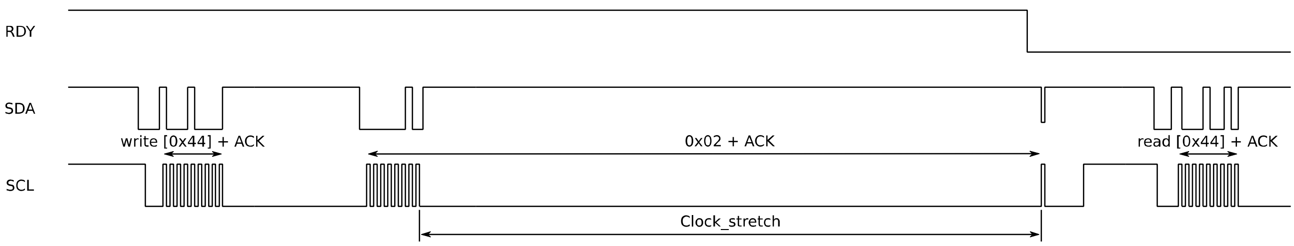


Figure 5.8 Clock Stretching During Inactive Communication (RDY high) Before Opening a Communication Window

Table 5.2 Clock Stretching Periods During Inactive Communications (RDY high)

	Typical	Maximum	Unit
Clock_stretch	250	300	µs

6 I²C Memory Map – Register Descriptions

Table 6.1 IQS269A Register Map Summary

Full address	**Group name**	**Item name (offset 0 – 8bits)**								**Item name (offset 1 – 8bits)**								**Data Access**
		Bit 7							**Bit 0**	**Bit 7**							**Bit 0**	
0x00	Version Info	Product number								Software version								Read-Only
		0x4F – IQS269A								See "version info" link for software revision details								Read-Only
0x01		Hardware number								Minor FW revision number								Read-Only
		See "version info" link for software revision details								See "version info" link for software revision details								Read-Only
0x02	Global flags	System Flags & Power mode flags [1]								Global Event flags								Read-Only
		Show Reset	Reserved		Power mode (see reg 0x80 bits 5:4)		ATI in progress	EVENT	ULP UPDATE	POWER MODE CHANGE	SYSTEM	REFER-ENCE CHAN-NEL	RESERVED	GES-TURE	DEEP-TOUCH	TOUCH	PROX	Read-Only
0x03	Slider event flags	Gesture (Slider1 & Slider 0) event flags								Reserved								Read-Only
		FLICK_-NEG_1	FLICK_-POS_1	HOLD_1	TAP_1	FLICK_-NEG_0	FLICK_-POS_0	HOLD_0	TAP_0									Read-Only
0x04	Channel states	Channels Proximity state								Channels Proximity direction state (for bi-directional triggers – enable in 0x86)								Read-Only
		CH7 (bit 7) → CH0 (bit 0)								CH7 (bit 7) → CH0 (bit 0)								Read-Only
0x05		Channels Touch state								Channels Deep Touch state								Read-Only
		CH7 (bit 7) → CH0 (bit 0)								CH7 (bit 7) → CH0 (bit 0)								Read-Only
0x06		Reference channels actively used								Reserved								Read-Only
		CH7 (bit 7) → CH0 (bit 0)																Read-Only
0x07		Reserved								Reserved								Read-Only
																		Read-Only
		LEAST SIGNIFICANT BYTE								**MOST SIGNIFICANT BYTE**								
0x08	Raw Counts & LTA	FILTERED COUNTS CHANNEL 0 (LSB)								FILTERED COUNTS CHANNEL 0 (MSB)								Read-Only
0x09		LONG TERM AVERAGE CHANNEL 0 (LSB)								LONG TERM AVERAGE CHANNEL 0 (MSB)								Read-Only
0x0A		FILTERED COUNTS CHANNEL 1 (LSB)								FILTERED COUNTS CHANNEL 1 (MSB)								Read-Only
0x0B		LONG TERM AVERAGE CHANNEL 1 (LSB)								LONG TERM AVERAGE CHANNEL 1 (MSB)								Read-Only
0x0C		FILTERED COUNTS CHANNEL 2 (LSB)								FILTERED COUNTS CHANNEL 2 (MSB)								Read-Only
0x0D		LONG TERM AVERAGE CHANNEL 2 (LSB)								LONG TERM AVERAGE CHANNEL 2 (MSB)								Read-Only
0x0E		FILTERED COUNTS CHANNEL 3 (LSB)								FILTERED COUNTS CHANNEL 3 (MSB)								Read-Only
0x0F		LONG TERM AVERAGE CHANNEL 3 (LSB)								LONG TERM AVERAGE CHANNEL 3 (MSB)								Read-Only
0x10		FILTERED COUNTS CHANNEL 4 (LSB)								FILTERED COUNTS CHANNEL 4 (MSB)								Read-Only
0x11		LONG TERM AVERAGE CHANNEL 4 (LSB)								LONG TERM AVERAGE CHANNEL 4 (MSB)								Read-Only
0x12		FILTERED COUNTS CHANNEL 5 (LSB)								FILTERED COUNTS CHANNEL 5 (MSB)								Read-Only
0x13		LONG TERM AVERAGE CHANNEL 5 (LSB)								LONG TERM AVERAGE CHANNEL 5 (MSB)								Read-Only
0x14		FILTERED COUNTS CHANNEL 6 (LSB)								FILTERED COUNTS CHANNEL 6 (MSB)								Read-Only
0x15		LONG TERM AVERAGE CHANNEL 6 (LSB)								LONG TERM AVERAGE CHANNEL 6 (MSB)								Read-Only
0x16		FILTERED COUNTS CHANNEL 7 (LSB)								FILTERED COUNTS CHANNEL 7 (MSB)								Read-Only
0x17		LONG TERM AVERAGE CHANNEL 7 (LSB)								LONG TERM AVERAGE CHANNEL 7 (MSB)								Read-Only
0x18	Channel Deltas (Signed value – 2's complement)	DELTA COUNTS CHANNEL 0 (LSB)								DELTA COUNTS CHANNEL 0 (MSB)								Read-Only
0x19		DELTA COUNTS CHANNEL 1 (LSB)								DELTA COUNTS CHANNEL 1 (MSB)								Read-Only
0x1A		DELTA COUNTS CHANNEL 2 (LSB)								DELTA COUNTS CHANNEL 2 (MSB)								Read-Only
0x1B		DELTA COUNTS CHANNEL 3 (LSB)								DELTA COUNTS CHANNEL 3 (MSB)								Read-Only
0x1C		DELTA COUNTS CHANNEL 4 (LSB)								DELTA COUNTS CHANNEL 4 (MSB)								Read-Only
0x1D		DELTA COUNTS CHANNEL 5 (LSB)								DELTA COUNTS CHANNEL 5 (MSB)								Read-Only
0x1E		DELTA COUNTS CHANNEL 6 (LSB)								DELTA COUNTS CHANNEL 6 (MSB)								Read-Only
0x1F		DELTA COUNTS CHANNEL 7 (LSB)								DELTA COUNTS CHANNEL 7 (MSB)								Read-Only

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							**Bit 0**	**Bit 7**							**Bit 0**	
		LEAST SIGNIFICANT BYTE								**MOST SIGNIFICANT BYTE**								
0x20	Reference channel deltas (the reference channel affects the channel LTA by this delta amount when the channel is in proximity or touch) Signed value, 2's complement	REFERENCE CHANNEL DELTA of CHANNEL 0 (CH0 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 0 (CH0 Weight applied) (MSB)								Read-Only
0x21		REFERENCE CHANNEL DELTA of CHANNEL 1 (CH1 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 1 (CH1 Weight applied) (MSB)								Read-Only
0x22		REFERENCE CHANNEL DELTA of CHANNEL 2 (CH2 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 2 (CH2 Weight applied) (MSB)								Read-Only
0x23		REFERENCE CHANNEL DELTA of CHANNEL 3 (CH3 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 3 (CH3 Weight applied) (MSB)								Read-Only
0x24		REFERENCE CHANNEL DELTA of CHANNEL 4 (CH4 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 4 (CH4 Weight applied) (MSB)								Read-Only
0x25		REFERENCE CHANNEL DELTA of CHANNEL 5 (CH5 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 5 (CH5 Weight applied) (MSB)								Read-Only
0x26		REFERENCE CHANNEL DELTA of CHANNEL 6 (CH6 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 6 (CH6 Weight applied) (MSB)								Read-Only
0x27		REFERENCE CHANNEL DELTA of CHANNEL 7 (CH7 Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL 7 (CH7 Weight applied) (MSB)								Read-Only
0x28 0x29 0x2A 0x2B 0x2C 0x2D 0x2E 0x2F	Reserved	Reserved																Read-Only
0x30	Slider output	SLIDER 0 COORDINATE								SLIDER 1 COORDINATE (N/A for IQS269A D0 option – 5 second timer)								Read-Only
0x31 0x32 0x33 0x34	Capacitance Measurement Data	Contact Azoteq for details on implementation. Use GUI (Azoteq PC software) where capacitance values need to be analyzed.																Read-Only
0x35	Calibration data	HALL bin HL (left plate)				HALL bin HR (right plate)				Reserved								Read-Only
0x36		Reserved								Reserved								
0x80	PMU and System settings	Power mode general settings								General settings & commands								Read-Write
		Main oscillator change '0' – 16MHz, '1' – 4MHz	Enable CH0 ultra low power (ULP) mode	Auto power mode switching '0' enable '1' disable	Power mode selection (when auto mode switching is disabled) '00' – NP '01' – LP '10' – ULP '11' – Halt mode		ULP Update rate (multiples of ULP sampling rate) '000' – 2, '001' – 4, '010' – 8 '011' – 16, '100' – 32, '101' – 64, '110' – 128, '111' - 255			Slider UI is '0' Flick or '1' Swipe (Flick requires release)	Advan-ced[2]	Event mode '0' Disable, '1' Enable	Advan-ced[3]	Advan-ced[4]	**CMD:** REDO-ATI (Define channels to ATI in reg 0x8B byte 1)	**CMD:** SOFT-RESET	**CMD:** ACK-RESET (Clears "Show reset" – reg 0x02 byte 0 bit 7)	Read-Write
0x81	(continued)	Active Channels								Raw count and LTA filter settings								Read-Write
		CH7 (bit 7) → CH0 (bit 0)								LTA Filter Strength_LP		Count Filter Strength_LP		LTA Filter Strength_NP		Count filter strength_NP		Read-Write
0x82		Channel Reseed Enable (Enable "LTA Halt time-out" according to reg 0x85 byte 2)								Global event mask (prevent the following event types from being generated)								Read-Write
		CH7 (bit 7) → CH0 (bit 0) Default: 0xFF								Power Mode Change	System (eg ATI, RESET)	Refer-ence channel	Reserve	Gesture (egSwipe, tap)	Deep-Touch	Touch	Proximity	Read-Write
0x83	Report rates and timings	Normal power report rate								Low power report rate								Read-Write
		0-255ms (4 - 240ms recommended)								0-255ms (4 - 240ms recommended)								Read-Write
0x84		Ultra-low power report rate (CH0 only – set "NP segment update rate" for periodic update of other channels)								Power mode timer								Read-Write
		(x16) 0 – 4080ms								(x512) 0 – 130 560ms								Read-Write
0x85		RDY time-out								LTA Halt timeout (Proximity / Touch timeout) 0xFF = never timeout								Read-Write
		(x0.5) 0 – 127.5ms Default: 10ms								(x512) 0 – 130 560ms								Read-Write

[1] When in "Event mode" the master must read at least byte 0 from register 0x02 to "clear" a registered event

[2] Advanced Setting: 8 Count Reseed Offset – After ATI procedure or reseed event, the LTA counts are forced 8 counts higher (self-capacitance) / lower (mutual capacitance) than the actual measured signal counts

[3] Advanced setting: Comms in NP – '0' normal event mode, '1' event mode in LP, streaming in NP mode

[4] Advanced setting: Comms during ATI – enable streaming communication during ATI procedure

Address	Name																	Access
0x86	Global settings	GENERAL_SETTINGS0								GENERAL_SETTINGS1								Read-Write
		Advanced[1]	ATI_LP (only ATI in LP mode – a more stable time to allow ATI)	ATI_BAND '0' = 1/8 '1' = 1/16 counts around the target count	Disable count filter '0' = filter '1' = raw	Reserve	GPIO3 touch output channel selection Bits 2-0 = Channel 0 – 7 '000' – Channel 0 '001' – Channel 1 '010' – Channel 2 '011' – Channel 3 '100' – Channel 4 '101' – Channel 5 '110' – Channel 6 '111' – Channel 7			Reserve Set "0"	Bi-directional (2-sided) threshold triggers[2]	Advanced[3] (For inductive sensing mode) Recommended: "00"		Reserved Set "000"			Global CAL-cap 0 – 0.5pF 1 – 1.5pF	Read-Write
0x87	(continued 1)	Reserved								Reference channel & other general settings								Read-Write
		N/A								Reference channel default UI Reseed when: '00' – No event '01' – Prox event '10' – Touch event '11' – All events		Reserve Set "0"	Enable reference channel tracking UI	Reserved Set "00"		Slider filter strength '00' 0 (Raw) '01' 1 '10' 2 '11' 3 (Slow)		Read-Write
0x88		Event blocking channel enable (uses reference channel association settings in "CHx Settings")								Reserved								Read-Write
		CH7 (bit 7) → CH0 (bit 0)								N/A								Read-Write
0x89	(continued 2)	Channels selection for Slider 0								Channel selection for Slider 1								Read-Write
		CH7 (bit 7) → CH0 (bit 0)								CH7 (bit 7) → CH0 (bit 0) (N/A for IQS269A D0 option – 5 second timer definition: 0x14 * 256ms)								Read-Write
0x8A		TAP timeout on slider (Required tap channel must be defined in slider)								Slider SWIPE gesture timeout								Read-Write
		x 16ms (0 – 1020ms)								x 16ms (0 – 1020ms)								Read-Write
0x8B		Slider SWIPE gesture threshold								**CMD:** Reseed enable **OR** ATI channel selection if "Redo ATI" bit is set								Read-Write
		x coordinate points (0-255)								CH7 (bit 7) → CH0 (bit 0) Default: "0000 0000" *By default, no channels will ATI when the "Redo ATI" bit is set. Required channels must be selected here.								Read-Write
0xF2	I²C control settings	I²C control settings																
		CMD: I²C end window	I²C disable stop condition handling	I²C disable read only	I²C sleep during ready window	Reserved – internal flags (Note: retain these bits while writing to this register)				N/A								
0xF5	HALL UI enable	HALL UI enable: '0' – Disabled '1' - Enabled								N/A								

[1] Advanced setting: Disable ATI band check. ATI algorithm convergence outside of the 1/8 (default) or 1/16 (small) is allowed without triggering consecutive ATI attempts

[2] If set '1' - Capacitance increase OR decrease will cause threshold crossing. Tip: set for typical use of projected and HALL sensor modes

[3] Advanced setting: TX_CLKD – Select Tx switching frequency. '00' Fosc, '01' Fosc/2, '10' Fosc/4, '11' Fosc/8

Table 6.2 Channel settings register map summary

CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	Item name (offset 0 – 8bits) CHx – Byte0 (Bit 7 … Bit 0)	Item name (offset 1 – 8bits) CHx – Byte1 (Bit 7 … Bit 0)	Data Access
0x8C	0x93	0x9A	0xA1	0xA8	0xAF	0xB6	0xBD	Channel CRX (sensing pin) enable	Channel TX transmit pin enable	Read-Write
								CRX7 (bit 7) → CRX0 (bit 0) (note: CRX1[1])	TX7 (bit 7) → TX0 (bit 0)	Read-Write
0x8D	0x94	0x9B	0xA2	0xA9	0xB0	0xB7	0xBE	Channel Sensing engine settings 1	Channel Sensing engine settings 2	Read-Write
								Advanced[2] Set '1' Reserved[3] Set '0' Advanced[4] Set '1' Internal Cap size '0' 0pF +global '1' 0.5pF +global Reserved Set '00' ATI_mode '11' Full ATI '10' Partial '01' Semi-Partial '00' ATI disabled	Advanced[5] Set '0' Projected mode bias current '00' – 2.5uA '01' – 5uA '10' – 10uA '11' – 20uA ('10' – default) Reserved Set '0' Sensor mode '0000' – Surface '0001' – Projected '1000' – Reserved '1001' – Self & Mutual inductance '1100' – Reserved '1110' – HALL '1111' – Temperature	Read-Write
0x8E	0x95	0x9C	0xA3	0xAA	0xB1	0xB8	0xBF	Channel Sensing engine settings 3	Auto Tuning Implementation (ATI) base value target and count target	Read-Write
								Reserved Set '00' Enable Internal Cap Reser-ved Set '0' Reserved Set '0' Sensing frequency selection (16M/4M) '00' – 4MHz/1MHz '01' – 2MHz/500kHz '10' – 1MHz/250kHz '11' – 500kHz/125kHz static fine multipliers (HALL) '0' – Off '1' – On	ATI Base value '00' – 75 '01' – 100 '10' – 150 '11' - 200 ATI Target (x 32)	Read-Write
0x8F	0x96	0x9D	0xA4	0xAB	0xB2	0xB9	0xC0	Channel Multiplier Setting – normal use is read only	Compensation (ATI) – normal use is read only	Read-Write
								Compensation (MSB) Coarse operating point (ATI) Fine operating point (ATI)	Compensation (LSB)	Read-Write
0x90	0x97	0x9E	0xA5	0xAC	0xB3	0xBA	0xC1	Channel Proximity Threshold = 0-255 counts	Channel Touch Threshold = x/256 of LTA value	Read-Write
0x91	0x98	0x9F	0xA6	0xAD	0xB4	0xBB	0xC2	Channel Deep Touch Threshold = x/256 of LTA value	Channel Hysteresis for Deep Touch Channel Hysteresis for Touch	Read-Write
0x92	0x99	0xA0	0xA7	0xAE	0xB5	0xBC	0xC3	Reference channel association (this channel is reference channel for up to 7 other channels – if no bits set, this channel is not a reference channel	Associated sensing channel impact weight (if this channel is associated to reference channel – 0 = no impact, 255 = 200% impact)	Read-Write
										Read-Write

[1] CRX1 has a higher capacitance load than other CRX pins due to the pin also available as "inductive bias point" in inductive sensing mode

[2] Advanced setting: Choose alternate fixed internal measurement capacitor – default "1" = 60pF, alternate "0" = 15pF. The smaller capacitor may be beneficial in some non-standard sensing modes.

[3] Reserved setting: P_mir range – set this bit "0"

[4] Advanced setting: Choose to float "0" or GND "1" (default) any inactive sensing pins (CRX)

[5] Advanced setting: Inverse logic direction – setting this bit will cause the trigger behavior to inverse direction eg. Releasing a button will cause a trigger, touching again will clear the trigger. '0' – normal, '1' - inverted

7 Applications, Implementation and Layout

NOTE

Information in the following Applications section is not part of the Azoteq component specification, and Azoteq does not warrant its accuracy or completeness. Azoteq's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Technology Fundamentals

Charge transfer is an effective way Azoteq uses to measure a change in capacitance based upon a fixed capacitance. By means of simple analogy, charge and capacitance are represented by a liquid and a container. The smaller container is the variable capacitance while the larger container is the fixed capacitance.

The smaller container is filled (charged) and then emptied (transferred) into the larger container. The number of times it takes to fill the larger container is representative of the volume (capacitance) of the smaller container. If the number of times it takes to fill the larger container changes, then the volume of the smaller container has changed. In most capacitive touch systems, the interest is not in the absolute capacitance but in the change in capacitance. That is when a touch or other interaction occurs, the capacitance of the smaller container changes and consequently the number of times it takes to charge and empty the smaller capacitance into the larger changes. It is this change that is used to determine if a touch occurred.

The Azoteq ProxFusion® technology allows for two different types of external capacitance to be measured. These two types are called self and mutual capacitance. In addition, the ProxFusion® sensing engine allows for the measurement of various other circuits including inductance, HALL effect, temperature and external sensor elements.

7.2 Reference Schematic

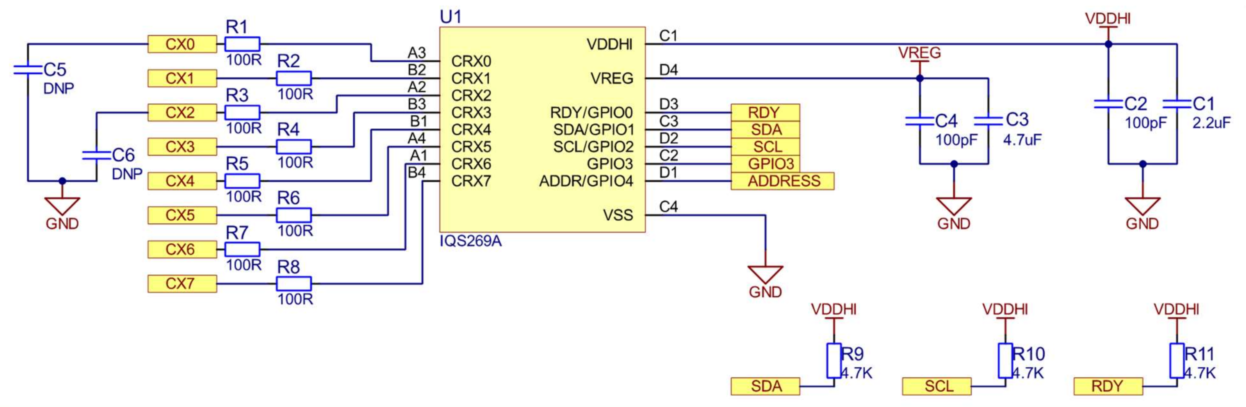


Figure 7.1 Basic Evaluation Kit Schematic

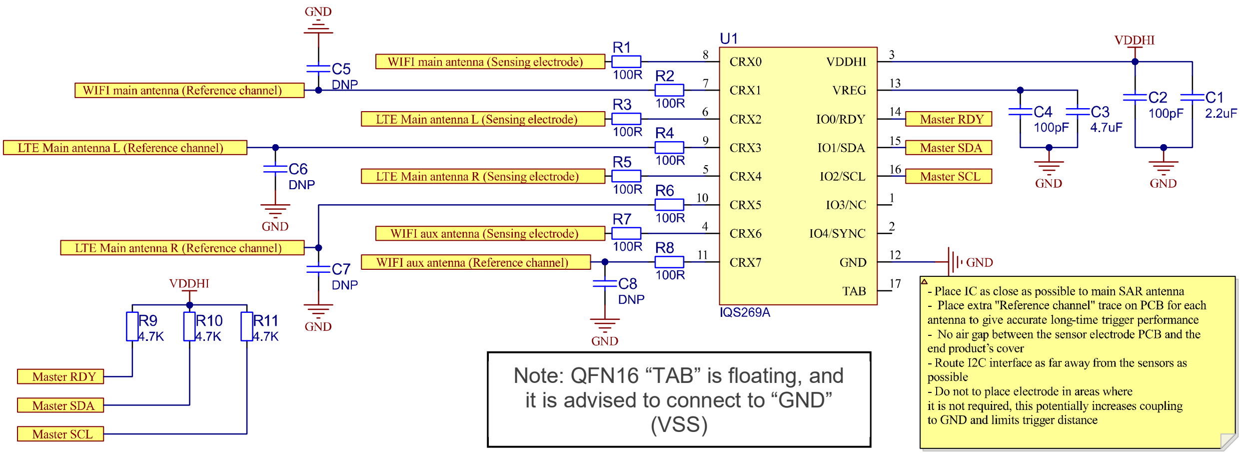


Figure 7.2 Reference Schematic for Limiting SAR Levels in Mobile Devices (Reference Channels for Correcting Typical PCB Changes Over Time)

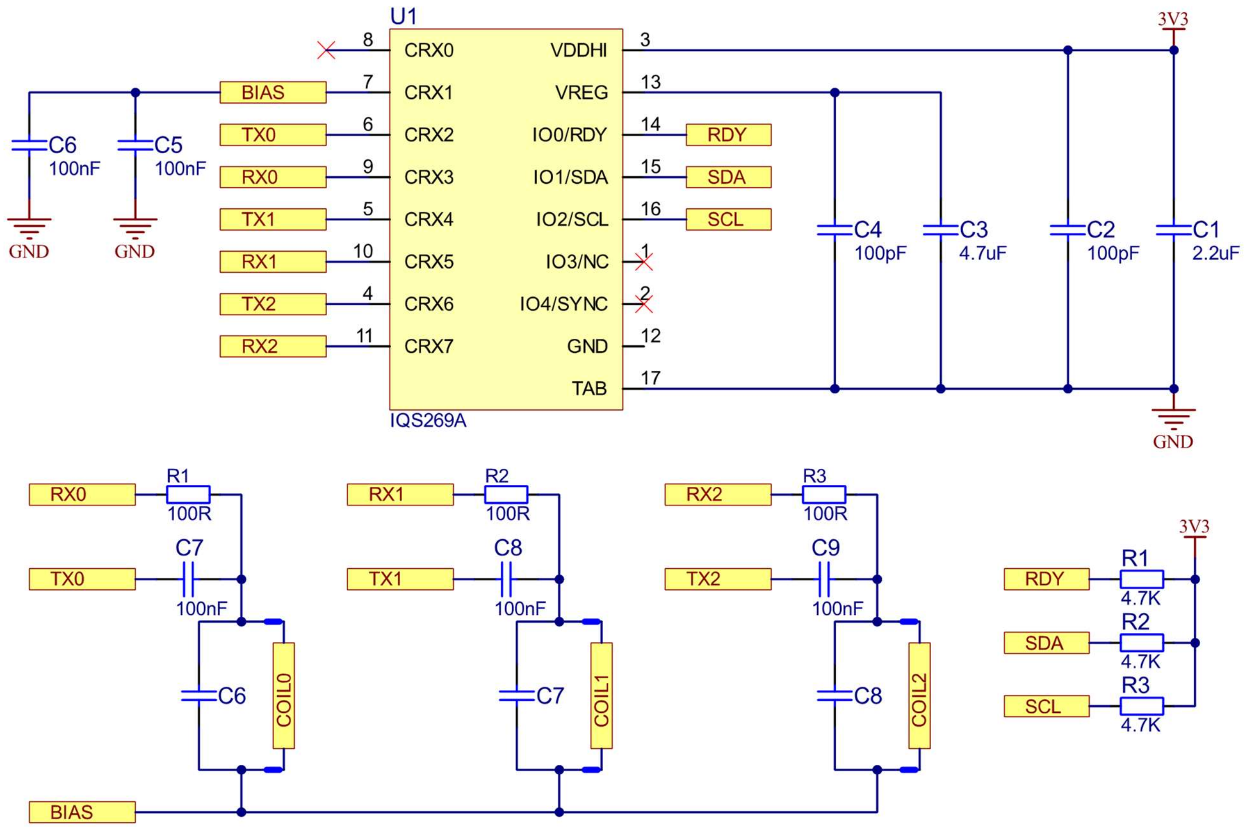


Figure 7.3 Reference Schematic for a 3 Coil Self-inductance Configuration

7.3 Layout Fundamentals

7.3.1 Power Supply Decoupling

Azoteq recommends connecting a combination of a 2.2-µF plus a 100-pF low-ESR ceramic decoupling capacitor to the VDDHI and VSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters). Depending on the application and requirements, 100nF may also be added here for best high frequency noise suppression.

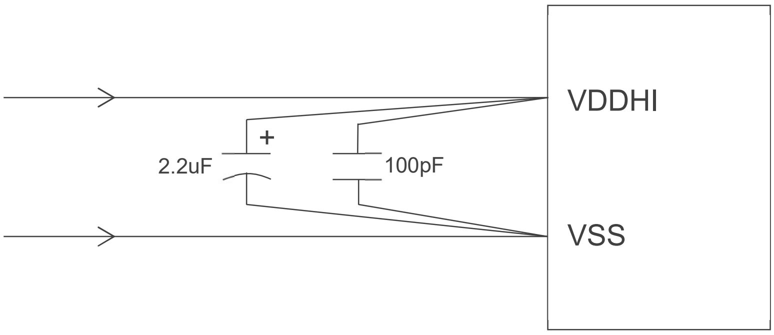


Figure 7.4 Recommended Power Supply Decoupling

7.3.2 Transient Signal Management

During power up, power down, and device operation, VDDHI must not exceed the absolute maximum ratings. Exceeding the specified limits may cause malfunction of the device.

7.3.3 ProxFusion® Peripheral

This section provides a brief introduction to the ProxFusion® technology with examples of PCB layout and performance from a design kit. Please contact Azoteq for more details on design variables not covered here.

7.3.4 VREG

The VREG pin requires at least a 1-µF capacitor to regulate the LDO internal to the device (VREG). This capacitor must be placed as close as possible to the microcontroller. Figure 7.5 shows an example layout where the capacitor is placed close to the IC.

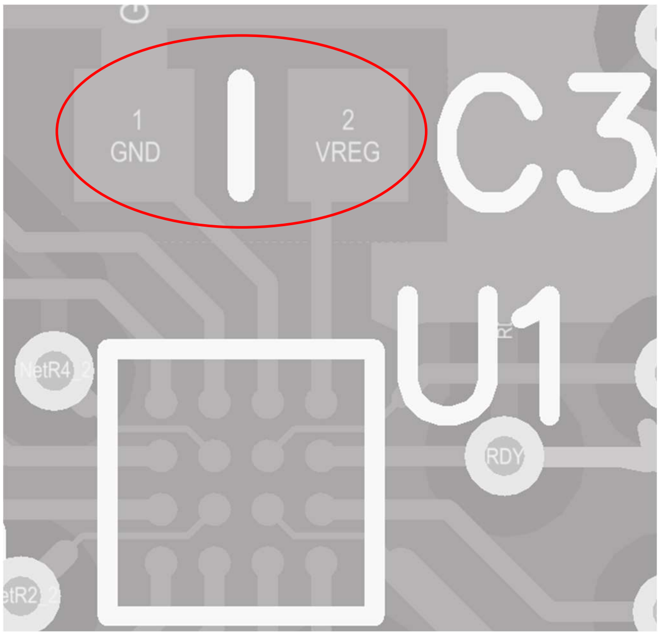


Figure 7.5 VREG External Capacitor Placement

Table 7.1 VREG minimum and recommended capacitor values

Report rate maximum	64ms	128ms	160ms	256ms	Recommended for general design
C_{VREG} minimum[1]	2.2uF	2.2uF	3.3uF	3.9uF	4.7uF
C_{VDDHI} recommended[2]	1uF	1uF	1.5uF	1.5uF	2.2uF

7.3.5 Recommended VREG and VDDHI capacitor ratio

For supplies with low in-line resistance and high current output capability is it recommended to ensure $C_{VREG} > 2C_{VDDHI}$. This is to prevent a known ESD risk.

Known risk: The IQS269A will not recover from ESD events is the following conditions are met:

- VDDHI source is present with low impedance path and high current sourcing capability
- $C_{VDDHI} > C_{VREG}$

With these conditions met, the source keeps VDDHI above the BOD level during the ESD event but drains the VREG capacitor during sleep mode causing a unique sleep-mode BOD event keeping the IC in reset. This only recovers when forcing a POR on VDDHI.

For supplies with a high in-line resistance (such as battery with high series resistance) it is recommended to ensure $C_{VDDHI} > C_{VREG}$ to prevent an unexpected dip on VDDHI when the sensor wakes from sleep-mode and re-charging the VREG capacitor.

7.3.6 ESD Protection

Typically, the laminate overlay provides several kilovolts of breakdown isolation to protect the circuit from ESD strikes. More ESD protection can be added with a series resistor placed on each channel used. A value of 470 Ω is recommended.

7.3.7 Self-capacitance Electrode Design

Self-capacitance electrodes are characterized by having only one channel from the IC that both excites and measures the capacitance. The capacitance being measured is between the electrode and circuit ground, so any capacitance local to the PCB or outside of the PCB (a touch event) influences the measurement.

For PCB layout design it is important to minimize local parasitic capacitances while shielding (with circuit GND) the self-capacitance traces against mechanical changes, induced noise and temperature effects of the board material. Minimize the local parasitic capacitances in order to maximize the effect of external capacitances (proximity and touch effects). To minimize parasitic effects on the PCB, the ground pour on the bottom layer is hatched and there is no pour directly below the electrode: 1.27mm spacing between the electrode and ground fill.

[1] Based on sleep mode current consumption of "I_{sleep}" with starting voltage "V_{VREG_OUT}" minimum voltage and discharge voltage > V_{VREG_BOD} maximum at the end of the sleep period

[2] Based on section 7.3.5

8 Power Mode Description

Auto power mode switching is a time and event-based mode control implemented to automatically adjust between the three available power modes. The auto mode switching is enabled by default and can be disabled by clearing the bit option in register 0x80 bit5. Enabling auto power mode switching will allow the IQS269A to switch between power modes normal, low and, if enabled, ultra-low power based on the occurrence of prox or touch, or the absence thereof for a fixed period. The sequence and timings of power mode switching is shown in Figure 8.1 below. The IQS269A will start up in normal power mode and switch to low power and ultimately ultra-low power if no event is recorded on any enabled channels. The inactive period before a power mode switch occurs (from NP to LP or from LP to ULP modes) is defined as the power mode timer, configurable in 512ms increments in register 0x84 offset 1. If a prox or touch event occurs on a channel while the IQS269A is in low or ultra-low power mode, the IQS269A will switch to normal power to update all channels.

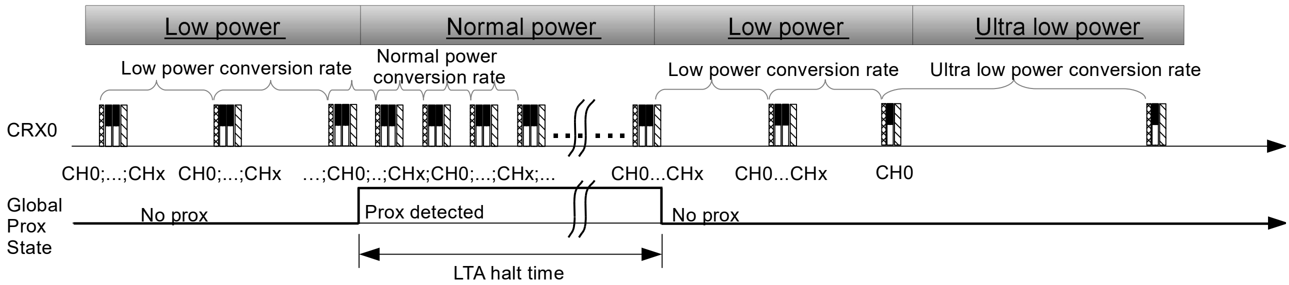


Figure 8.1 Power Mode Switching Timing Diagram

8.1 Normal Power (NP) Mode

Normal power mode continuously updates all channels that are enabled. The rate at which updates occur can be set in register 0x83, offset 0. The timing for normal power mode is shown in Figure 8.2 below.

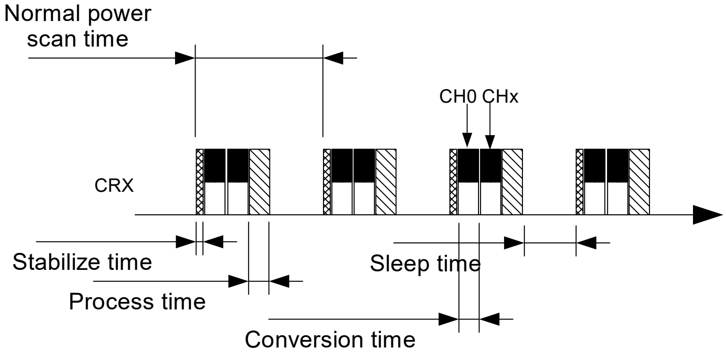


Figure 8.2 Normal Power Mode Conversion Process

8.2 Low Power (LP) Mode

The IQS269A will switch from normal power mode to low power mode if no prox or touch event is registered on any enabled channels for a predefined time. Low power mode continuously updates all channels that are enabled at a lower sampling rate than normal power. The rate of the updates can be set in register 0x83 offset 1. The timing diagram for low power mode is shown in Figure 8.3 below.

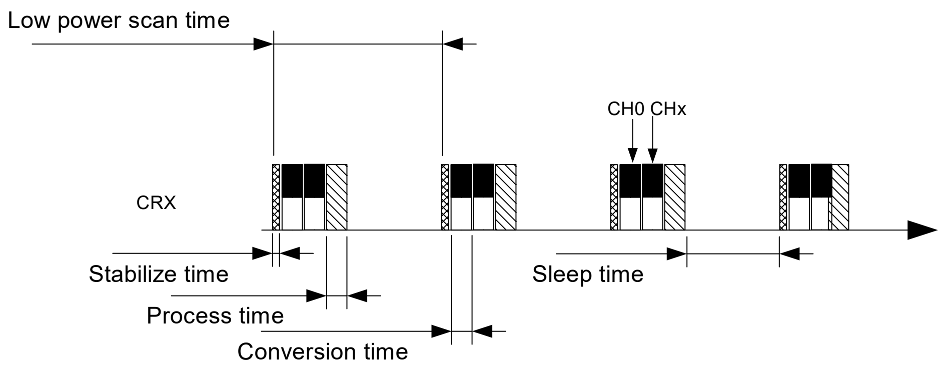


Figure 8.3 Low Power Mode Conversion Process

8.3 Ultra-low Power (ULP) Mode

The IQS269A will switch from low power mode to ultra-low power mode if no prox or touch event is registered on any enabled channels for a predefined time. The IQS269A will continuously update Channel 0 and only update all other enabled channels every n^{th} cycle, with n defined by the selectable ULP update rate. The ULP update rate options can be selected by bit 0-2 in register 0x80, offset 0. A diagram of the ultra-low power conversion process (with ULP update rate: n = 4) is shown in Figure 8.4 below.

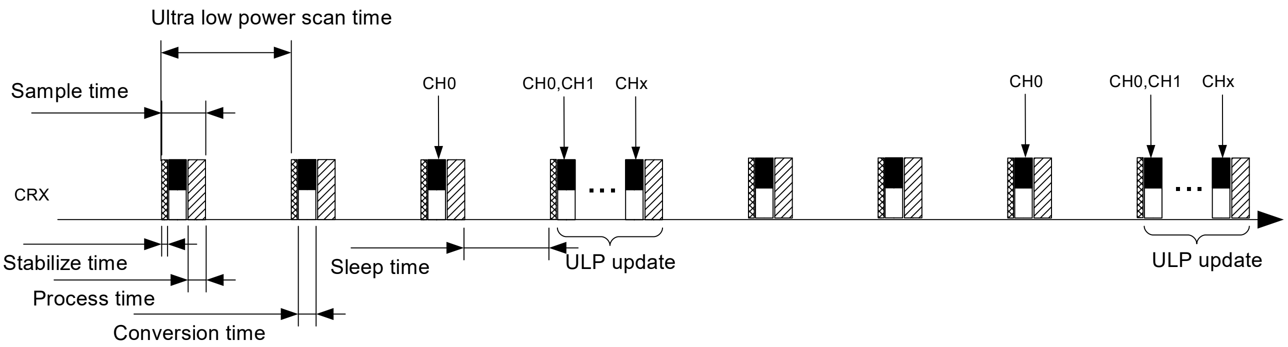


Figure 8.4 Ultra-low Power Mode Conversion Process

9 How to Setup a HALL Effect Sensor

Crx0 (right plate) / Crx1 (left plate) and Crx6 (inverse) setting for HALL sensing have no impact on external connections to CRX0 & CRX6.

The ATI (auto-calibration) of the Hall channels will be handled by the IQS269A. The feature will be restricted to channels 6 and 7.

Required setup:

- This feature may be enabled by setting bit 7 at 0xF5
- Channels 6 and 7 must be enabled and set to Hall sensing mode
- The reseed enable setting (0x82) of channels 6 and 7 must both be cleared.
- The Hall plate selection (0xB6 and 0xBD, bits 0-1) of channels 6 and 7 must be equal.
- The Hall polarity (0xB6 and 0xBD, bit 6) of channels 6 and 7 must not be equal.
- The ATI of channel 6 must be disabled.
- The ATI target of channels 6 and 7 must be equal. (This is required since the counts of the channels are inverted around their respective ATI targets.)
- The Inverse logic bit, for both channels, must be set at 0xB7 and 0xBE, bit 15 (This makes the channels dual-directional)

10 How to Use HALL Bin Values

The ATI feature provided by the IQS269A automatically calibrates the hall channels to achieve a desired target value.

However, due to variation in the production of each IC, the sensitivity of each hall sensor to a given magnetic field is different. This variation is a result of differences in the bias current flowing through the hall effect circuitry. During production, the bias currents for the hall sensors are measured, and each hall sensor is designated a "bin" value to indicate its bias current.

Furthermore, different sensitivities may be required for different applications and different magnet strengths. It is therefore necessary to calibrate each hall-sensing channel based on its application and its bin value.

10.1 Overview

The sensitivity of a hall channel can be adjusted by choosing an ATI target value that will result in a desired maximum counts value in the presence of a magnet. As an example, a hall sensor switch may require the counts value to reach 1000. (Note that, depending on the orientation of the magnet, the counts value may increase or decrease. Maximum counts defined here assumes the counts increases to a maximum value, above the ATI target.)

The required ATI target value can be calculated from:

$$N_T = \left(n_z^{-1} + N_B^{-1} \times \frac{i_a}{I}\right)^{-1}$$

Where:

- N_T = ATI target
- i_a = Signal on hall plates
- I = DC bias current in hall plates
- N_B = ATI base value
- n_z = Desired maximum counts

The base value N_B is decided beforehand. The bias current is obtained from the hall sensor's bin value. These bin values can be read from the IC in register 0x35 (byte 0).

Bit	7	6	5	4	3	2	1	0
0x35	Hall bin (Left - CX1)				Hall bin (Right – CX0)			

The bin values map to bias currents I as shown in the following table:

Bin	Min (uA)	Max (uA)	Bin	Min (uA)	Max (uA)
0			8	6.00	6.49
1	2.50	2.99	9	6.50	6.99
2	3.00	3.49	10	7.00	7.49
3	3.5	3.99	11	7.50	7.99
4	4.00	4.49	12	8.00	8.49
5	4.50	4.99	13	8.50	8.99
6	5.00	5.49	14	9.00	9.49
7	5.50	5.99	15	9.50	10.00

i_a represents the change in current in the hall plates due to the influence of the magnetic field. This value is necessary to calibrate the hall channel, and it can be measured using the counts provided by the hall sensor.

$$i_a = IN_B|N_T^{-1} - n^{-1}|$$

Here, N_B is the ATI base setting, N_T is the ATI target setting, and n is the counts reading provided by the IC.

10.2 Calibration Process

The following steps show how to calibrate both hall channels on the IQS269A.

1. Power on the IQS269A, with no magnets present.
2. Read the hall sensor bin values from register 0x35.
3. Enable Channel 0 and Channel 1 (register 0x81).
4. Enable hall sensing on both channels (registers 0x8D/0x94).
5. Enable CR0 (right hall sensor) on channel 0, and CR1 (left hall sensor) on channel 1 (registers 0x8C/0x93).
6. Enable “static fine multipliers” (registers 0x8E/0x95).
7. Set initial values for the ATI base and target (registers 0x8E/0x95). 200 and 512, respectively, are good starting values.
8. Redo ATI on both channels.
9. Place the magnet close to the IC, where the maximum counts are expected. The counts will increase or decrease based on the orientation of the magnet. (If the counts reach 8192, see below.)
10. Calculate i_a using the measured counts, ATI base, ATI target, and bias currents.
11. Use the calculated i_a and the desired maximum counts (e.g. 1000) to calculate the required target value, N_T.
12. Remove the magnet, write the new target value to the IC, and redo ATI.
13. Check if the magnet causes the hall channels to reach the desired maximum counts. It may be necessary to repeat the process from step 8 if the desired performance is not achieved. If the sensor is not sensitive enough, a lower base value can be chosen.

If the magnet causes a channel to time out at 8192 counts, setup the channel for the counts to decrease, rather than increase. This can be done by using the other pole of the magnet, or by setting bit 6 of register 0x8C/0x93, offset 0, to invert the direction of the counts.

11 How to Configure Sliders

11.1 Registers to Configure

Table 11.1 Registers to Configure for Sliders

	Register Name	Description
0x89, offset 0	Channel selection slider 0	Select channels associated to slider 0
0x89, offset 1	Channel selection slider 1	Select channels associated to slider 1
0x8A, offset 0	Tap gesture timeout	Timeout value in increments of 16ms
0x8A, offset 1	Swipe gesture timeout	Timeout value in increments of 16ms
0x8B, offset 0	Swipe gesture threshold	Threshold coordinate for flick/swipe gestures
0x80, offset 1 bit7	General setting and commands	Slider UI selection: Flick (requires a release) or swipe (no touch release required) UI
0x82, offset 1 bit3	Gesture global event mask	Event can be masked to prevent event types from being generated

11.2 Gesture Descriptions

The sliders on the IQS269A allow the user to identify 4 gestures: tap, hold, and swipe or flick. Any gesture event occurrence on slider 0 or slider 1 will be indicated by the global gesture event bit in register 0x02 offset 1 bit3. The gesture specifications are described below.

11.2.1 Tap

A tap gesture occurs when the slider receives a touch condition for a period shorter than the timeout defined in register 0x8A, offset 0. The tap gesture will be rejected if the coordinate change is too large, this limit is defined by the value of register 0x8B, offset 0, divided by 2.

The event will set the TAP flag in register 0x03, offset 0, bit 4 (for slider1) or bit 0 (for slider0).

11.2.2 Flick

A flick gesture will be registered if a coordinate change and a touch release is detected on the slider within the swipe gesture timeout period as defined in register 0x8A, offset 1. The flick gesture will be positive if the gesture is detected from CH0 to CH7 and negative if the gesture is detected from CH7 to CH0, depending on the channels selected for the specific slider.

The default slider UI for both sliders is the flick UI (register 0x80 offset 1: bit7 = ‘0’). The alternative slider UI is explained in the next section.

A flick event will be indicated by the specific associated slider event bits in register 0x03 offset 0. The occurrence and direction of the flick gesture can be identified by reading the value of FLICK NEG and FLICK POS in register 0x03 where the bit will be set if the gesture occurred in the relevant direction.

11.2.3 Swipe

A swipe gesture will be recognised if the gesture coordinate change is larger than the threshold specified in register 0x8B, offset 0 and the duration of the gesture, from the initial touch to the instance when the threshold is achieved, is shorter than the timeout specified in register 0x8A, offset 1.

The alternative swipe slider UI needs to be selected by setting register 0x80 offset 1: bit7. This option is globally applied to both sliders.

A swipe event will be indicated by the specific associated slider event bits in register 0x03 offset 0. The occurrence and direction of the swipe gesture can be identified by reading the value of FLICK NEG and FLICK POS in register 0x03 where the bit will be set if the gesture occurred in the relevant direction.

11.2.4 Hold

A hold event will be registered if any slider selected channel, or multiple channels simultaneously, detect a touch for longer than the tap and swipe gesture timeouts defined in register 0x8A.

The event will set the HOLD flag in register 0x03, offset 0: bit 1 (for slider 0) or bit 5 (for slider 1).

The hold gesture is the only gesture flag(s) that will remain set during the total duration of the event.

12 Reference Channel UIs

Introduction

The IQS269A offers the following reference channel UIs

- Reference channel RESEED UI (default)
- Reference channel BLOCKING UI
- Reference channel TRACKING UI

12.1 Reference Channel RESEED UI (default)

Steps to enable RESEED UI:

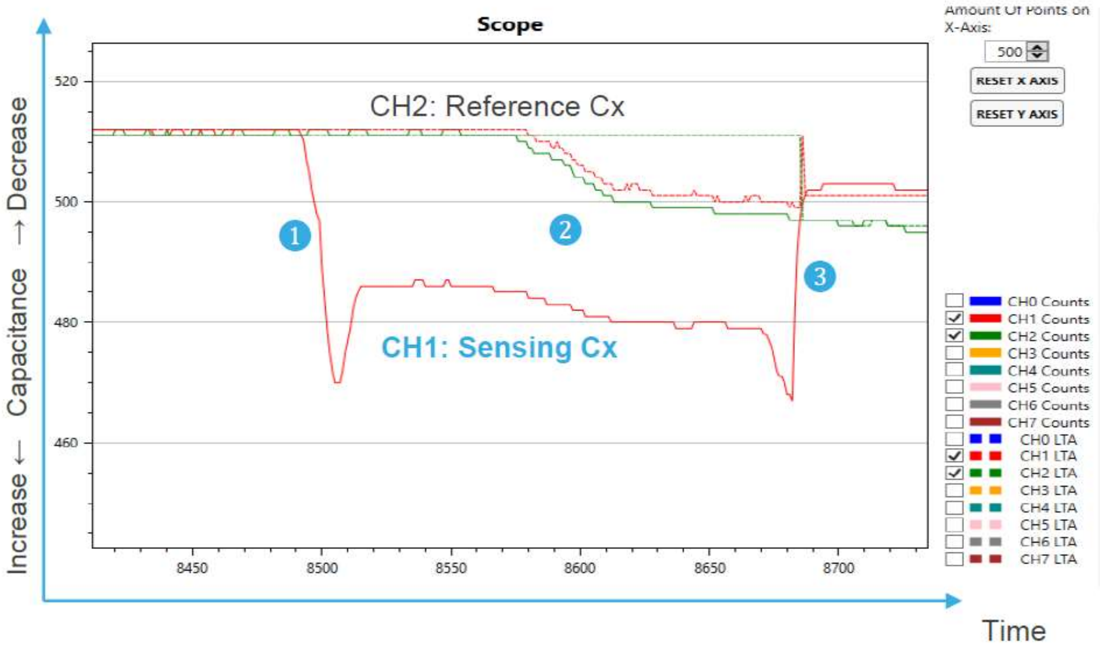
- Enable a specific channel as a reference channel (e.g. register 0x99 byte 0, enable any one or more channels – called “associated channels”).
- Set the reference channel reseed level (global setting: register 0x87 byte 1, bits 6-7)
- Set the reference channel proximity threshold (channel setting: e.g. register 0x97 byte 0) to determine the trigger level when a RESEED is applied to all “associated channels”.
- The reference channel is now ready to apply the intended reseed on the selected “associated channels”

12.2 Reference Channel BLOCKING UI

Steps to enable BLOCKING UI:

- Enable a specific channel as a reference channel (e.g. register 0x99 byte 0, enable any one or more channels – called “associated channels”).
- Change the default RESEED UI of selected channels to BLOCKING UI via register 0x88 byte 0.
- Set the reference channel proximity and touch threshold (channel setting: e.g. register 0x97 byte 0 & 1) to determine at which level proximity and touch events will be blocked on the "associated channels"
- The reference channel is now ready to apply the intended “event blocking” on the selected “associated channels”

12.3 Reference Channel TRACKING UI



Step 1	Step 2	Step 3
Sensing channel trigger. Now reference channel is actively affecting CH1	Heating of PCB. Now, changes on CH2 is applied to reference (LTA) of CH1	Release is successful because the LTA was adapted via the reference channel

Figure 12.1 An Example of a Reference Channel (CH2) Keeping the Sensing Channel (CH1) Output Accurate

As example, refer to 0 where CH1 will be configured with only Cx2 and CH2 configured with only Cx3.

Steps to enable TRACKING UI:

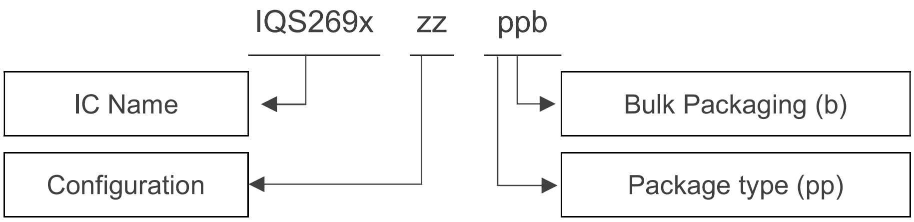
- Enable a specific channel as a reference channel (e.g. register 0x99 byte 0, enable any one or more channels – called "associated channels").
- Change all defined reference channels to have a TRACKING UI (global setting: register 0x87 byte 1, bit 4).
- Set the reference channel reseed & tracking level (global setting: register 0x87 byte 1, bits 6-7)

Bit setting	Reseed level setting	Associated channel NO EVENT	Associated channel in PROXIMITY	Associated channel in TOUCH	Associated channel in DEEP TOUCH
'00'	No event	RESEED UI	**TRACKING UI**	**TRACKING UI**	**TRACKING UI**
'01'	Prox event	RESEED UI	RESEED UI	**TRACKING UI**	**TRACKING UI**
'10'	Touch event	RESEED UI	RESEED UI	RESEED UI	**TRACKING UI**
'11'	Deep touch event	RESEED UI	RESEED UI	RESEED UI	RESEED UI

- Set the reference channel proximity threshold (channel setting: e.g. register 0x97 byte 0) to determine the trigger level when a RESEED is applied to all "associated channels".

13 Ordering Information

Please check stock availability with your local distributor.



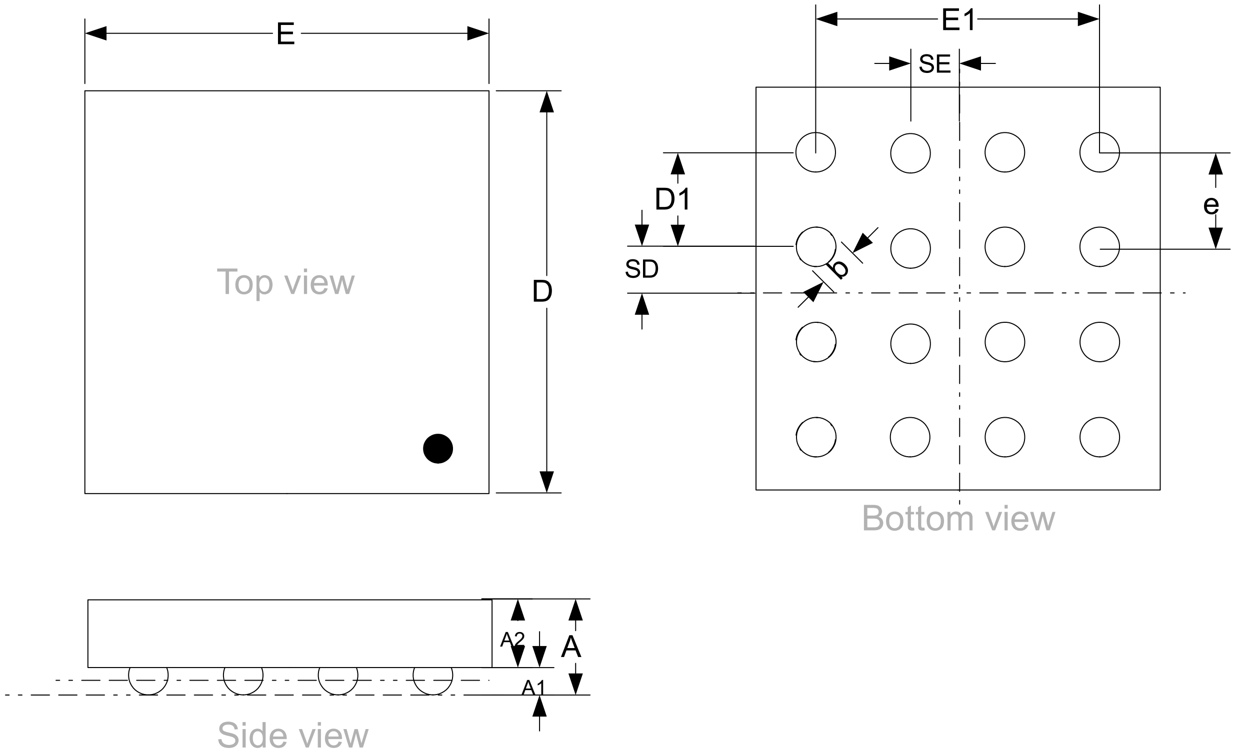
IC NAME	IQS269A	=	IQS269A
CONFIGURATION	zz	=	IC configuration (hexadecimal)
		=	**00** (QFN16 default) **D0** (WLCSP-16 default) TWS touch out **zz** (Minimum order quantities apply)
PACKAGE TYPE	QN	=	QFN16 package
	CS	=	WLCSP-16 package
BULK PACKAGING	R	=	Reel (3000pcs/reel) – MOQ = 3000pcs
		=	MOQ = 1 reel (orders shipped as full reels)

Figure 13.1 Order Code Description

Detailed bulk packaging specifications for this product can be found in AZD054 Package Specifications

14 Package Specification

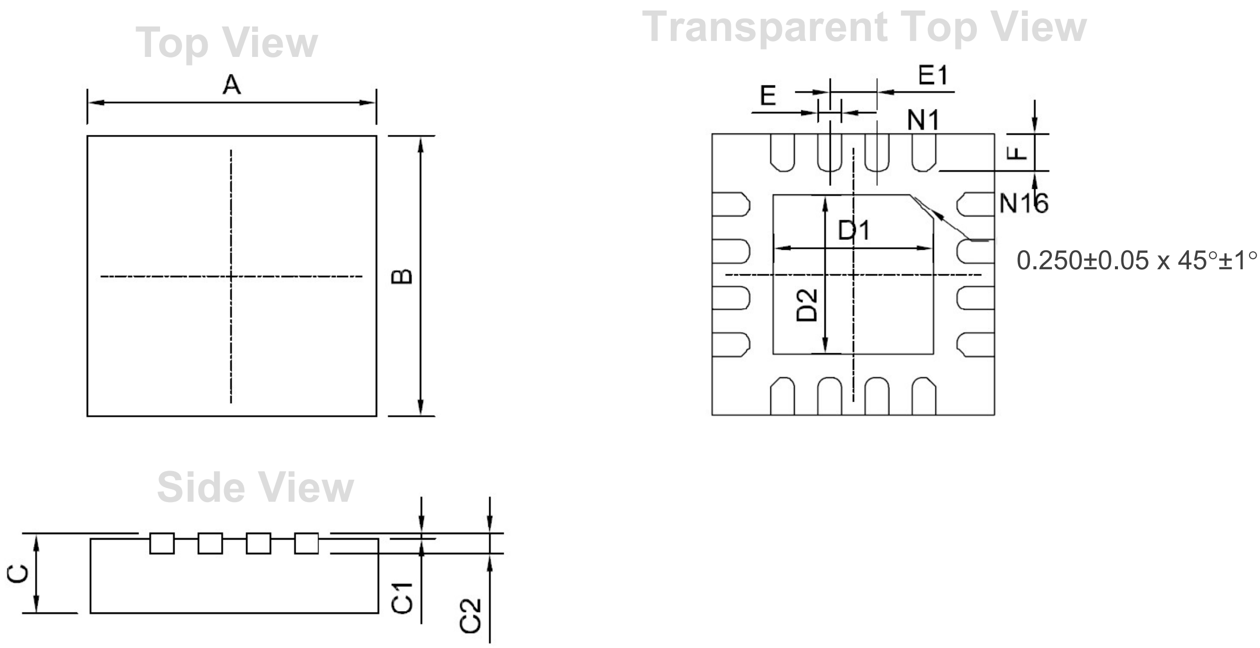
14.1 Package Outline Description – WLCSP16



Dimension	[mm]	Dimension	[mm]
A	0.5±0.05	D1	0.4±0.025
A1	0.2±0.015	SD	0.2 BSC
A2	0.3±0.025	E	1.62±0.05
b	0.25±0.025	E1	1.2
D	1.62±0.05	SE	0.2 BSC
		e	0.4 BSC

Figure 14.1 WLCSP (1.62x1.62)–16 Package Outline Description

14.2 Package Outline Description – QFN16



Dimension	[mm]	Dimension	[mm]
A	3.0±0.1	D1	1.7±0.05
B	3.0±0.1	D2	1.7±0.05
C	0.75±0.05	E	0.25±0.05
C1	0.025±0.025	E1	0.5±0.05
C2	0.203±0.05	F	0.4±0.05

Figure 14.2 QFN(3x3)–16 Package Outline Description

15 Revision History

Revision Number	Description	Date of Issue
V1.0	IQS269A datasheet first release	
V1.4	Template update	
V1.5	SYNC UI explanation inserted RDY line and clock stretching behavior inserted in section 5.8. Power mode descriptions added in section 8 Reference schematic for inductive sensing added. Gesture timer period updated to 16ms Configuration and description of sliders added in section 11. Stop bit disable description added in section 5.6 Corrected the offset for the RDY window timeout in memory map Link to memory map inserted in footer Clarification on Hall touch and deep touch thresholds inserted Hardware ID for version 3 added	5 June 2020
V1.6	I2C options description added to OTP section, I2C section and Order code section SYNC explanation for GPIO3 added Description for I2C stop bit disable on different device versions added in section 5.6.1 IC version 4 information added – mainly explained in change note VDDHI & VREG capacitor recommendations updated throughout datasheet to follow section 7.3.4 recommendations and section 7.3.5 information V_{OL} and V_{OH} parameters added for GPIOs	26 August 2020

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Appendix A. Memory Map Descriptions

Version Info

(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits) Bit 7 … Bit 0	Item name (offset 1 – 8bits) Bit 7 … Bit 0	Data Access
0x00	Version Info	Product number	Software version	Read-Only
		0x4F – IQS269A	0x01 – IC Version mark: "0" (pre-production) 0x02 – IC Version mark: "1" (production – obsolete) 0x03 – IC version mark: "2", "3" & "4" (production)	Read-Only
0x01		Hardware number	Minor FW revision number	Read-Only
		0x0D or 0x4D – Device version 2 0x2D or 0x6D – Device version 3 and 4	0x03 – Device version: 2 0x10 – Device version: 3 and 4	Read-Only

- Specific product checks can be done via registers 0x00 – 0x01
- It is recommended to responsibly check for any firmware or hardware changes at start-up.
- Any changes in this regard will be clearly communicated via a product change notice
- Relevant product change notices for various IC versions can be found at www.azoteq.com

Global Flags

(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x02	Global flags	System Flags & Power mode flags								Global Event flags								Read-Only
		Show Reset	Reserved		Power mode (see reg 0x80 bits 5:4)		ATI in progress	EVENT	ULP UPDATE	POWER MODE CHANGE	SYSTEM	REFER-ENCE CHAN-NEL	RESERVED	GES-TURE	DEEP-TOUCH	TOUCH	PROX	Read-Only

- **Show reset:** "1" indicates the IQS269A has gone through a reset condition and should be initialized again.
- **Power mode:** Report of the currently active power mode
  - "00": Normal power (NP) – all channels sampled fast
  - "01": Low power (LP) – all channels samples slow
  - "10": Ultra low power (ULP) – CH0 sampled slow and other channels slowly updated in the background.
  - "11": N/A
- **ATI in progress:** ATI is a procedure that is done to tune the channel for a target sensing performance. During this procedure it is possible to communicate with the device (via RDY window OR I^2C polling). More on ATI.
- **EVENT:** An indicator that an event has occurred. The power mode timer will be reset in this case.
- **ULP update:**
  - Indication of a sensing update on all active channels during ULP mode.
  - During an update event, the LTA (long-term average) counts are updated for all active channels.
  - If there is a valid state change on any of the active channels, normal power will be entered

- **Global event flags:**
  - POWER MODE – Power mode change has occurred according to the mode timer.
  - SYSTEM – A re-calibration event (ATI), reseed (LTA is made equal to "counts") or reset event has occurred.
  - REFERENCE CHANNEL – A change on a reference channel has occurred and will be applied to a sensing channel. More on reference channels
  - RESERVED
  - GESTURE – A gesture has occurred on slider0 or slider1
  - DEEP TOUCH – An active channel has triggered a "deep touch" threshold
  - TOUCH - An active channel has triggered a "touch" threshold
  - PROX - An active channel has triggered a "proximity" threshold

Slider Event Flags (Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x03		Gesture (Slider1 & Slider 0) event flags								Reserved								Read-Only
		FLICK_-NEG_1	FLICK_-POS_1	HOLD_1	TAP_1	FLICK_-NEG_0	FLICK_-POS_0	HOLD_0	TAP_0									Read-Only

- **Gesture event flags for Slider0 and Slider1:**
  - FLICK_NEG_0/1 – A flick or swipe detected from CH7 side to CH0 side, depending on the channels selected.
  - FLICK_POS_0/1 - A flick or swipe detected from CH0 side to CH7 side, depending on the channels selected.
  - HOLD_0/1 –
    - Any sensing element in the "slider" has been in touch condition for a time longer than the longest of the tap and swipe gesture time-outs as set in register 0x8A.
  - TAP_0/1 –
    - Any sensing element in the "slider" has received a touch condition for a period shorter than defined in register 0x8A.
    - For full specification of tap event requirements, see register 0x8A definition

Channel States (Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x04		Channels Proximity state								Channels Proximity direction state (for bi-directional triggers – enable in 0x86)								Read-Only
		CH7 (bit 7) → CH0 (bit 0)								CH7 (bit 7) → CH0 (bit 0)								Read-Only
0x05		Channels Touch state								Channels Deep Touch state								Read-Only
		CH7 (bit 7) → CH0 (bit 0)								CH7 (bit 7) → CH0 (bit 0)								Read-Only
0x06		Reference channels actively used								Reserved								Read-Only
		CH7 (bit 7) → CH0 (bit 0)																Read-Only
0x07		Reserved								Reserved								Read-Only
																		Read-Only

- **Channels Proximity state:**
  - When a proximity event has occurred, this register will be updated and report on the proximity state of all channels.
  - "0" – No proximity, "1" – Channel x in proximity.
- **Channels Proximity direction state:**
  - When a threshold trigger is made with the "count value" above the LTA (long term average reference), this bit will be set.
  - With the "count value" below the LTA, this bit will be cleared
- **Channels Touch state:**
  - When a touch event has occurred, this register will be updated and report on the touch state of all channels.
  - "0" – No touch, "1" – Channel x in touch.
- **Channels Deep Touch state:**
  - When a deep touch event has occurred, this register will be updated and report on the deep touch state of all channels.
  - "0" – No touch, "1" – Channel x in deep touch.
- **Reference channels actively used:**
  - When a reference channel is setup and a REFERENCE CHANNEL event is registered, this register will report which reference channels are actively used.

Count, Reference, Delta & Slider Values

(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
		LEAST SIGNIFICANT BYTE								MOST SIGNIFICANT BYTE								
0x08 - 0x17	Raw Counts & LTA	FILTERED COUNTS CHANNEL X (LSB)								FILTERED COUNTS CHANNEL X (MSB)								Read-Only
		LONG TERM AVERAGE CHANNEL X (LSB)								LONG TERM AVERAGE CHANNEL X (MSB)								Read-Only
0x18 - 0x1F	Channel Deltas	DELTA COUNTS CHANNEL X (LSB)								DELTA COUNTS CHANNEL X (MSB)								Read-Only
0x20 – 0x27	Reference channel deltas	REFERENCE CHANNEL DELTA of CHANNEL X (CHX Weight applied) (LSB)								REFERENCE CHANNEL DELTA of CHANNEL X (CHX Weight applied) (MSB)								Read-Only
0x30	Slider output	SLIDER 0 COORDINATE								SLIDER 1 COORDINATE (N/A for IQS269A D0 option – 5 second timer)								Read-Only

- **Raw counts & LTA:** The counts reported here are considered the "raw" output of the sensor.
- **Channel deltas:** Calculated value = LTA - Raw counts. Signed value – 2's complement
  - **Known issue for device version (IC version marking) "0" and "1"**
    - Under normal sensing modes, the delta value here is correct
    - When "reference tracking UI" is enabled, then the delta value is not correct
    - No IC function or output state will be affected by this issue
    - For the correct "Channel Delta", the LTA and Raw counts must be read and subtracted by the master device
- **Reference channel deltas:** the reference channel affects the "associated channel" LTA by this delta amount when the channel is in proximity or touch. The weight defined (eg. register 0x92 for channel 0) is already applied to this delta. This is a signed value, 2's complement.
- **Slider output:**
  - An 8-bit output per slider.
  - This output will only be updated while any channels of the sliders are in a touch state.
  - When the touch is released, the value will indefinitely remain as it was at time of release.
  - Enable register 0x80 byte 1, bit 4 for streaming the detailed slider data
  - **Exception:** With the order option IQS269A D0, slider 1 is disabled permanently and the output register will not indicate any coordinates.

Power Mode and System Settings

(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)								Item name (offset 1 – 8bits)								Data Access
		Bit 7							Bit 0	Bit 7							Bit 0	
0x80	PMU and System settings	Power mode general settings								General settings & commands								Read-Write
		Main oscillator change '0' – 16 MHz, '1' – 4MHz	Enable CH0 ultra low power (ULP) mode	Auto power mode switching '0' enable '1' disable	Power mode selection (when auto mode switching is disabled) '00' – NP '01' – LP '10' – ULP '11' – Halt mode		ULP Update rate (multiples of ULP sampling rate) '000' – 2, '001' – 4, '010' – 8 '011' – 16, '100' – 32, '101' – 64, '110' – 128, '111' - 255			Slider UI is '0' Flick or '1' Swipe (Flick requires release)	Advanced[1]	Event mode '0' Disable, '1' Enable	Advanced[2]	Advanced[3]	**CMD:** REDO-ATI (Define channels to ATI in reg 0x8B byte 1)	**CMD:** SOFT-RESET	**CMD:** ACK-RESET (Clears "Show reset" – reg 0x02 byte 0 bit 7)	Read-Write

- **Main oscillator change:**
  - The default of 16MHz allows for rapid charge transfers and other sampling modes.
  - The optional 4MHz allows for slow charge transfers in highly resistive environments with larger capacitive loads in the charge transfer path.
- **Enable CH0 ultra low power (ULP) mode:**
  - By default, automatic power mode switching will only switch between normal power (NP) mode and low power (LP) mode.
  - By setting this bit another power mode step will be available from LP mode to ULP mode.
  - In ULP mode only CH0 will be actively sensed while other channels will be updated at a slower rate (ULP update rate).
- **Auto power mode switching:**
  - If enabled the IQS269A will automatically step power modes if there are no events.
  - For auto-mode switching there should be no user events within a defined time window (register 0x84 byte 1).
  - Custom sampling rates can be defined for each mode.
- **Power mode selection:**
  - NP – Normal power. The power mode intended for use during event changes to allow for a quick response.
  - LP – Low power. The power mode intended for lower power consumption via a fixed sampling period for all channels.
  - ULP – Ultra low power. The power mode intended for use with a proximity or touch wake-up on CH0. Only CH0 is sampled at a regular interval for a defined wake-up response. Other channels are updated via the "ULP update rate" which periodically updates all channels to keep track of drift and channel states.
  - Halt mode – No sensing done on any channel.
- **ULP update rate:**
  - During ULP mode, active channels other than CH0 require to be updated. This is done at a lower rate than CH0 sampling. The rate is defined as a "normal power segment update rate". The update will occur once for every n^{th} samples of CH0. Options for "n" are as defined below:

Bit option	Update rate – n – no. of ULP samples (CH0) before all channels are updated
'000'	2
'001'	4
'010'	8
'011'	16
'100'	32
'101'	64
'110'	128
'111'	255

- **Slider UI selection:**
  - '0' – Flick UI: Gesture must include a touch release. This UI is less prone to unintentional gestures and typically applies cases where safety or water immunity is important.
  - '1' – Swipe UI: Gesture will be generated as soon as the threshold and time conditions are met. This UI will give an improved user experience via optimal responsiveness.
- **Event mode enable:**
  - '0' – Event mode disabled: A communication window will be given after each sample ("streaming mode"). These windows will be indicated on the RDY pin for efficient communications and sampling.
  - '1' – Event mode enabled: A communication window will only be given when an event has occurred that is not masked in register 0x82, byte 1. This window will be indicated on the RDY pin.

  When an event has occurred, a communication window will be given after each sample, until register 0x02 is read.
- **Command REDO-ATI:** Force an ATI event on all or specific channels by setting this bit along with a selection of channels in reg 0x8B byte 1
- **Command SOFT RESET:** Force a software reset condition, clearing all settings made and reverting back to default values for all registers.
- **Command ACK RESET:** Acknowledge the "show reset" bit from register 0x02 here. The "show reset" bit will be cleared after this command.

[1] Advanced Setting: 8 Count Reseed Offset – After ATI procedure or reseed event, the LTA counts are forced 8 counts higher (self-capacitance) / lower (mutual capacitance) than the actual measured signal counts

[2] Advanced setting: Comms in NP – '0' normal event mode, '1' event mode in LP, streaming in NP mode

[3] Advanced setting: Comms during ATI – enable streaming communication during ATI procedure

Power Mode and System Settings

(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)	Item name (offset 1 – 8bits)								Data Access
0x81		Active Channels	Raw count and LTA filter settings								Read-Write
		CH7 (bit 7) → CH0 (bit 0)	LTA Filter Strength_LP		Count Filter Strength_LP		LTA Filter Strength_NP		Count filter strength_NP		Read-Write
0x82		Channel Reseed Enable (Enable "LTA Halt time-out" according to reg 0x85 byte 2)	Global event mask (prevent the following event types from being generated)								Read-Write
		CH7 (bit 7) → CH0 (bit 0) Default: 0xFF	Power Mode Change	System (eg ATI, RESET)	Refer-ence channel	Reserve	Gesture (egSwipe, tap)	Deep-Touch	Touch	Proximity	Read-Write

- **Active channels**
  - Choose to activate up to 8 channels
  - Each channel activated does sensing in a different time-slot
  - Each time-slot (channel) can be set up in registers 0x8C to 0xC3
  - Each time-slot can be set up to use any sensing technology from external sensing modes to internal sensors.
  - CH0 is special because it is used as a wake-up channel in ULP mode.
- **Raw count and LTA filter settings**
  - Filter strength choices:
    - Weak & fast offers best response rate (Count filter)
    - Weak & fast offers best environmental tracking (LTA filter – prevents a false touch or proximity)
    - Strong & slow offers noise rejection in low SNR cases like proximity sensing (Count filter)
    - Strong & slow offers best performance if detection distance is required to be accurate even for a slow approach (LTA filter – prevent environmental tracking of a slow approach)
  - LTA filter strength (LP)
    - 00 – 5 (weak & fast)
    - 01 – 6
    - 10 – 7
    - 11 – 8 (strong & slow)
  - Count filter strength (LP)
    - 00 – 0 (no filtering)
    - 01 – 1
    - 10 – 2
    - 11 – 3 (strong & slow)
  - LTA filter strength (NP)
    - 00 – 7 (weak & fast)
    - 01 – 8
    - 10 – 9
    - 11 – 10 (strong & slow)
  - Count filter strength (NP)
    - 00 – 1 (weak & fast)
    - 01 – 2
    - 10 – 3
    - 11 – 4 (strong & slow)
- **Channel reseed enable**
  - Reseed = clear touch and proximity conditions by making LTA (long-term average) = channel counts
  - "Reseed enable" = Reseed will be done automatically (on the specific channels) after the timer in 0x85 byte 1 runs out.
  - The timer is reset with any events on any of the channels with reseed enabled. When all channels remain in a steady state, the reseed is executed at the same time on all channels
- **Global event mask**
  - Event reporting can be customized here
  - When a bit is set '1', the event will not be reported via RDY indication and event flags
  - When a bit is cleared '0', the event will be reported via RDY indication and event flags
  - Event flags will remain set and RDY indication will repeat with each sample until the event flag register is read

Report Rates and Timings (Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)	Item name (offset 1 – 8bits)	Data Access
0x83	Report rates and timings	Normal power report rate	Low power report rate	Read-Write
		0-255ms (4 - 240ms recommended)	0-255ms (4 - 240ms recommended)	Read-Write
0x84		Ultra-low power report rate (CH0 only – set “NP segment update rate” for periodic update of other channels)	Power mode timer	Read-Write
		(x16) 0 – 4080ms	(x512) 0 – 130 560ms	Read-Write
0x85		RDY time-out	LTA Halt timeout (Proximity / Touch timeout) 0xFF = never timeout	Read-Write
		(x0.5) 0 – 127.5ms Default: 10ms	(x512) 0 – 130 560ms	Read-Write

- **Normal power report rate**
  - Report rate may be chosen in increments of 1ms
  - A minimum report rate of 4ms is recommended as it is the fastest normal power period that can be reached without inaccuracy. At the minimum sampling rate, the device’s fastest cycle period is limited by the number of active channels and the setup of these channels (charge frequency, target etc.).
  - A maximum limitation of 240ms is recommended on the sampling rate as it is required to accurately execute gesture recognition timings with 16ms increments from the gesture timing limitation settings. A sampling rate higher than 240ms will cause longer or inaccurate gesture timing behaviour.
  - A report rate of 0ms and other low values will result in a best effort to do sampling as fast as possible.
  - As a reference, 8 channels doing capacitive sensing (target count = 1000) at 2MHz will take a minimum time of 4ms to complete.
- **Low power report rate**
  - Report rate may be chosen in increments of 1ms
- **Ultra-low power report rate**
  - Report rate may be chosen in increments of 16ms
  - Active sensing only done for CH0
  - All other channels are updated according to the “ULP update rate” in register 0x80 byte 0 bits 2-0
- **Power mode timer**
  - Automatic power mode stepping will be done when this timer runs out
  - The timer will reset when any user event occurs (user event = threshold trigger/release)
  - Power mode timer may be set in increments of 512ms
- **RDY time-out**
  - A dedicated communication window is given by the RDY window period
  - This register defines this period
  - Default: 10ms
  - If the RDY window is missed, the IC will still rapidly respond to I^{2}C address polling
  - The RDY time-out may be set in increments of 0.5ms
- **LTA Halt timeout**
  - This timer will cause a reseed on all channels with reseed enabled (register 0x82 byte 0)
  - An exception is 0xFF that will block the potential time-out.
  - LTA Halt timeout may be set in increments of 512ms

Global Settings
(Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)						Item name (offset 1 – 8bits)					Data Access
0x86	Global settings	GENERAL_SETTINGS0						GENERAL_SETTINGS1					Read-Write
		Advan-ced[1]	ATI_LP (only ATI in LP mode – a more stable time to allow ATI)	ATI_-BAND '0' = 1/8 '1' = 1/16 counts around the target count	Disable count filter '0' = filter '1' = raw	Reserve	GPIO3 touch output channel selection Bits 2-0 = Channel 0 – 7 '000' – Channel 0 '001' – Channel 1 '010' – Channel 2 '011' – Channel 3 '100' – Channel 4 '101' – Channel 5 '110' – Channel 6 '111' – Channel 7	Reserve Set "0"	Bi-direc-tional (2-sided) threshold triggers[2]	Advanced[3] (For inductive sensing mode) Recommended: "00"	Reserved Set "000"	Global CAL-cap	Read-Write

- **ATI_LP**
  - Only allow auto-ATI if the power mode is LP
  - This allows for the ATI algorithm to run only when the proximity or touch states on all active channels are stable.
- **ATI_BAND**
  - '0' = 1/8
  - '1' = 1/16
  - Recommended value '0' (1/8).
  - Example: 1/8*Target = 0.125*800 = 100; Thus, a band of 100counts above and below the target value is monitored
  - A band of '1' (1/16) could help in some safety critical applications where very accurate sensitivity is required. If such case the ATI algorithm will converge into a smaller band.
- **Disable count filter**
  - Disable all filtering of the raw count values that result directly from the charge transfer measurements or other sensor modes.
- **GPIO3 touch output channel selection**
  - The GPIO3 pin can become the touch flag output of any channel
  - Select any one channel here
- **Bi-directional thresholds**
  - Default thresholds are below the LTA only
  - The LTA will freeze when the counts go down, but the LTA will follow when the counts go upward
  - With this bit set, the LTA will freeze when counts go up or down
  - When set, the threshold triggers will happen in both directions by the amount of counts
  - This option enables 2 directions for all active channels
  - An alternative exists where the threshold and LTA follow direction can be inversed per channel – for example, see register 0x8D byte 1 bit 7.
- **Global CAL-cap**
  - An internal capacitor selection with known sizes are available to add to the sensor pins
  - Some of the selection need to be added globally and the others locally for each channel
  - The internal capacitors will only be applied to the channel if they are enabled per channel – for example, see register 0x8E byte 0 bit 5
  - This bit gives the option to add
    - '0' – 0.5pF
    - '1' – 1.5pF
  - Each channel then gives the ability to add another 0pF or 0.5pF to this, give a full range of options between 0.5pF and 2pF.

[1] Advanced setting: Disable ATI band check. ATI algorithm convergence outside of the 1/8 (default) or 1/16 (small) is allowed without triggering consecutive ATI attempts

[2] If set '1' - Capacitance increase OR decrease will cause threshold crossing. Tip: set for typical use of projected and HALL sensor modes

[3] Advanced setting: TX_CLKD – Select Tx switching frequency. '00' Fosc, '01' Fosc/2, '10' Fosc/4, '11' Fosc/8

Global Settings

(Back to memory map)

<table>
<tr><th>Full address</th><th>Group name</th><th>Item name (offset 0 – 8bits)</th><th colspan="5">Item name (offset 1 – 8bits)</th><th>Data Access</th></tr>
<tr><td rowspan="2">0x87</td><td rowspan="4"></td><td>Reserved</td><td colspan="5">Reference channel & other general settings</td><td>Read-Write</td></tr>
<tr><td>N/A</td><td>Reference channel default UI
Reseed when:
‘00’ – No event
‘01’ – Prox event
‘10’ – Touch event
‘11’ – All events</td><td>Reserve
Set “0”</td><td>Enable reference channel tracking UI</td><td>Reserved
Set “00”</td><td>Slider filter strength
‘00’ 0 (Raw)
‘01’ 1
‘10’ 2
‘11’ 3 (Slow)</td><td>Read-Write</td></tr>
<tr><td rowspan="2">0x88</td><td>Event blocking channel enable (uses reference channel association settings in “CHx Settings”)</td><td colspan="5">Reserved</td><td>Read-Write</td></tr>
<tr><td>CH7 (bit 7) → CH0 (bit 0)</td><td colspan="5">N/A</td><td>Read-Write</td></tr>
</table>

- **Reseed level for reference channel RESEED UI**
  - More on the reference channel RESEED UI
  - Reference channel default UI will
    - reseed (LTA = counts) a connected sensing channel
    - when a proximity/touch threshold trigger is detected on the reference channel
    - the reseed action will be allowed up to a level specified here
  - The reference channel event will cause a ‘reseed’ operation on all of the associated channels if associated channel has:
    - ‘00’ no event,
    - ‘01’ proximity or no event,
    - ‘10’ proximity/touch or no event,
    - ‘11’ prox/touch/deeptouch or no event (always)
- **Enable reference channel tracking UI**
  - When the ‘reference channel tracking UI’ is enabled, the ‘reference channel default UI’ will be disabled.
  - When enabled, this UI will have no effect if the associated sensing channel DOES NOT have a proximity/touch condition.
  - If the associated sensing channel DOES have a proximity/touch condition, the following will happen:
    - The LTA of the reference channel will be halted for the duration of the proximity/touch
    - The delta on the reference channel will be subtracted from the LTA of the sensing channel
    - The delta used will have a channel specific “weight” assigned and may be from 0% to 200% of the reference channel delta
- **Slider filter strength**
  - Slider coordinate filter
  - Values range from raw (‘00’) to strong & slow (‘11’) as shown above
  - Filter is applied for “flick” and “swipe” gesture detection
  - This filter does not affect “tap” gesture detection, normal channel filters apply in this case
- **Event blocking channel enable**
  - This byte determines which channels are blocking channels
  - A "blocking" channel works in conjunction with another channel, as selected in the "Reference channel association: Channel “x" byte (for example register 0x92 byte 0). The purpose of a blocking channel is to alter the event behaviour of the associated channel(s). The following table illustrates the modified event reporting behaviour:

Blocking CH state change	Associated CH state change	Blocking CH state	Associated CH state	Event Reported
None	Activation	No Prox	N/A	Yes
None	Deactivation	No Prox	N/A	Yes
None	Activation	Prox	N/A	No
None	Deactivation	Prox	N/A	No
Activation	None	N/A	Prox	Yes
Deactivation	None	N/A	Prox	Yes
Activation	None	N/A	No Prox	No
Deactivation	None	N/A	No Prox	No
Activation	Activation	N/A	N/A	No
Deactivation	Deactivation	N/A	N/A	No
Activation	Deactivation	N/A	N/A	No
Deactivation	Activation	N/A	N/A	No

Global Settings (Back to memory map)

Full address	Group name	Item name (offset 0 – 8bits)	Item name (offset 1 – 8bits)	Data Access
0x89		Channels selection for Slider 0	Channel selection for Slider 1	Read-Write
		CH7 (bit 7) → CH0 (bit 0)	CH7 (bit 7) → CH0 (bit 0) (N/A for IQS269A D0 option – 5 second timer definition: 0x14 * 256ms)	Read-Write
0x8A		TAP timeout on slider (Required tap channel must be defined in slider)	Slider SWIPE gesture timeout	Read-Write
		x 16ms (0 – 1020ms)	x 16ms (0 – 1020ms)	Read-Write
0x8B		Slider SWIPE gesture threshold	**CMD:** Reseed enable **OR** ATI channel selection if "Redo ATI" bit is set	Read-Write
		x coordinate points (0-255)	CH7 (bit 7) → CH0 (bit 0) Default: "0000 0000" *By default, no channels will ATI when the "Redo ATI" bit is set. Required channels must be selected here.	Read-Write

- **Channel selection for Slider0/1**
  - Select up to 8 channels to define slider 0 and slider 1
  - **Exception:** With the order option IQS269A D0, "Slider 1 coordinate" is disabled and the register is repurposed used for the 5 second GPIO4 hold output timer definition.
- **TAP timeout on slider**
  - A tap (touch & release) within a certain time bound must also adhere to the restriction below
  - A slider coordinate change bound is also applied to the tap gesture. A tap will be rejected if the coordinate change is too big
  - Coordinate shift limit = 0x8B,byte0 (Swipe gesture threshold) divide by 2
- **SWIPE gesture timeout**
  - A swipe gesture must be below the gesture time-out
- **SWIPE gesture threshold**
  - A swipe gesture coordinate change must be more than the gesture threshold chosen
- **Command: Reseed / Redo-ATI**
  - By setting only the bits here, a reseed (LTA = sensor count value) will be executed on corresponding channels
  - By setting bits here along with register 0x80 byte 1 bit 2 (Redo ATI command) in the same communication window, the corresponding channels will re-ATI
  - Note: If the "reseed" action causes the LTA to fall outside of the "ATI band" (register 0x86 byte 0 bit 5), a re-ATI will be triggered automatically.

I²C Control Settings

Full address	Group name	Item name (offset 0 – 8bits)					Item name (offset 1 – 8bits)	Data Access
0xF2	I²C control settings	I²C control settings						
		CMD: I²C end window	I²C disable stop	I²C disable read only	I²C sleep during ready window	Reserved – Internal flags (Note: retain these bits while writing to this register)		Read-Write

- **Command: I²C end window**
  - End the current communication window and return to sensing operations. More on I²C end window here
  - **Note:** This bit is not automatically cleared. This bit must be cleared by the master in the next communications window.
- **I²C disable stop**
  - Disable the stop bit recognition on the IQS269A I²C engine as explained here.
- **I²C disable read-only**
  - Allow writing to read-only registers
- **I²C sleep during RDY window**
  - Let the processor sleep while waiting for comms in the I²C RDY window period
  - This option is to save power in certain applications

HALL UI Enable

0xF5	HALL UI enable	HALL UI enable: '0' – Disabled '1' - Enabled							N/A	

- **HALL UI enable**
  - Set this bit along with the recommended settings below to allow for effective calibration (ATI) of HALL channels in the presence of magnetic fields (typically required for power-on state detection)
  - Set this bit also in order to calculate a delta differentially between a HALL sense plate and its analogue inverse. This typically increases the signal delta and minimizes unwanted offsets.

SYNC UI Enable
(Back to memory map)

0x87		Reserved	Reference channel & other general settings						Read-Write
		N/A	Reference channel default UI Reseed when: '00' – No event '01' – Prox event '10' – Touch event '11' – All events	Reserve Set "0"	Enable reference channel tracking UI	**SYNC UI type: '0' – High / Low '1' – Zero cross**	**Enable SYNC UI on GPIO3**	Slider filter strength '00' 0 (Raw) '01' 1 '10' 2 '11' 3 (Slow)	Read-Write

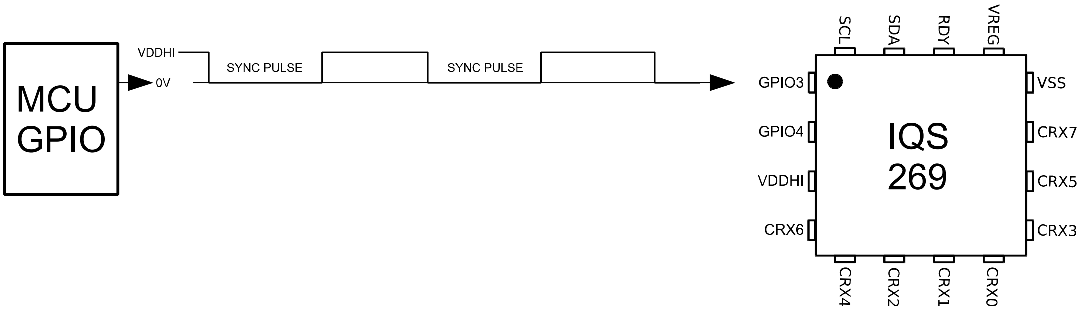

Figure A1: Sync input of the IQS269A

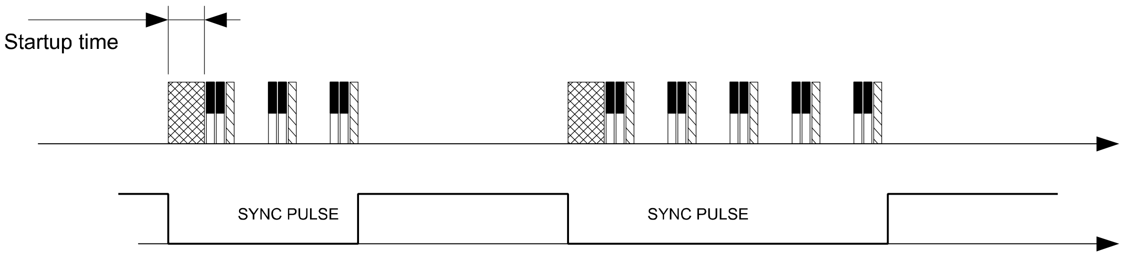

Figure A2: Default High/Low Operation (active low synchronisation)

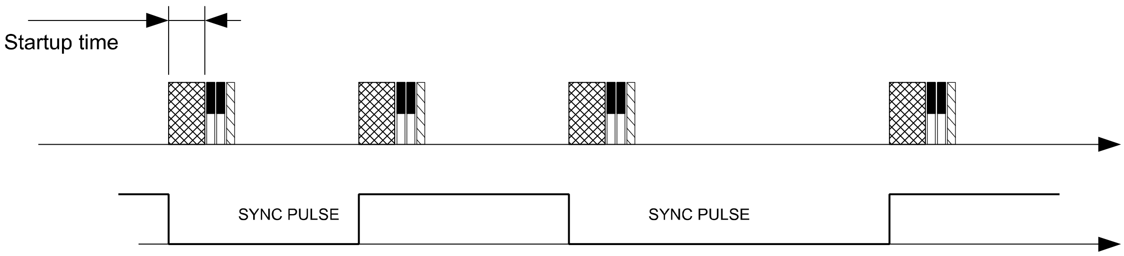

Figure A3: Alternative Zero-Cross Operation (rising and falling edge triggered synchronisation)

If the default SYNC UI is enabled on GPIO3, GPIO3 is held low during conversions. If GPIO3 is held low by the MCU, the IQS269A will continue to execute conversions periodically based on the NP sample period.

If the alternative 100Hz sync UI is enabled, GPIO3 is not held low and conversions will be active for a certain period depending on the system clock (16/4MHz), sensing frequency and sensing mode. The maximum conversion duration will be based on the conversion count limit depending on the type of conversion:

- Self-capacitive mode: 2048
- Projected mode: 4096
- Other: 8192

Channel Settings – Pin Setup

<table>
<tr><td colspan="8">Full address per channel number</td><td colspan="8">Item name (offset 0 – 8bits)</td><td colspan="8">Item name (offset 1 – 8bits)</td><td>Data Access</td></tr>
<tr><td>CH0</td><td>CH1</td><td>CH2</td><td>CH3</td><td>CH4</td><td>CH5</td><td>CH6</td><td>CH7</td><td colspan="8">CHx – Byte0</td><td colspan="8">CHx – Byte1</td><td></td></tr>
<tr><td colspan="8"></td><td>Bit 7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>Bit 0</td><td>Bit 7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>Bit 0</td><td></td></tr>
<tr><td rowspan="2">0x8C</td><td rowspan="2">0x93</td><td rowspan="2">0x9A</td><td rowspan="2">0xA1</td><td rowspan="2">0xA8</td><td rowspan="2">0xAF</td><td rowspan="2">0xB6</td><td rowspan="2">0xBD</td><td colspan="8">Channel CRX (sensing pin) enable</td><td colspan="8">Channel TX transmit pin enable</td><td>Read-Write</td></tr>
<tr><td colspan="8">CRX7 (bit 7) → CRX0 (bit 0)</td><td colspan="8">TRX7 (bit 7) → TRX0 (bit 0)</td><td>Read-Write</td></tr>
</table>

- **Channel CRX enable**
  - Choose external sense pad connections here
  - By selecting more than one external pad per channel, a “distributed channel” is formed
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each CRX is an external pin
      - Each pin is used for charge transfer “charge” and “discharge” operations
      - CRX1 has a reserved circuit connected, do not include CRX1 in designs where even performance is required over various pins. A slightly less sensitive CRX1 may result when compared to other pins
    - Projected capacitance mode:
      - Each CRX pin is an external pin
      - Each pin is used as a sensitive receiver for projected capacitance
    - HALL sensor mode:
      - No CRX pins are externally connected
      - CRX register is re-purposed for HALL channel setup
      - Select CRX0 (right) / CRX1 (left) for the HALL pad (refer to figures 2.1 & 2.2)
      - Select CRX0 (right) / CRX1 (left) and CRX6 for the inverse HALL pad
      - For HALL sensor mode, all other CRX bits should be set to ‘0’
      - Two channels, “HALL pad” and “inverse HALL” pad is required for accurate HALL effect detection
- **Channel TX enable**
  - Choose more external sense pad connections here
  - This register has different functions for different sensor modes:
    - Self-capacitance mode:
      - Each TRX is an external pin definition of the CRX pin state when the pin is not part of any active channel
      - With the corresponding bit set, undefined CRX pins will be GND during sensing conversions of other channels
    - Projected capacitance mode:
      - Each TX pin is an external pin
      - Each pin is used as a transmit pin for projected capacitance
    - HALL sensor mode:
      - No CRX pins are externally connected
      - Select all TX pins for defining the state of unused external pins

Sensing Engine Settings (Back to memory map)

<table>
<tr><td colspan="8">Full address per channel number</td><td colspan="8">Item name (offset 0 – 8bits)</td><td colspan="8">Item name (offset 1 – 8bits)</td><td>Data Access</td></tr>
<tr><td>CH0</td><td>CH1</td><td>CH2</td><td>CH3</td><td>CH4</td><td>CH5</td><td>CH6</td><td>CH7</td><td colspan="8">CHx – Byte0</td><td colspan="8">CHx – Byte1</td><td></td></tr>
<tr><td colspan="8"></td><td>Bit 7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>Bit 0</td><td>Bit 7</td><td></td><td></td><td></td><td></td><td></td><td></td><td>Bit 0</td><td></td></tr>
<tr><td rowspan="2">0x8D</td><td rowspan="2">0x94</td><td rowspan="2">0x9B</td><td rowspan="2">0xA2</td><td rowspan="2">0xA9</td><td rowspan="2">0xB0</td><td rowspan="2">0xB7</td><td rowspan="2">0xBE</td><td colspan="8">Channel Sensing engine settings 1</td><td colspan="8">Channel Sensing engine settings 2</td><td>Read-Write</td></tr>
<tr><td>Advanced[1] Set ‘1’</td><td>Reserved Set ‘0’</td><td>Advanced[2] Set ‘1’</td><td>Internal Cap size ‘0’ 0pF +global ‘1’ 0.5pF +global</td><td colspan="2">Reserved Set ‘00’</td><td colspan="2">ATI_mode ‘11’ Full ATI ‘10’ Partial ‘01’ Semi-Partial ‘00’ ATI disabled</td><td>Advanced[3] Set ‘0’</td><td colspan="2">Projected mode bias current ‘00’ – 2.5uA ‘01’ – 5uA ‘10’ – 10uA ‘11’ – 20uA (‘10’ – default)</td><td>Reserved Set ‘0’</td><td colspan="4">Sensor mode ‘0000’ – Self capacitance ‘0001’ – Projected ‘1000’ – Reserved ‘1001’ – Self & Mutual inductance ‘1100’ – Reserved ‘1110’ – HALL ‘1111’ – Reserved</td><td>Read-Write</td></tr>
</table>

- **Internal Capacitor size:**
  - Select to add only the global capacitance value or adding another 0.5pF to the sensor pin.
- **Projected mode bias current:**

[1] Advanced setting: Choose alternate fixed internal measurement capacitor – default “1” = 60pF, alternate “0” = 15pF. The smaller capacitor may be beneficial in some non-standard sensing modes. Dissimilar measurement capacitor selections for multiple channels and use of ultra-low power (ULP) mode is not recommended.

[2] Advanced setting: Choose to float “0” or GND “1” (default) any inactive sensing pins (CRX).

[3] Advanced setting: Inverse logic direction – setting this bit will cause the trigger behavior to inverse direction eg. Releasing a button will cause a trigger, touching again will clear the trigger. ‘0’ – normal, ‘1’ - inverted

- For projected capacitance sensing
- Keep at 10uA for best performance versus power consumption

- **Sensor mode:**
  - **Self-capacitance**
    - Excitation and measurements are done on the same pin
    - Any pin can be used for self-capacitance measurements
  - **Projected capacitance**
    - Projected channel setup has a very flexible implementation on the IQS269A
    - Any of the 8 channels may be any combination of TX pins and CRX pins
    - Self-capacitance may be selected for one channel and projected capacitance for another, giving more information about a trigger than available on a single sensing mode
  - **Self-inductance**
    - Please contact Azoteq for application guidance or see the inductive sensing application note on the Azoteq website
  - **Mutual inductance**
    - Please contact Azoteq for application guidance or refer to AZD115 inductive sensing application note on the Azoteq website.
  - **HALL**
    - An internal HALL pad offers the ability to detect the HALL effect and make use of the IQS269A's multi direction, multi threshold trigger levels
    - No external connections are required for this mode
    - The proposed CRX connections (CRX0 and CRX6) do not affect choosing CRX0 and CRX6 for other sensing modes.
    - For HALL sensor mode the touch and deep touch thresholds will be defined by the register decimal values in units of counts directly and will thus be independent of LTA value.

Sensing Engine Settings

Full address per channel number								**Item name (offset 0 – 8bits)**								**Item name (offset 1 – 8bits)**								**Data Access**
CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CHx – Byte0								CHx – Byte1								
								Bit 7							Bit 0	Bit 7							Bit 0	
0x8E	0x95	0x9C	0xA3	0xAA	0xB1	0xB8	0xBF	Channel Sensing engine settings 3								Auto Tuning Implementation (ATI) base value target and count target								Read-Write
								Reserved Set '00'		Enable Internal Cap	Reser-ved Set '0'	Reserved Set '0'	Sensing frequency selection (16M/4M) '00' – 4MHz/1MHz '01' – 2MHz/500kHz '10' – 1MHz/250kHz '11' – 500kHz/125kHz		Static fine multipliers (HALL) '0' – Off '1' – On	ATI Base value '00' – 75 '01' – 100 '10' – 150 '11' - 200		ATI Target (x 32)						Read-Write
0x8F	0x96	0x9D	0xA4	0xAB	0xB2	0xB9	0xC0	Channel Multiplier Setting – normal use is read only								Compensation (ATI) – normal use is read only								Read-Write
								Compensation (MSB)		Coarse operating point (ATI)		Fine operating point (ATI)				Compensation (LSB)								Read-Write

- **Enable internal Capacitor:**
  - Add a small internal capacitance (0.5 – 2pF range) to the sensor
- **Sensing frequency:**
  - Select a higher frequency for optimized time and function in some cases
  - Select a lower frequency to reach optimal charge transfers characteristics in capacitive sensing modes containing higher resistance paths and large load capacitors
- **Static fine multipliers (HALL):**
  - Enable for non-charge transfer sensor modes such as HALL and "external"
  - This bit ensures optimal power consumption in these modes and is not critical

Thresholds

								Item name (offset 0 – 8bits)		Item name (offset 1 – 8bits)		Data Access
CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CHx – Byte0		CHx – Byte1		
								Bit 7	Bit 0	Bit 7	Bit 0	
0x90	0x97	0x9E	0xA5	0xAC	0xB3	0xBA	0xC1	Channel Proximity Threshold (4 sample debounce) = 0-255 counts		Channel Touch Threshold = x/256 of LTA value		Read-Write
0x91	0x98	0x9F	0xA6	0xAD	0xB4	0xBB	0xC2	Channel Deep Touch Threshold = x/256 of LTA value		Channel Hysteresis for Deep Touch	Channel Hysteresis for Touch	Read-Write

- **Channel Touch and Deep touch thresholds**
  - The threshold will be calculated as $x/256 \times LTA$
  - **Exception:** Sensor mode configured to Hall will result in touch and deep touch thresholds defined by register decimal values in units of counts directly and will thus be independent of the LTA value.
- **Hysteresis for Touch and Deep touch**
  - The release threshold will be adjusted according to the table below:

Bit setting	Threshold adjustment	Threshold change percentage
"0000"	0/256	0.00%
"0001"	1/256	0.39%
"0010"	3/256	1.17%
"0011"	8/256	3.13%
"0100"	14/256	5.47%
"0101"	21/256	8.20%
"0110"	31/256	12.11%
"0111"	42/256	16.41%
"1000"	55/256	21.48%
"1001"	69/256	27.95%
"1010"	85/256	33.20%
"1011"	103/256	40.23%
"1100"	123/256	48.05%
"1101"	144/256	56.25%
"1110"	167/256	65.23%
"1111"	195/256	75.00%

  - The release threshold will be (Threshold - Hysteresis) * LTA/256

Reference Channel Association & Weight

Full address per channel number								Item name (offset 0 – 8bits)		Item name (offset 1 – 8bits)		Data Access
CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CHx – Byte0		CHx – Byte1		
								Bit 7	Bit 0	Bit 7	Bit 0	
0x92	0x99	0xA0	0xA7	0xAE	0xB5	0xBC	0xC3	Reference channel association (this channel is reference channel for up to 7 other channels – if no bits set, this channel is not a reference channel		Associated sensing channel impact weight (if this channel is associated to reference channel – 0 = no impact, 255 = 200% impact)		Read-Write
								CH7 (bit 7) → CH0 (bit 0)				Read-Write

- See reference channel UI details

Known Issue – TWS Configuration

- If the IC is configured in TWS mode ('D0' config) for special GPIO requirements, then a brown-out reset may cause the settings to default to the '00' config.
- A master device will be able to detect state and re-initialize the 'D0' state
- A power-on reset will also recover the 'D0' state
- Please contact Azoteq for procedures if this state needs to be recovered
- This issue is solved from device version 3 and higher