Keywords: ism transmitter, frac-n, fractional-n, integer-n, synthesizer, pll, channel, spacing, phase noise loop, filter, bandwidth, synthesizer IC, ism, transmitter, rf, rfic, wireless, radio frequency, rf ics, rfics

APPLICATION NOTE 2873

Combine the MAX2902 with an External Frequency Synthesizer

By: Roger Bremer, Strategic Applications Engineer
Nov 21, 2003

Abstract: The MAX2902 ISM transmitter is designed to combine with an external synthesizer IC to form a complete TX path solution. Either a fractional-N or an integer-N synthesizer IC can be utilized depending on system requirements. Understanding how channel step size, phase noise, and PLL lock time differ between the two types of synthesizers is necessary to determine which is more appropriate for a specific application. This note will attempt to illustrate the key differences so that a proper synthesizer selection can be made.

The MAX2900-MAX2904 are single-chip 200mW transmitters designed for use in the 868MHz/915MHz frequency bands. Integrated onto each IC are a baseband PN sequence low-pass filter, transmit modulator, power amplifier, and RF VCO. The MAX2900, MAX2901 and MAX2903 also include a complete synthesizer that allows these parts to operate as complete, stand-alone RF transmitter solutions. The MAX2902 and MAX2904 have been designed to combine with an external synthesizer to allow ultimate flexibility in frequency planning and channel setup.

Click here for an overview of the wireless components used in a typical radio transceiver.

When choosing a synthesizer IC, the first decision that must be made is whether to use an integer-N or fractional-N model. A well designed sigma delta Fractional-N Synthesizer can yield superior performance in terms of phase noise, PLL lock time and comparison spur suppression. However, while the cost of fractional-N synthesizers continues to drop, integer-N synthesizer ICs still offer a less expensive solution. Understanding how performance parameters can be traded will help in making a more informed decision about what synthesizer to use.

Comparison Frequency

One of the main differences between using the MAX2902 with an fractional-N synthesizer versus an integer-N synthesizer is that a higher comparison frequency (F_{COMP}) can be used while maintaining the same, or in many cases a smaller, frequency resolution or step-size (F_{STEP}). In an integer-N synthesizer the step size is the same as the comparison frequency. However, in a fractional-N approach, the step-size is related to the comparison frequency by $F_{STEP} = F_{COMP}/2^{BITS}$, where BITS is the number of fractional bits in the synthesizer.

A higher comparison frequency can significantly reduce the in-loop phase noise of the LO signal being

created. Phase noise is proportional to the main synthesizer divider value (N). By increasing the comparison frequency, a lower value for N is required to achieve the same RF frequency, thus lowering the divider's noise contribution. The decrease in phase noise can then be calculated by

$$\Delta PhaseNoise = 20 * \log(N_2 / N_1)$$

Loop Bandwidth

As the synthesizer's comparison frequency increases, it is possible to use a wider loop bandwidth without causing degradation to the suppression of comparison spurs. The comparison spurs are pushed outward as the comparison frequency increases allowing the 3dB point for the loop filter to also be moved outward while still providing sufficient attenuation to the reference spurs.

The benefit of increasing the loop bandwidth is a shorter lock time. Lock time is inversely proportional to the loop filter's cutoff frequency so increasing the loop bandwidth decreases the time it takes for a PLL to lock. In many applications lock time is a critical parameter and the wide loop bandwidths compatible with fractional-N synthesizers can prove invaluable.

The downside to an increased loop bandwidth is that the phase detector noise is now integrated over a larger bandwidth. Phase noise is constant through the loop filter corner frequency and begins to roll off after that. Thus, as the loop filter corner is pushed farther out, the integrated phase error of the LO signal is increased according to the following equation: ΔIntegrated Noise = 10 x log(F_2/F_1) where F1 and F2 are the narrow and wide loop bandwidths respectively.

A Note on Coupling

The MAX2902 has an on-chip Power Amplifier that puts out up to +23.5dBm, typical. With this amount of power, it is easy for the modulated, RF output signal to couple onto the VCO traces between the MAX2902 and the synthesizer IC. While careful consideration of trace routing and grounding will help to minimize any coupling, layout size constraints can often make it impossible to completely eliminate the effects of coupling. Having an unwanted signal on the VCO line will cause the LO phase noise of the MAX2902 to worsen. The wider that the loop bandwidth is set, the less susceptible the circuit will be to RF coupling since the closed loop will attenuate the coupled noise. As previously mentioned though, a wider loop bandwidth will increase the integrated phase error of the system.

Application Example

Two examples are presented. The first uses an integer-N topology and the second uses a fractional-N. The same synthesizer IC will be used in both its integer and fractional modes to illustrate typical performance of the MAX2902 in a closed loop. The setup parameters are listed below along with the phase noise plots for both configurations. Both arrangements offer viable real world solutions depending on the overall synthesizer requirements.

The fractional-n synthesizer being used has 4 bits, which gives it a modulus 16 fractional component. This allows the comparison frequency to be eight times larger than the integer case while providing a 50 percent smaller achievable step size. If a larger modulus fractional synthesizer were used this difference could be made even greater.

As can be seen from the phase noise plots, the difference in in-band phase noise is (-73.00 - -82.83) = 9.83dB. This is very close to the theoretical difference based on the different N divider values of 10 * log (5856/732) = 9.03dB. Hence the fractional synthesizer has provided an improvement for in-band phase noise. However, when integrated phase noise is calculated the two values converge to -29dBc and -

30dBc for the integer and fractional methods respectively. The wider bandwidth used in the fractional case has removed the initial phase noise advantage but created a PLL lock time improvement of approximately 5X.

Conclusion

The MAX2902 is a highly integrated transmiter IC that can be combined with either an integer-N for a fractional-N synthesizer to form a complete transmitter solution. When choosing what type of synthesizer to mate the MAX2902 with, the necessary performance specifications and tradeoffs must first be evaluated and understood. Phase Noise, lock time, channel spacing, and cost can all varied to find the appropriate synthesizer solution.

Related Parts		
MAX2902	200mW Single-Chip Transmitter ICs for 868MHz/915MHz ISM Bands	Free Samples

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