SLVS528E–JULY 2004–REVISED NOVEMBER 2007

500-mA, 3-MHz SYNCHRONOUS STEP-DOWN CONVERTER IN CHIP SCALE PACKAGING

FEATURES

- **Up to 93% Efficiency at 3-MHz Operation**
- **Up to 500-mA Output Current at V_I = 2.7 V**
- **3-MHz Fixed Frequency Operation**
- ***Best in Class* Load and Line Transient**
- **Complete 1-mm Component Profile Solution**
- **-0.5% / +1.3% PWM DC Voltage Accuracy Over Temperature**
- **35-ns Minimum On-Time**
- **Power-Save Mode Operation at Light Load Currents**
- **Fixed and Adjustable Output Voltage**
- **Only 86-μA Quiescent Current**
- **100% Duty Cycle for Lowest Dropout**
- **Synchronizable *On the Fly* to External Clock Signal**
- **Integrated Active Power-Down Sequencing (TPS6232x only)**
- **Available in a 10-Pin QFN (3 x 3 mm), 8-Pin NanoFree™, and NanoStar™ (CSP) Packaging**

APPLICATIONS

- **Cell Phones, Smart-Phones**
- **WLAN and Bluetooth™ Applications**
- **Micro DC-DC Converter Modules**
- **PDAs, Pocket PCs**
- **USB-Based DSL Modems**
- **Digital Cameras**

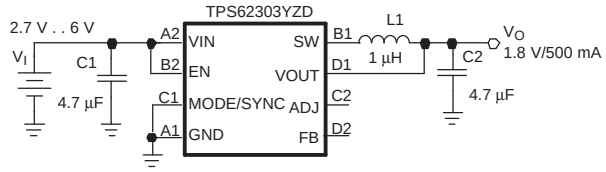


Figure 1. Smallest Solution Size Application (Fixed Output Voltage)

DESCRIPTION

The TPS623xx device is a high-frequency synchronous step-down dc-dc converter optimized for battery-powered portable applications. Intended for low-power applications, the TPS623xx supports up to 500-mA load current and allows the use of tiny, low cost chip inductor and capacitors.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Li-Ion battery or by 3-cell NiMH/NiCd batteries. With an output voltage range from 5.4 V down to 0.6 V, the device supports the low-voltage TMS320™ DSP family, processors in smart-phones, PDAs as well as notebooks, and handheld computers.

The TPS62300 operates at 3-MHz fixed switching frequency and enters the power-save mode operation at light load currents to maintain high efficiency over the entire load current range. For low noise applications, the device can be forced into fixed frequency PWM mode by pulling the MODE/SYNC pin high. The device can also be synchronized to an external clock signal in the range of 3 MHz. In the shutdown mode, the current consumption is reduced to less than 1 μA.

The TPS623xx is available in a 10-pin leadless package (3 x 3 mm QFN) and an 8-pin chip-scale package (CSP).

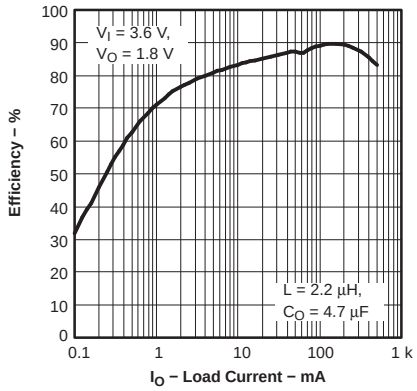


Figure 2. Efficiency vs Load Current

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PART NUMBER	OUTPUT VOLTAGE	UNDERVOLTAGE LOCKOUT	PACKAGE	ORDERING(1)(2)	PACKAGE MARKING
-40°C to 85°C	TPS62300	Adjustable	2.4 V	QFN-10	TPS62300DRC	AMN
			2.4 V	CSP-8	TPS62300YZD	N/A
	TPS62301	1.5 V	2.4 V	QFN-10	TPS62301DRC	AMO
			2.4 V	CSP-8	TPS62301YZD	N/A
	TPS62302	1.6 V	2.4 V	QFN-10	TPS62302DRC	AMQ
			2.4 V	CSP-8	TPS62302YZD	N/A
	TPS62303	1.8 V	2.4 V	QFN-10	TPS62303DRC	AMR
			2.4 V	CSP-8	TPS62303YZD	N/A
	TPS62304	1.2 V	2.4 V	QFN-10	TPS62304DRC	AMS
			2.4 V	CSP-8	TPS62304YZD	N/A
	TPS62305	1.875 V	2.4 V	QFN-10	TPS62305DRC	ANU
			2.4 V	CSP-8	TPS62305YZD	N/A
	TPS62311	1.5 V	2 V	CSP-8	TPS62311YZD	N/A
	TPS62313	1.8 V	2 V	CSP-8	TPS62313YZD	N/A
	TPS62315	1.875 V	2 V	CSP-8	TPS62315YZ	N/A
	TPS62320	Adjustable	2.4 V	QFN-10	TPS62320DRC	AMX
			2.4 V	CSP-8	TPS62320YZD	N/A
			2.4 V	CSP-8	TPS62320YED	N/A
	TPS62321	1.5 V	2.4 V	QFN-10	TPS62321DRC	AMY
			2.4 V	CSP-8	TPS62321YZD	N/A
			2.4 V	CSP-8	TPS62321YED	N/A

(1) The YZD, YED and YZ packages are available in tape and reel. Add a R suffix (e.g. TPS62300YxDR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS62300YxDT) to order quantities of 250 parts. The DRC package is available in tape and reel. Add a R suffix (e.g. TPS62300DRCR) to order quantities of 3000 parts.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
V_I	Voltage at VIN, AVIN(2)	-0.3 V to 7 V
	Voltage at SW (2)	-0.3 V to 7 V
	Voltage at FB, ADJ	-0.3 V to 3.6 V
	Voltage at EN, MODE/SYNC (2)	-0.3 V to V_I + 0.3 V
	Voltage at VOUT(2)	0.3 V to 5.4 V
I_O	Continuous output current	500 mA
	Power dissipation	Internally limited
T_A	Operating temperature range	-40°C to 85°C
T_J (max)	Maximum operating junction temperature	150°C
T_{stg}	Storage temperature range	-65°C to 150°C
ESD rating(3)	Human body model at AVIN, FB, ADJ, EN, MODE_SYNC, VOUT	2 kV
	Human body model at VIN, SW	1 kV
	Charge device model	1.5 kV

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$(2)	POWER RATING FOR $T_A \leq 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$
DRC	49°C/W	2050 mW	21 mW/°C
YZD	250°C/W	400 mW	4 mW/°C
YED	250°C/W	400 mW	4 mW/°C
YZ	250°C/W	400 mW	4 mW/°C

(1) Maximum power dissipation is a function of $T_J(max)$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_J(max)-T_A] / \theta_{JA}$
(2) This thermal data is measured with low-K board (1 layer board according to JESD51-7 JEDEC standard).

ELECTRICAL CHARACTERISTICS

V_I = 3.6 V, V_O = 1.6 V, EN = V_I, MODE/SYNC = GND, L = 1 µH, C_O = 10 µF, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage range			2.7		6	V
I_Q	Operating quiescent current	TPS6230x TPS6232x	I_O = 0 mA. PFM mode enabled, device not switching		86	105	µA
		TPS6231x	I_O = 0 mA. PFM mode enabled, device not switching		86	120	µA
		TPS6230x TPS6231x TPS6232x	I_O = 0 mA. Switching with no load (MODE/SYNC = VIN)		3.6		mA
$I_{(SD)}$	Shutdown current		EN = GND		0.1	1	µA
UVLO	Undervoltage lockout threshold	TPS6230x TPS6232x			2.40	2.55	V
		TPS6231x			2.00	2.20	V
ENABLE, MODE/SYNC							
$V_{(EN)}$	EN high-level input voltage			1.2			V
$V_{(MODE/SYNC)}$	MODE/SYNC high-level input voltage			1.3			V
$V_{(EN)}$, $V_{(MODE/SYNC)}$	EN, MODE/SYNC low-level input voltage					0.4	V
$I_{(EN)}$, $I_{(MODE/SYNC)}$	EN, MODE/SYNC input leakage current		EN, MODE/SYNC = GND or VIN		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance	TPS6230x TPS6231x TPS6232x	$V_I = V_{(GS)}$ = 3.6 V		420	750	mΩ
			$V_I = V_{(GS)}$ = 2.8 V		520	1000	mΩ
I_{lkg}	P-channel leakage current, PMOS		$V_{(DS)}$ = 6 V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance		$V_I = V_{(GS)}$ = 3.6 V		330	750	mΩ
			$V_I = V_{(GS)}$ = 2.8 V		400	1000	mΩ
$R_{(DIS)}$	Discharge resistor for power-down sequence (TPS6232x only)				30	50	Ω
I_{lkg}	N-channel leakage current, NMOS		$V_{(DS)}$ = 6 V			1	µA
	P-MOS current limit		2.7 V ≤ V_I ≤ 6 V	670	780	890	mA
	N-MOS current limit - sourcing		2.7 V ≤ V_I ≤ 6 V	550	720	890	mA
	N-MOS current limit - sinking		2.7 V ≤ V_I ≤ 6 V	–460	–600	–740	mA
	Input current limit under short-circuit conditions		V_O = 0 V		390		mA
	Thermal shutdown				150		°C
	Thermal shutdown hysteresis				20		°C

ELECTRICAL CHARACTERISTICS (continued)

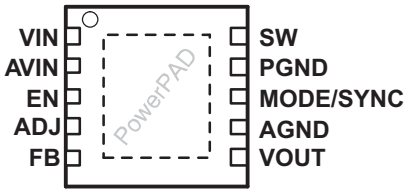
V_I = 3.6 V, V_O = 1.6 V, EN = V_I, MODE/SYNC = GND, L = 1 µH, C_O = 10 µF, T_A = -40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
OSCILLATOR								
f_{SW}	Oscillator frequency				2.65	3	3.35	MHz
$f_{(SYNC)}$	Synchronization range				2.65		3.35	MHz
	Duty cycle of external clock signal				20%		80%	
OUTPUT								
V_O	Adjustable output voltage range	TPS62300 TPS62320			0.6		5.4	V
$V_{(FB)}$	Regulated feedback voltage	TPS62300 TPS62320				0.4		V
$A_{(PT)}$	DC power train amplification ($V_O/V_{(ADJ)}$)				1.496	1.5	1.504	
$t_{on(MIN)}$	Minimum on-time (P-channel MOSFET)					35		ns
	Resistance into VOUT sense pin				700	1000		kΩ
	Resistance into ADJ pin		$V_{(FB)}$ > 0.4 V		700	1000	1300	kΩ
$I_{(FB)}$	Feedback input bias current	TPS62300 TPS62320	$V_{(FB)}$ = 0.4 V			1		nA
V_O	Adjustable output voltage(1)	TPS62300 TPS62320	2.7 V ≤ V_I ≤ 6 V, 0 mA ≤ $I_{O(DC)}$ ≤ 500 mA PFM/PWM mode operation		–2%		+2%	
	Fixed output voltage	TPS6230x TPS62311 TPS62313 TPS6232x			–2%		+2%	
		TPS62304			-2%		+2.5%	
		TPS62305 TPS62315			–2%		+2.7%	
	Adjustable output voltage dc accuracy(1)	TPS62300 TPS62320	PWM mode operation, V_I = 3.6 V, No Load	T_A = 25°C	–0.5%		+1.3%	
				–40°C ≤ T_A ≤ 85°C	–0.5%		+1.3%	
	Fixed output voltage dc accuracy	TPS6230x TPS62311 TPS62313 TPS6232x		T_A = 25°C	–0.5%		+1.3%	
				–40°C ≤ T_A ≤ 85°C	–0.5%		+1.3%	
		TPS62304		T_A = 25°C	-0.5%		+1.8%	
				–40°C ≤ T_A ≤ 85°C	-0.5%		+1.8%	
		TPS62305 TPS62315		T_A = 25°C	–0.3%		+1.7%	
				–40°C ≤ T_A ≤ 85°C	–0.5%		+2%	
	DC output voltage load regulation		I_O = 0 mA to 500 mA, MODE/SYNC = V_I			–0.001	–0.002	%/mA
	DC output voltage load regulation (power train in direct drive mode)		$V_{(ADJ)}$ externally forced to 1.067 V, I_O = 0 mA to 500 mA, MODE/SYNC = V_I			–0.0003	–0.0006	%/mA
	DC output voltage line regulation		V_I = V_O + 0.5 V (min 2.7 V) to 6 V, I_O = 100 mA, MODE/SYNC = V_I			0.11	0.2	%/V
	DC output voltage line regulation (power train in direct drive mode)		$V_{(ADJ)}$ externally forced to 1.067 V, V_I = V_O + 0.5 V (min 2.7 V) to 6 V I_O = 100 mA, MODE/SYNC = V_I			0.035	0.1	%/V
	Integrator slew rate				100	150	200	µV/µs
ΔV_O	Power-save mode ripple voltage		I_O = 1 mA, MODE/SYNC = GND			0.025 V_O		V_{P-P}
	Start-up time		I_O = 200 mA, Time from active EN to V_O			250		µs
I_{lkg}	Leakage current into SW pin		V_I > V_O, 0 V ≤ $V_{(SW)}$ ≤ VIN, EN = GND			0.1	1	µA
	Reverse leakage current into SW pin		V_I = open, $V_{(SW)}$ = 6 V, EN = GND			0.1	1	

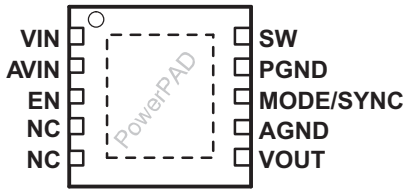
(1) Output voltage specification for the adjustable version does not include tolerance of external voltage programming resistors.

PIN ASSIGNMENTS

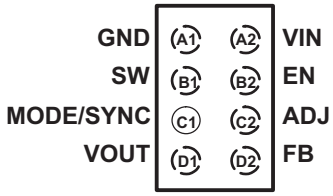
TPS62300, TPS62320
QFN-10
(TOP VIEW)



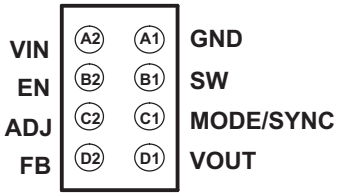
TPS6230x, TPS6232x
FIXED OUTPUT VOLTAGE (QFN-10)
(TOP VIEW)



TPS6230x, TPS6231x, TPS6232x
CSP-8
(TOP VIEW)



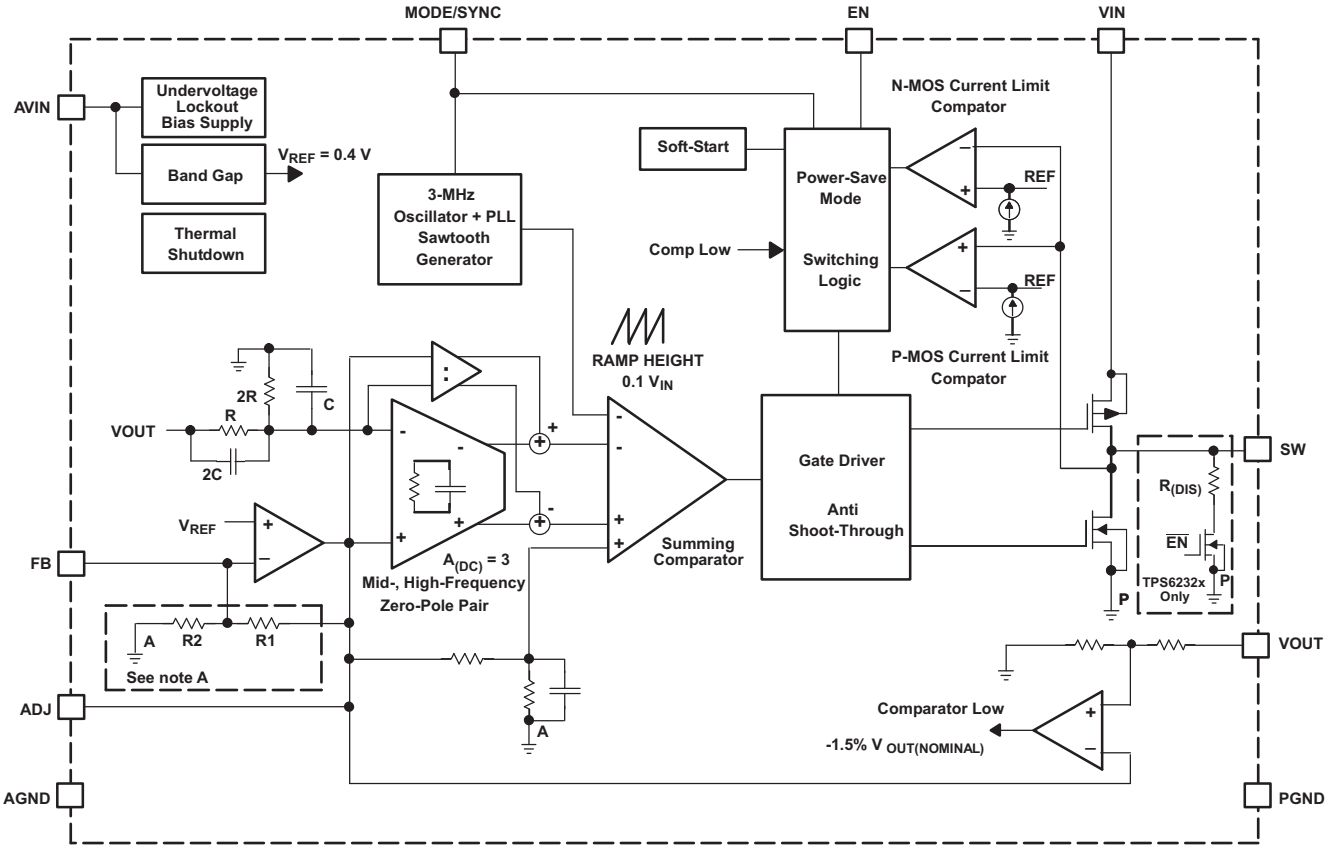
TPS6230x, TPS6231x, TPS6232x
CSP-8
(BOTTOM VIEW)



TERMINAL FUNCTIONS

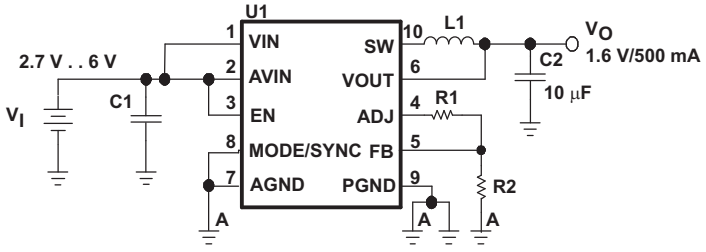
TERMINAL			I/O	DESCRIPTION
NAME	NO. QFN	NO. CSP		
VIN	1	A2	I	Supply voltage for output power stage.
AVIN	2		I	This is the input voltage pin of the device. Connect directly to the input bypass capacitor.
EN	3	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
ADJ	4	C2	I/O	This is the internal reference voltage used to regulate V_O. This pin is not connected on fixed output voltage version of TPS6230xDRC and TPS6232xDRC. Do not connect ADJ pin on fixed output voltage version of TPS6230xYZD, TPS6231xYZD, TPS6231xYZ and TPS6232xYxD. On TPS62300 and TPS62320, this pin can also be used as an external control input. The output voltage is 1.5x the applied voltage at ADJ.
FB	5	D2	I	This is the feedback pin of the device. For the adjustable version, an external resistor divider is connected to this pin. The internal voltage divider is disabled for the adjustable version. This pin is not connected on fixed output voltage version of TPS6230xDRC and TPS6232xDRC. Do not connect the FB pin on the fixed output voltage version of TPS6230xYZD, TPS6231xYZD, TPS6231xYZ and TPS6232xYxD.
VOUT	6	D1	I	Output feedback sense input. Connect VOUT to the converter's output.
AGND	7			Analog ground. Connect to PGND via the PowerPAD™ underneath IC.
MODE/SYNC	8	C1	I	Input for synchronization to external clock signal. This pin must not be left floating and must be terminated. Synchronizes the converter switching frequency to an external clock signal MODE/SYNC = LOW (GND): The device is operating in fixed frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE/SYNC = HIGH (VIN): Low-noise mode enabled, fixed frequency PWM operation forced.
PGND	9	A1		Power ground.
SW	10	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
PowerPAD™			N/A	Internally connected to PGND.

FUNCTIONAL BLOCK DIAGRAM



NOTE A: For the adjustable versions (TPS62300 and TPS62320) the internal feedback divider is disabled.

PARAMETER MEASUREMENT INFORMATION



List of Components:
U1 = TPS6230x
L1 = FDK MIPW3226 Series
C1, C2 = X5R/X7R

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4, 5, 6
		vs Input voltage	7
	Line transient response		8
	Load transient response		9, 10, 11, 12, 13, 14, 15, 16
V_O	DC output voltage	vs Load current	17
V_{FB}	Regulated feedback voltage	vs Temperature	18
I_Q	No load quiescent current	vs Input voltage	19
f_s	Switching frequency	vs Temperature	20
	Duty cycle jitter		21
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	22
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	23
	PWM operation		24
	Power-save mode operation		25
	Dynamic voltage management		26, 27
	Start-up		28, 29
	Power down (TPS6232x)		30

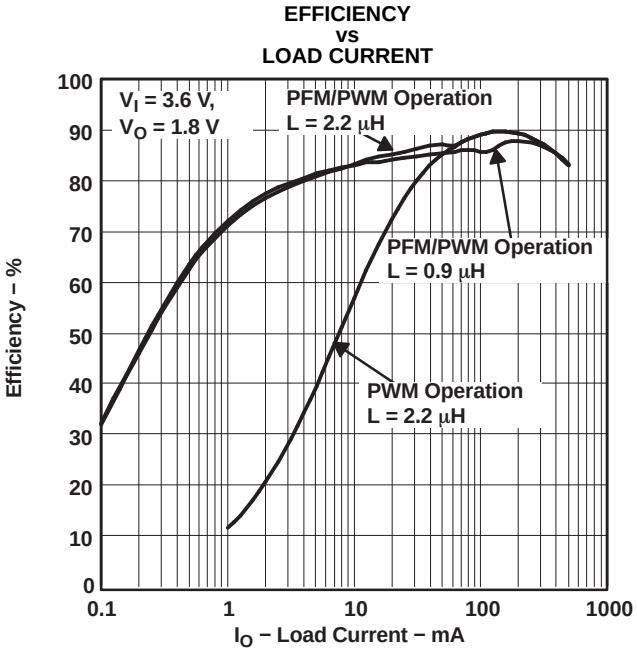


Figure 3.

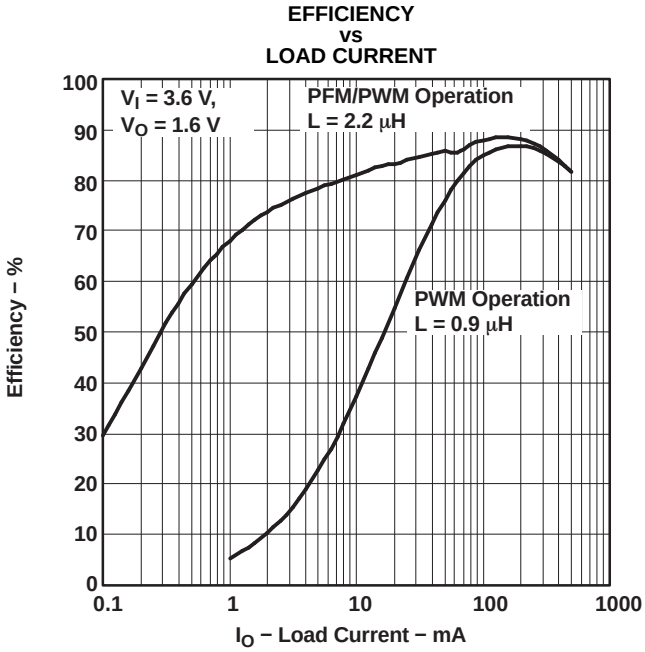


Figure 4.

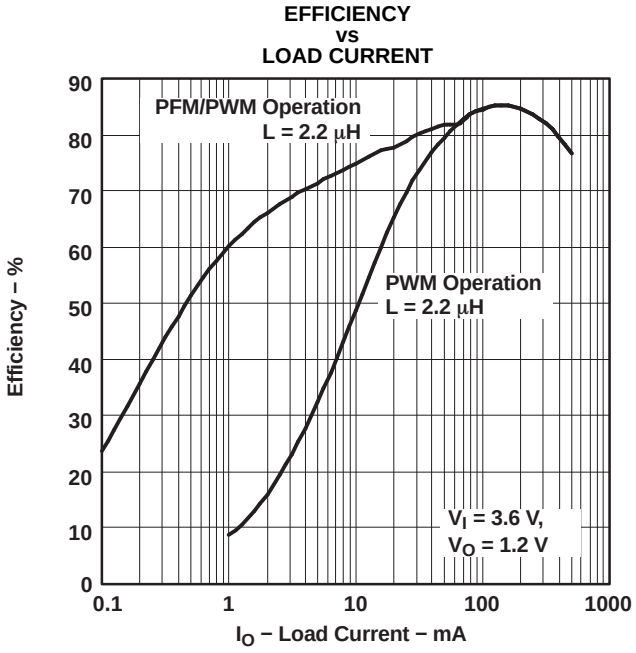
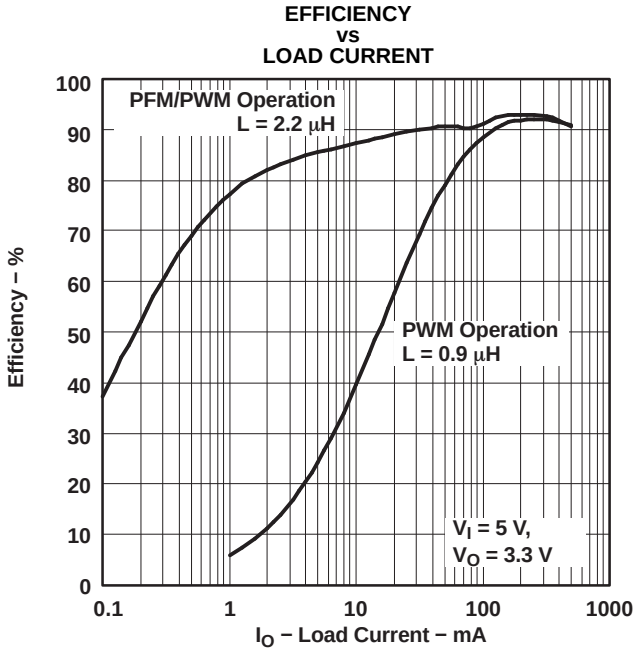


Figure 5.



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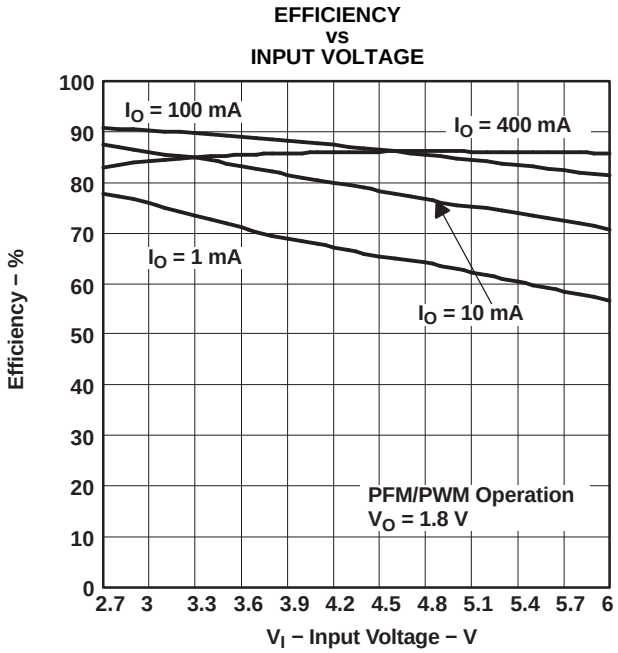

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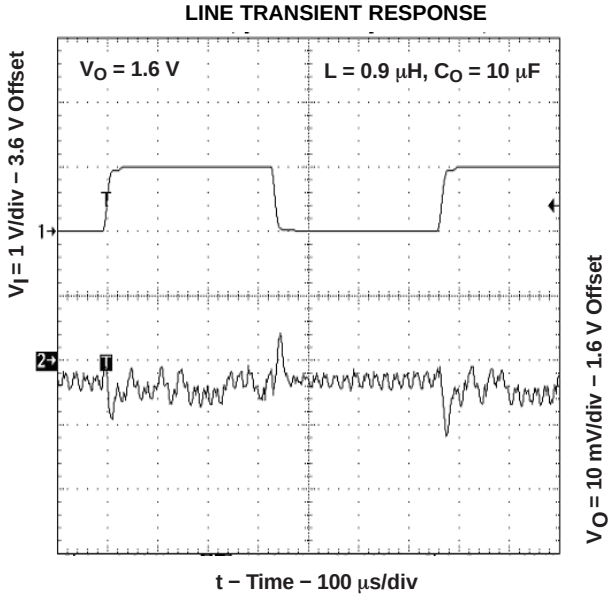


Figure 8.

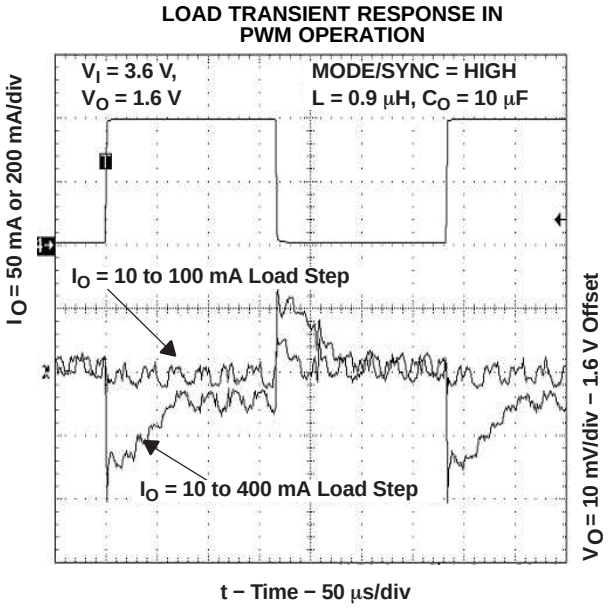


Figure 9.

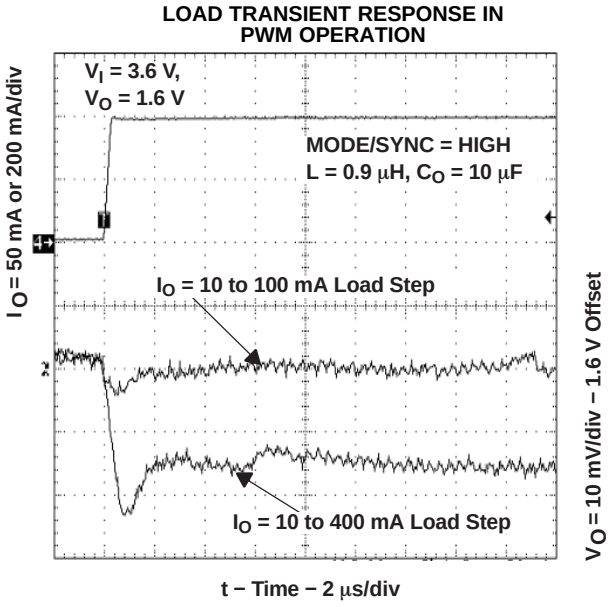


Figure 10.

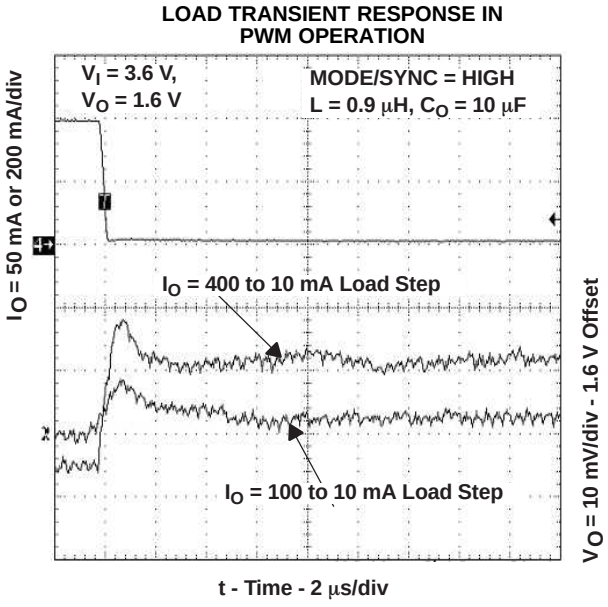


Figure 11.

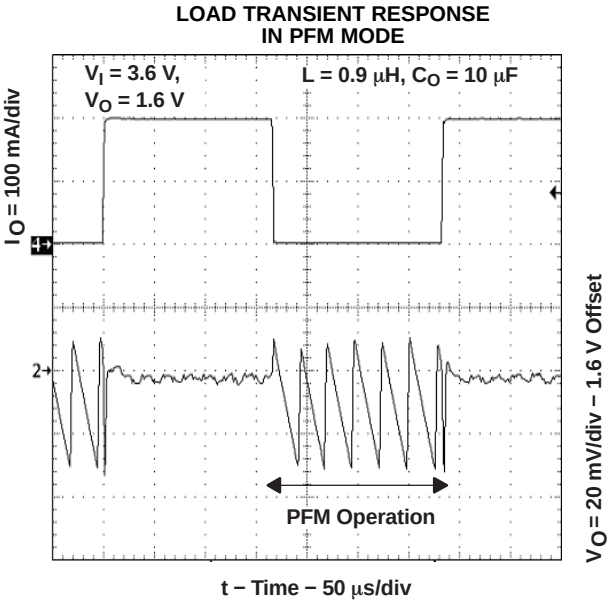


Figure 12.

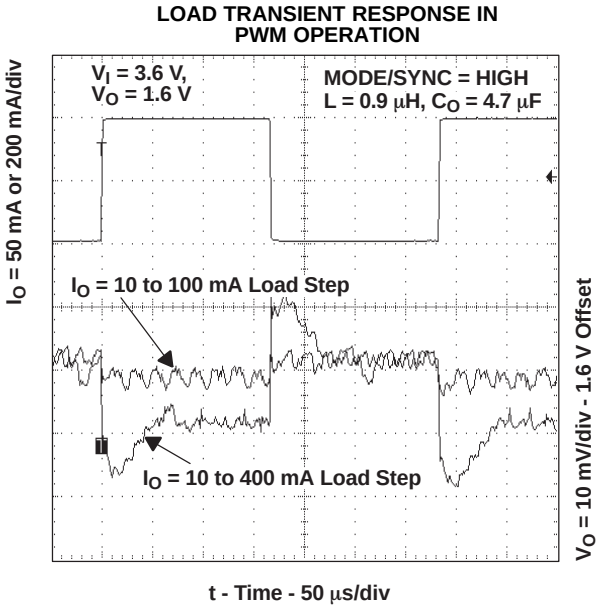
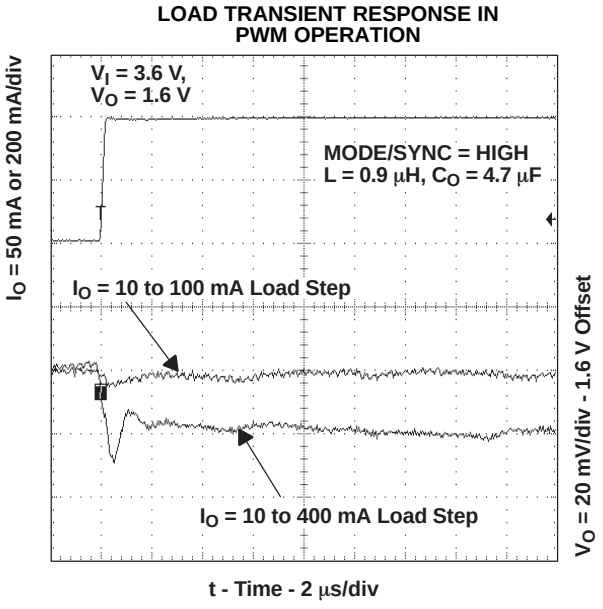


Figure 13.



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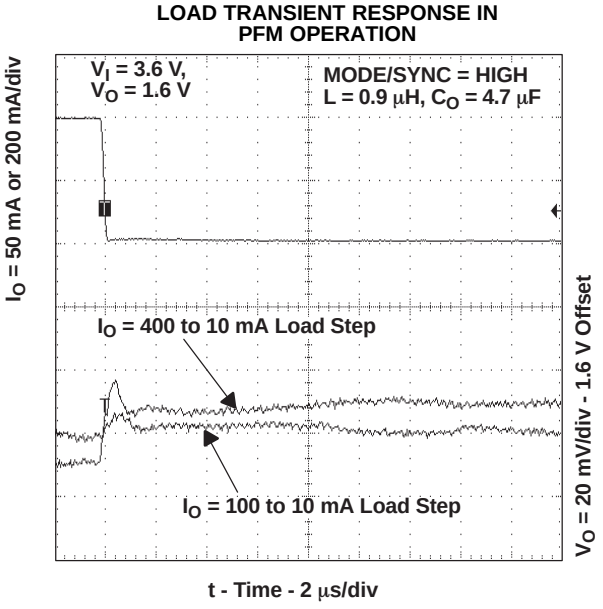
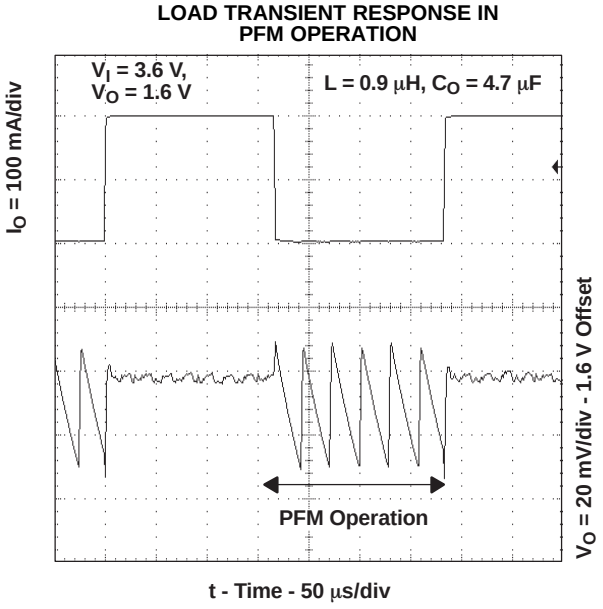


Figure 15.



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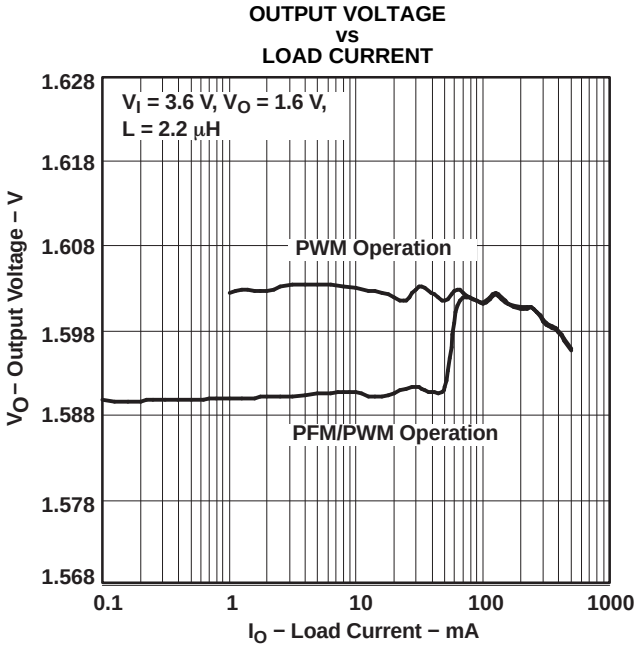

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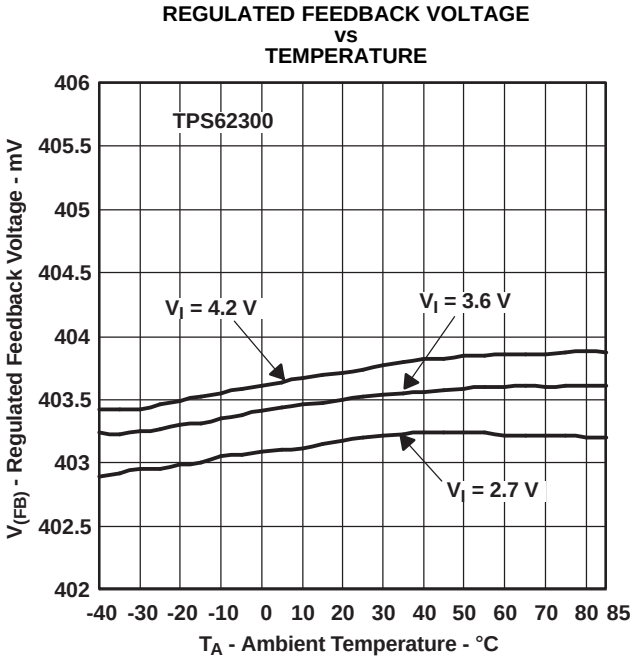

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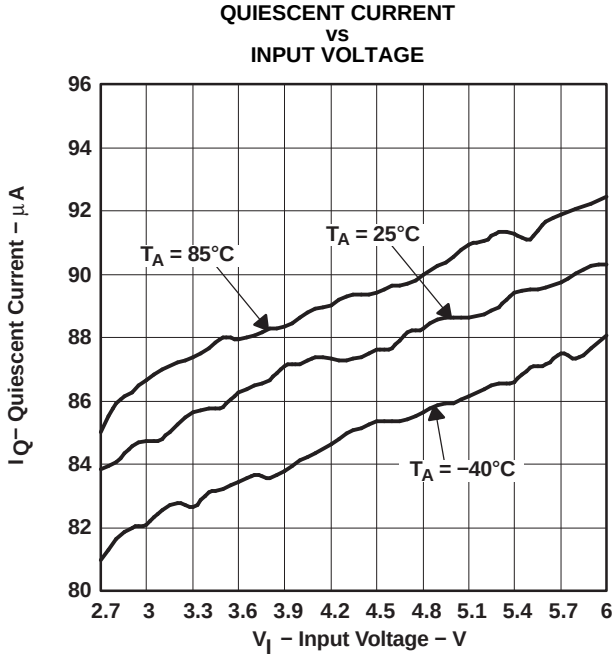

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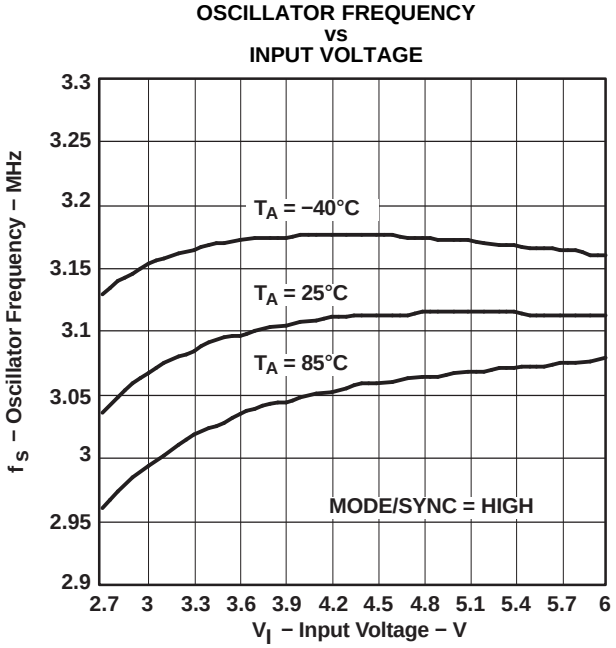


Figure 20.

DUTY CYCLE JITTER

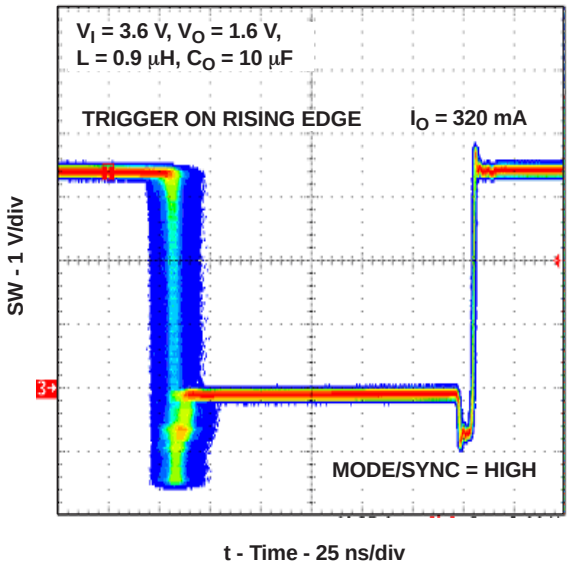


Figure 21.

P-CHANNEL $r_{DS(ON)}$ vs INPUT VOLTAGE

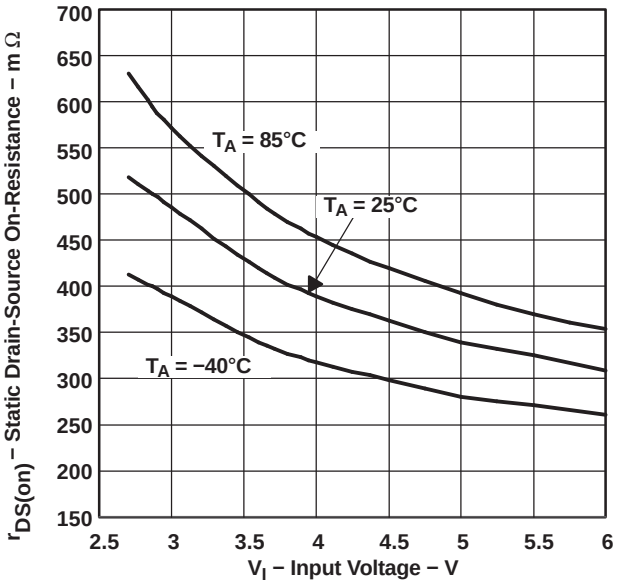


Figure 22.

N-CHANNEL $r_{DS(ON)}$ vs INPUT VOLTAGE

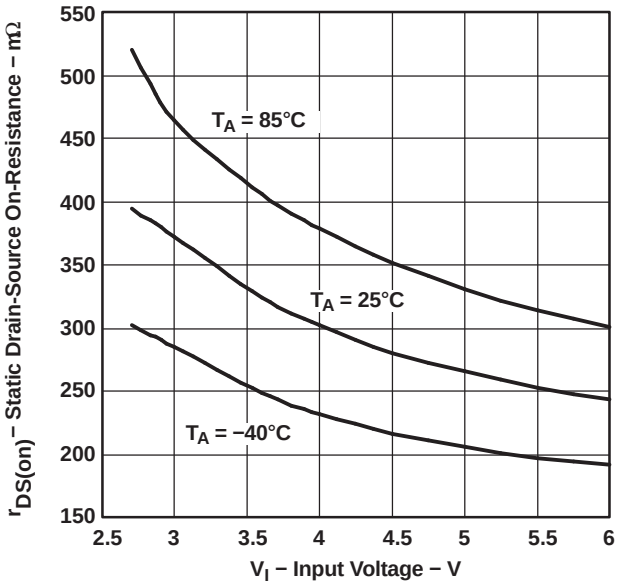


Figure 23.

PWM OPERATION

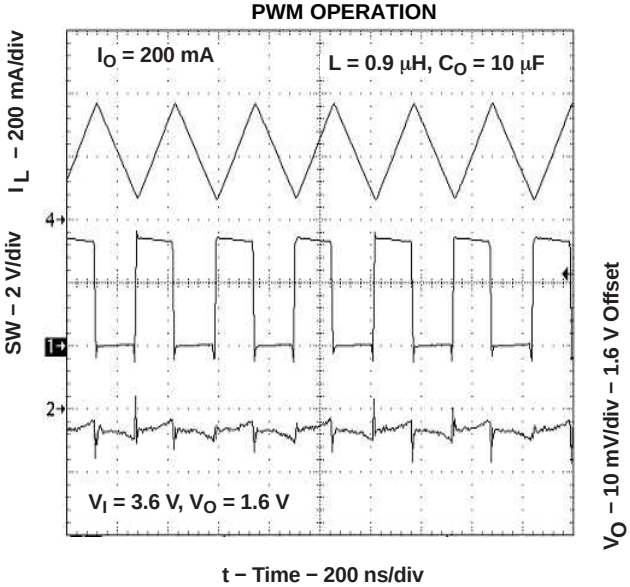


Figure 24.

POWER-SAVE MODE OPERATION

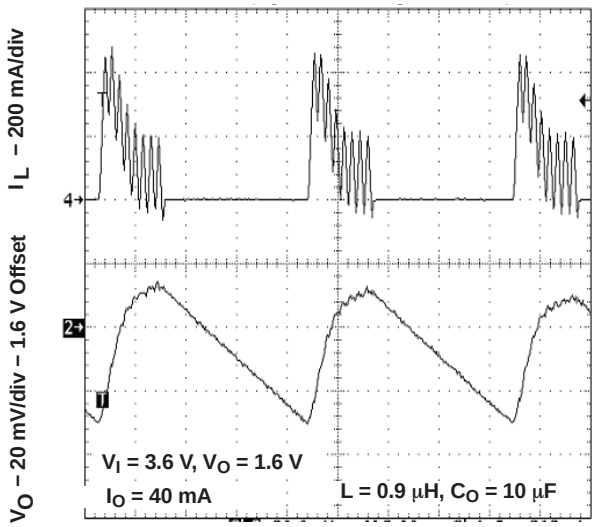


Figure 25.

DYNAMIC VOLTAGE MANAGEMENT

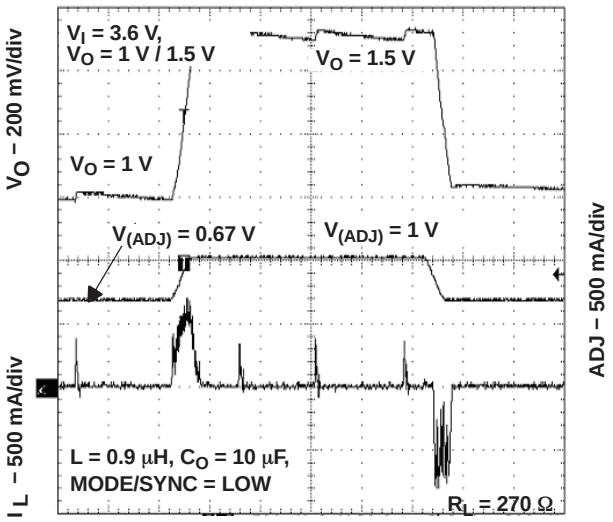


Figure 26.

DYNAMIC VOLTAGE MANAGEMENT

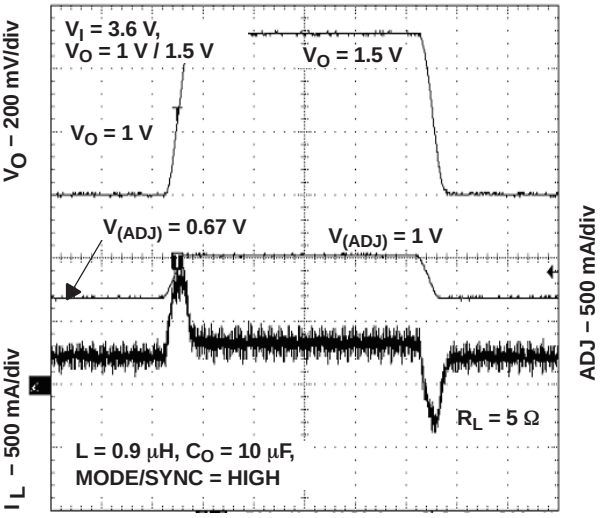


Figure 27.

START-UP

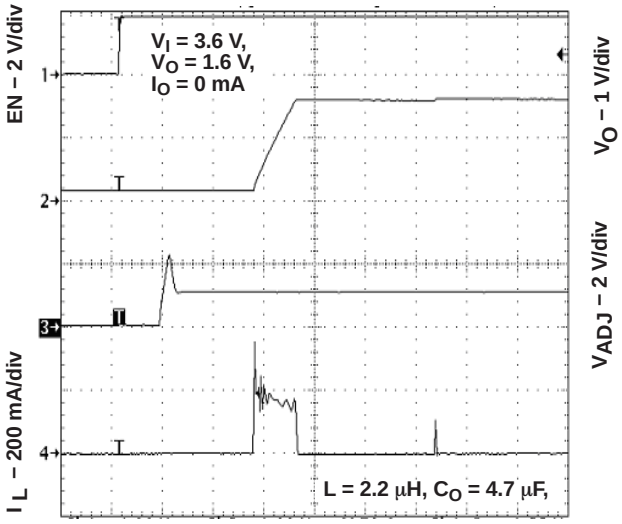


Figure 28.

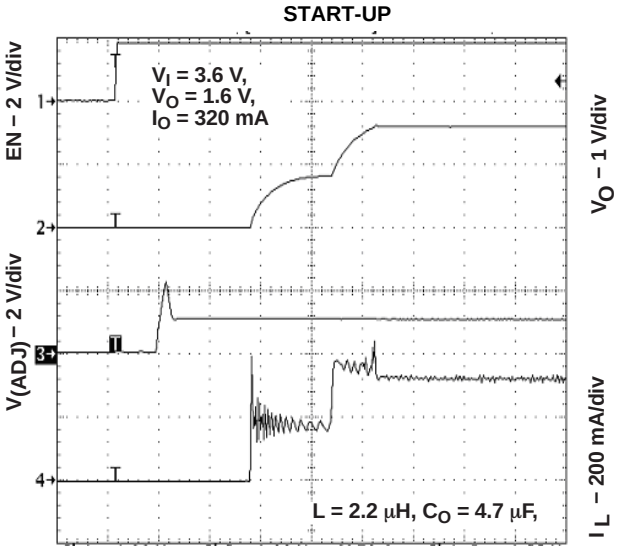


Figure 29.

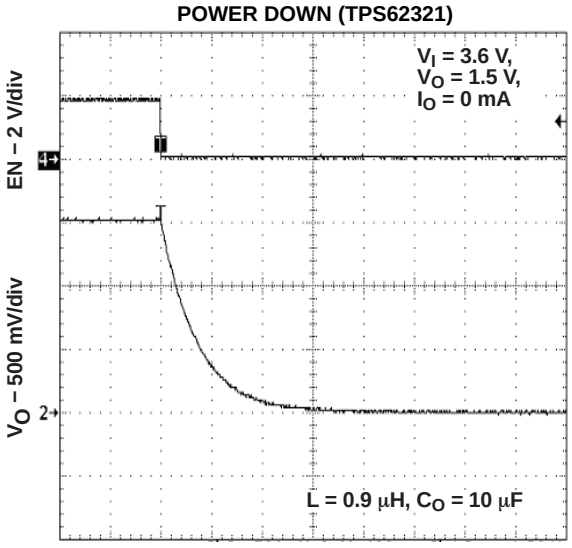


Figure 30.

DETAILED DESCRIPTION

OPERATION

The TPS6230x, TPS6231x, and TPS6232x are synchronous step-down converters typically operating with a 3-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter operates in power-save mode with pulse frequency modulation (PFM). The operating frequency is set to 3 MHz and can be synchronized *on-the-fly* to an external oscillator.

During PWM operation, the converter uses a unique fast response, voltage mode, controller scheme with input voltage feed-forward. This achieves *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch.

The device integrates two current limits, one in the P-channel MOSFET and another one in the N-channel MOSFET. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. When the current in the N-channel MOSFET is above the N-MOS current limit threshold, the N-channel MOSFET remains on until the current drops below its current limit. The current limit in the N-channel MOSFET is important for small duty-cycle operation when the current in the inductor does not decrease because of the P-channel MOSFET current limit delay, or because of start-up conditions where the output voltage is low.

POWER-SAVE MODE

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized, and the device runs with a minimum quiescent current and maintaining high efficiency.

In power-save mode, the converter only operates when the output voltage trips below a set threshold voltage (-1.5% $V_{O(NOMINAL)}$). It ramps up the output voltage with several pulses and goes into power-save mode once the output voltage exceeds the nominal output voltage. As a consequence, the average output voltage is slightly lower than its nominal value in the power-save mode operation.

The output current at which the PFM/PWM transition occurs is approximated by Equation 1:

$$I_{PFM/PWM} = \frac{V_O}{V_I} \times \frac{V_I - V_O}{2 \times L \times f_{SW}} \quad (1)$$

- $I_{PFM/PWM}$: output current at which PFM/PWM transition occurs
- f_{SW} : switching frequency (3-MHz typical)
- L : inductor value

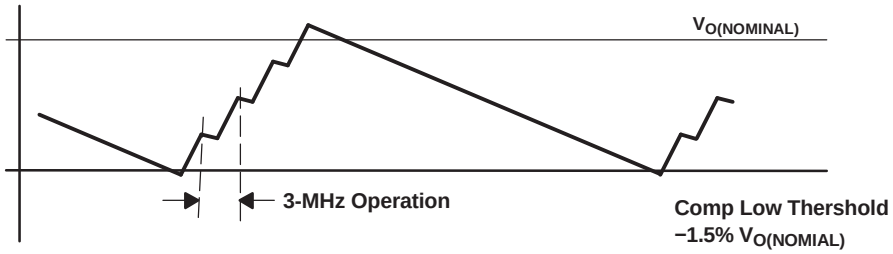


Figure 31. Power-Save Mode Threshold

MODE SELECTION AND FREQUENCY SYNCHRONIZATION

The MODE/SYNC pin is a multipurpose pin which allows mode selection and frequency synchronization. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE/SYNC pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter operates with a fixed frequency that allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads. For additional flexibility, it is possible to switch from power-save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

The TPS6230x, TPS6231x, and TPS6232x can also be synchronized to an external 3-MHz clock signal by the MODE/SYNC pin. During synchronization, the mode is set to fixed-frequency operation and the P-channel MOSFET turnon is synchronized to the falling edge of the external clock. This creates the ability for multiple converters to be connected together in a master-slave configuration for frequency matching of the converters (see the application section for more details, Figure 37).

SOFT START

The TPS6230x, TPS6231x, and TPS6232x have an internal soft-start circuit that limits the inrush current during start-up. This prevents possible input voltage drops when a battery or a high-impedance power source is connected to the input of the converter. The soft start is implemented as a digital circuit increasing the switch current in steps of typically 195 mA, 390 mA, 585 mA, and the typical switch current limit of 780 mA.

The current limit transitions to the next step every 256 clocks (≈88µs). To be able to switch from 390 mA to 585 mA current limit step, the output voltage needs to be higher than 0.5 x $V_{O(NOM)}$, otherwise, the parts continues to operate at the 390-mA current limit. This mechanism is used to limit the output current under short-circuit conditions. Therefore, the start-up time mainly depends on the output capacitor and load current.

LOW-DROPOUT OPERATION 100% DUTY CYCLE

In 100% duty cycle mode, the TPS6230x, TPS6231x, and TPS6232x offer a low input-to-output voltage difference. In this mode, the P-channel MOSFET is constantly turned on. This is particularly useful in battery-powered applications to achieve the longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain regulation, depending on the load current and output voltage, can be calculated as:

- $V_{I(MIN)} = V_{O(MAX)} + I_{O(MAX)} \times (r_{DS(on)\ MAX} + R_L)$
- $I_{O(MAX)}$: Maximum output current
- $r_{DS(on)\ MAX}$: Maximum P-channel switch $r_{DS(on)}$
- R_L : DC resistance of the inductor
- $V_{O(MAX)}$: nominal output voltage plus maximum output voltage tolerance

ENABLE

The device starts operation when EN is set high and starts up with the soft start as previously described.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.1 μA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off. When an output voltage is present during shutdown mode, which can be caused by an external voltage source or super capacitor, the reverse leakage is specified under electrical characteristics. For proper operation, the EN pin must be terminated and must not be left floating.

In addition, the TPS6232x devices integrate a resistor, typically 35 Ω, to actively discharge the output capacitor when the device turns off. The required time to discharge the output capacitor at V_O depends on load current.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions.

The TPS6231x devices have a UVLO threshold set to 2 V (typical). Fully functional operation is permitted down to 2.4 V input voltage. EN is set low for input voltages lower than 2.4 V to avoid the possibility of misoperation.

TPS6231x devices are to be considered where the user requires direct control of the turn-off sequence as part of a larger power management system.

SHORT-CIRCUIT PROTECTION

As soon as the output voltage falls below 50% of the nominal output voltage, the converter current limit is reduced by 50% of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds 50% of the nominal output voltage. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 150°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature falls below typically 130°C again.

APPLICATION INFORMATION

ADJUSTABLE OUTPUT VOLTAGE

When the adjustable output voltage versions, TPS62300 or TPS62320, are used, the output voltage is set by the external resistor divider (see Figure 32).

The output voltage is calculated as:

$$V_O = 1.5 \times V_{ref} \times \left(1 + \frac{R1}{R2}\right) \text{ with an internal reference voltage } V_{ref} \text{ typical } = 0.4\ V \quad (2)$$

To keep the operating quiescent current to a minimum, it is recommended that R2 be set in the range of 75 kΩ to 130 kΩ. Route the FB line away from noise sources, such as the inductor or the SW line.

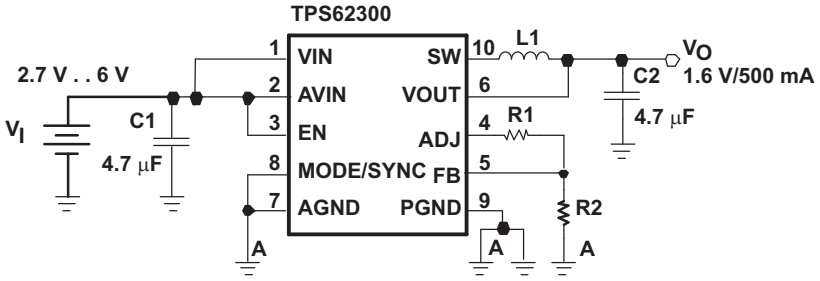


Figure 32. Adjustable Output Voltage Version

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

The TPS6230x, TPS6231x, and TPS6232x series of step-down converters have internal loop compensation. Therefore, the external L-C filter must be selected to work with the internal compensation.

The device has been designed to operate with inductance values between a minimum of 0.7 µH and maximum of 6.2 µH. The internal compensation is optimized to operate with an output filter of L = 1 µH and C_O = 10 µF. Such an output filter has its corner frequency at:

$$f_c = \frac{1}{2\pi\sqrt{L \times C_O}} = \frac{1}{2\pi\sqrt{1\ \mu H \times 10\ \mu F}} = 50.3\ kHz \quad (3)$$

Operation with a higher corner frequency (e.g., L = 1 µH, C_O = 4.7 µF) is possible. However, it is recommended the loop stability be checked in detail. Selecting a larger output capacitor value (e.g., 22 µF) is less critical because the corner frequency moves to lower frequencies with fewer stability problems. The possible output filter combinations are listed in Table 1.

Regardless of the inductance value, operation is recommended with 10-µF output capacitor in applications with high-load transients (e.g., ≥ 1600 mA/µs).

Table 1. Output Filter Combinations

INDUCTANCE (L)	OUTPUT CAPACITANCE (C_O)
1 µH	≥ 4.7 µF (ceramic capacitor)
2.2 µH	≥ 2.2 µF (ceramic capacitor)

The inductor value also has an impact on the pulse skipping operation. The transition into power-save mode begins when the valley inductor current goes below a level set internally. Lower inductor values result in higher ripple current which occurs at lower load currents. This results in a dip in efficiency at light load operations.

INDUCTOR SELECTION

Even though the inductor does not influence the operating frequency, the inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2} \tag{4}$$

with: f_{SW} = switching frequency (3 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current

Normally, it is advisable to operate with a ripple of less than 30% of the average output current. Accepting larger values of ripple current allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

The total losses of the coil consist of both the losses in the DC resistance ($R_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6230x, TPS6231x, and TPS6232x converters.

Table 2. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
FDK	MIPW3226	3.2 x 2.6 x 1 = 8.32 mm^3
	MIPSA2520	2.5 x 2.0 x 1.2 = 6 mm^3
Murata	LQM2HP	2.5 x 2.0 x 1.2 = 6 mm^3
Taiyo Yuden	LQ CB2016	2 x 1.6 x 1.6 = 5.12 mm^3
	LQ CB2012	2 x 1.2 x 1.2 = 2.88 mm^3
	LQ CBL2012	2 x 1.2 x 1 = 2.40 mm^3
TDK	VLF3010AT	2.8 x 2.6 x 1 = 7.28 mm^3
Coilcraft	LPS3010	3.3 x 3.3 x 1 = 10.89 mm^3
JFE	32R1560	3.2 x 2.5 x 0.6 = 4.8 mm^3

OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS6230x, TPS6231x, and TPS6232x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \times \left(\frac{1}{8 \times C_O \times f_{SW}} + ESR \right), \text{maximum for high } V_I \tag{5}$$

At light loads, the device operates in power-save mode and the output voltage ripple is independent of the output capacitor value. The output voltage ripple is set by the internal comparator thresholds and propagation delays. The typical output voltage ripple is 1.5% of the nominal output voltage V_O.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2-µF or 4.7-µF capacitor is sufficient.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

PROGRAMMING THE OUTPUT VOLTAGE WITH A DAC

On TPS62300 and TPS62320 devices, the output voltage can be dynamically programmed to any voltage between 0.6 V and V_I (or 5.4 V whichever is lower) with an external DAC driving the ADJ and FB pins (see Figure 33). The output voltage is then equal to $A_{(PT)}$ x $V_{(DAC)}$ with a *Power Train* amplification $A_{(PT)}$ typical = 1.5.

When the output voltage is driven low, the converter reduces its output quickly in forced PWM mode, boosting the output energy back to the input. If the input is not connected to a low-impedance source capable of absorbing the energy, the input voltage can rise above the absolute maximum voltage of the part and get damaged. The faster V_O is commanded low, the higher is the voltage spike at the input.

For best results, ramp the ADJ/FB signal as slow as the application allows. To avoid over-slew of the regulation loop of the converter, avoid abrupt changes in output voltage of > 300 mV/µs (depending on V_I , output voltage step size and L/C combination). If ramp control is unavailable, an RC filter can be inserted between the DAC output and ADJ/FB pins to slow down the control signal.

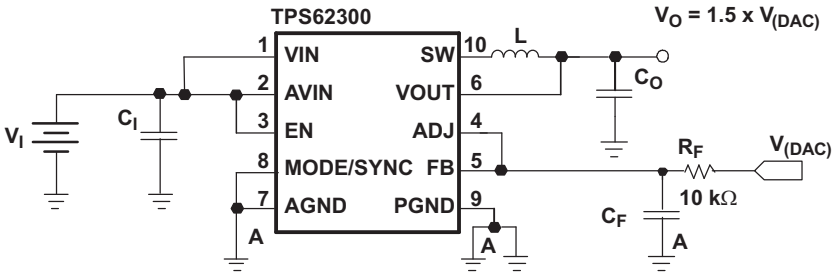


Figure 33. Filtering the DAC Voltage

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6230x, TPS6231x, and TPS6232x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths as indicated in bold on Figure 34.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Use a common ground node for power ground and a different one for control ground (AGND) to minimize the effects of ground noise. Connect these ground nodes together (star point) underneath the IC and make sure that small signal components returning to the AGND pin do not share the high current path of C1 and C2.

The output voltage sense line (VOUT) should be connected right to the output capacitor and routed away from noisy components and traces (e.g., SW line). Its trace should be minimized and shielded by a guard-ring connected to the reference ground. The voltage setting resistive divider should be placed as close as possible to the AGND pin of the IC.

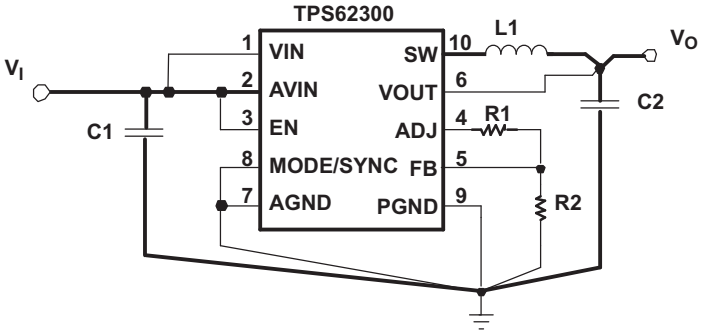


Figure 34. Layout Diagram

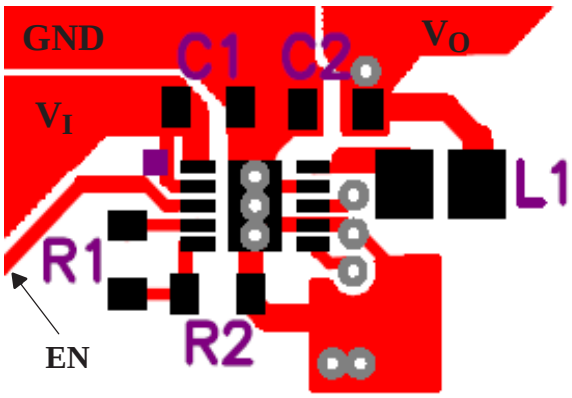


Figure 35. Suggested QFN Layout (Top)

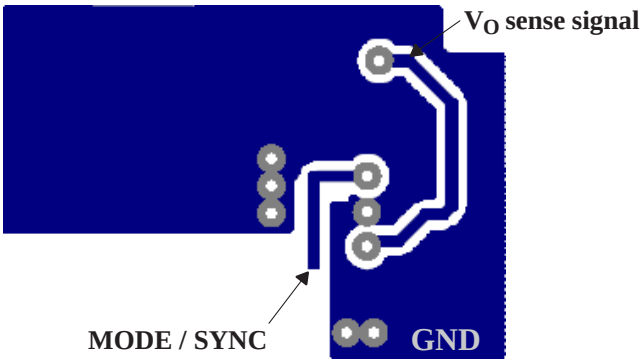


Figure 36. Suggested QFN Layout (Bottom)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6230x, TPS6231x, and TPS6232x devices is 125°C. The thermal resistance of the 8-pin CSP package (YZD, YZ and YED) is $R_{\theta JA}$ = 250°C/W. Specified regulator operation is specified to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW. More power can be dissipated if the maximum ambient temperature of the application is lower, or if the PowerPAD™ package (DRC) is used.

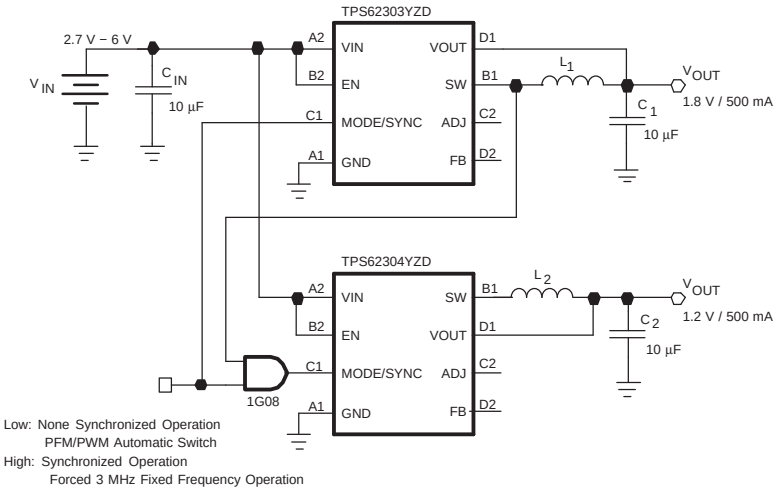
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125°C - 85°C}{250°C/W} = 160 \text{ mW} \quad (6)$$

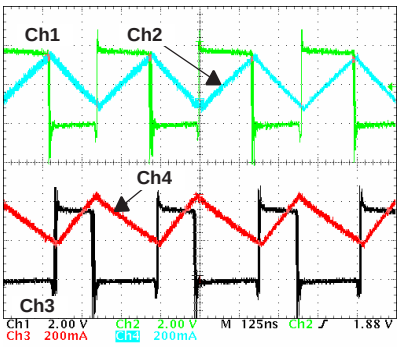
CHIP SCALE PACKAGE DIMENSIONS

The TPS6230x, TPS6231x, and TPS6232x are also available in an 8-bump chip scale package (YZD, YZ NanoFree™ and YED, NanoStar™). The package dimensions are given as:

- D = 1.970 ±0.05 mm
- E = 0.970 ±0.05 mm

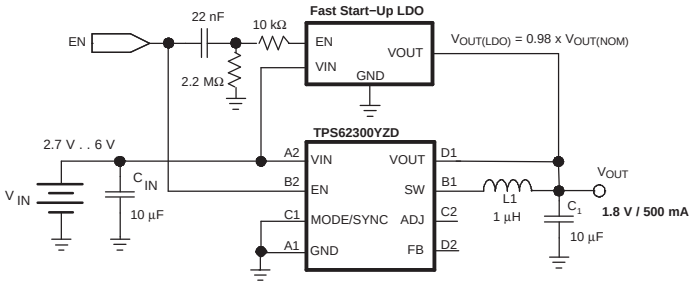
APPLICATION EXAMPLES

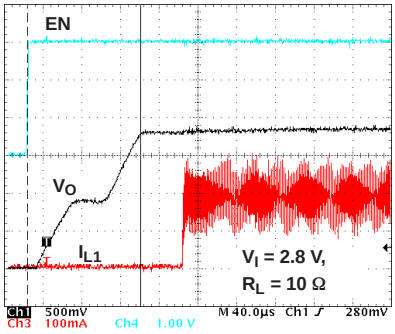




Ch1: SW (1.8-V Output), Ch2: I_{L1}
Ch3: SW (1.2-V Output), Ch4: I_{L2}

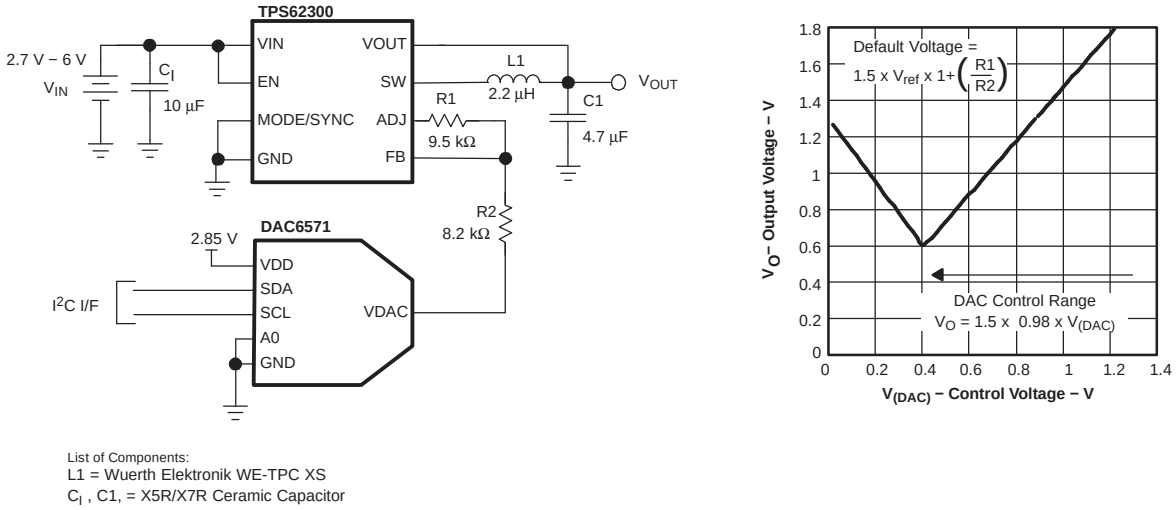
Figure 37. Dual, Out-of-Phase, 3-MHz, 500-mA Step-Down Regulator Features Less Than 50-mm^2 Total Solution Size





Ch1: V_O
Ch3: Inductor Current: I_{L1}
Ch3: EN − External Control Signal

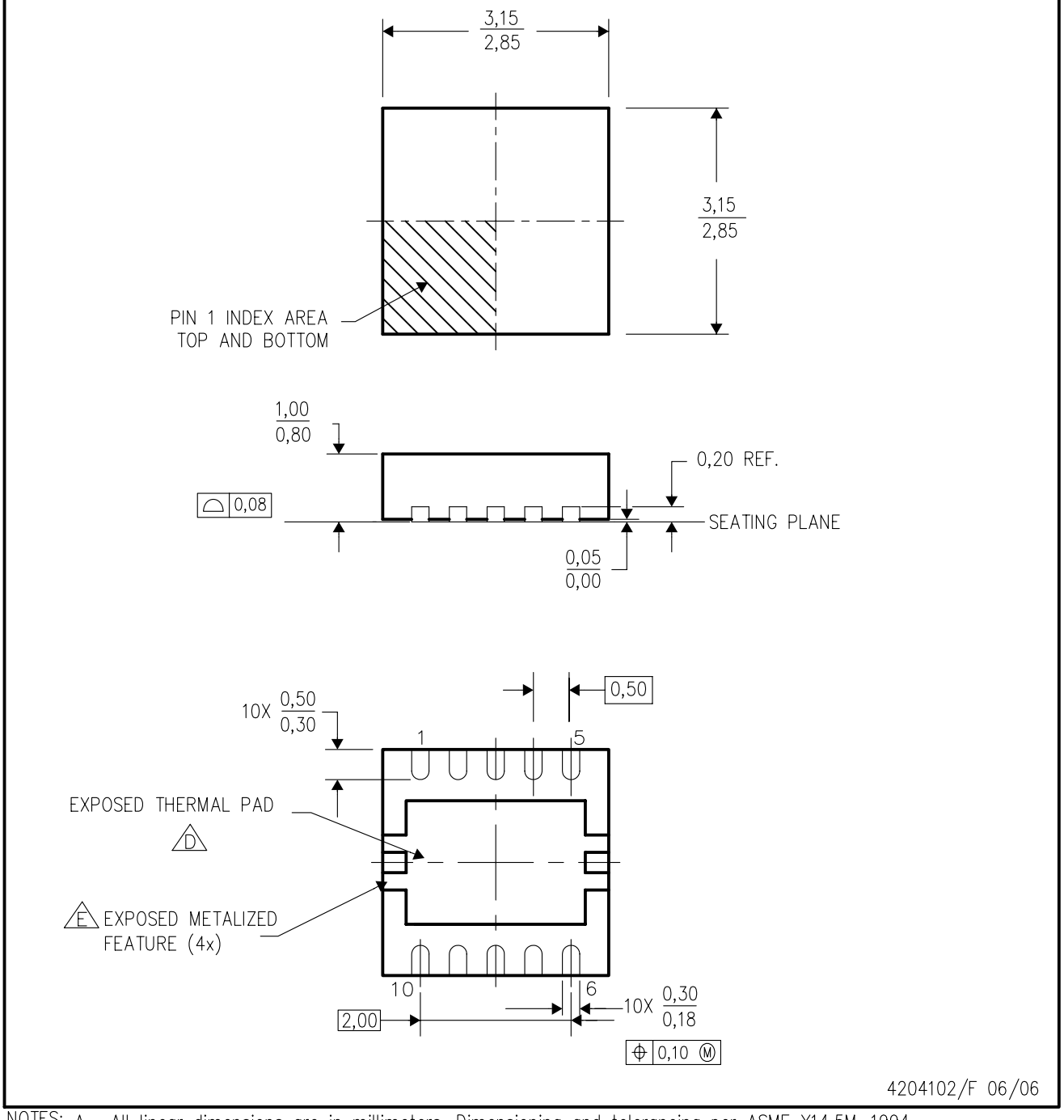
Figure 38. Speed-Up Circuitry for Fast Turnon Time



List of Components:
L1 = Wuerth Elektronik WE-TPC XS
C_I , C1, = X5R/X7R Ceramic Capacitor

Figure 39. Dynamic Voltage Management Using I²C I/F

DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL PAD MECHANICAL DATA

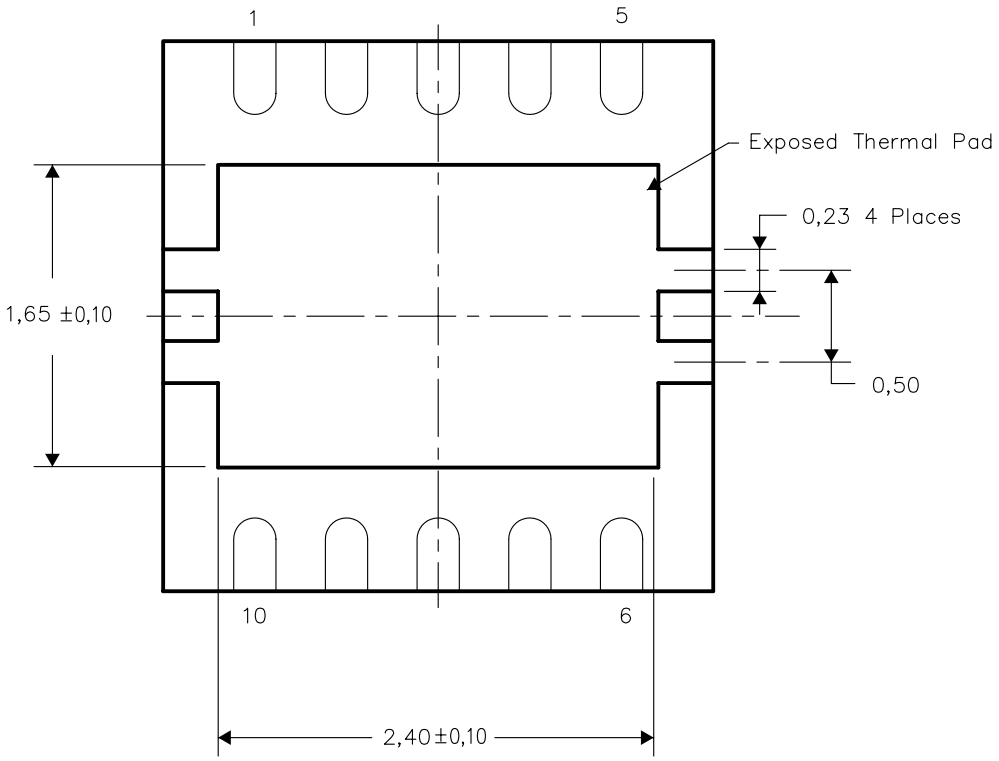
DRC (S–PDSO–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

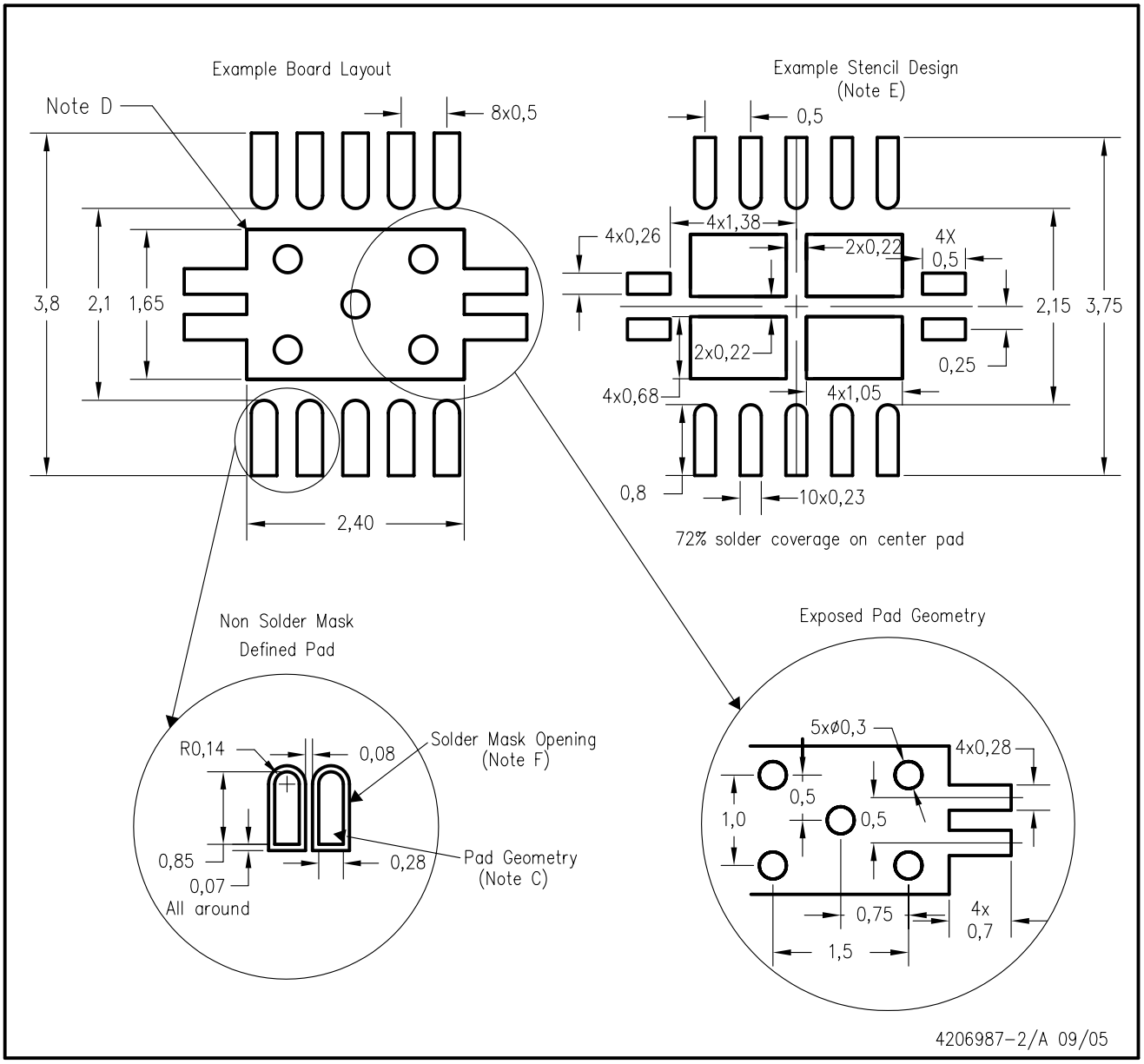


Bottom View

NOTE: All linear dimensions are in millimeters

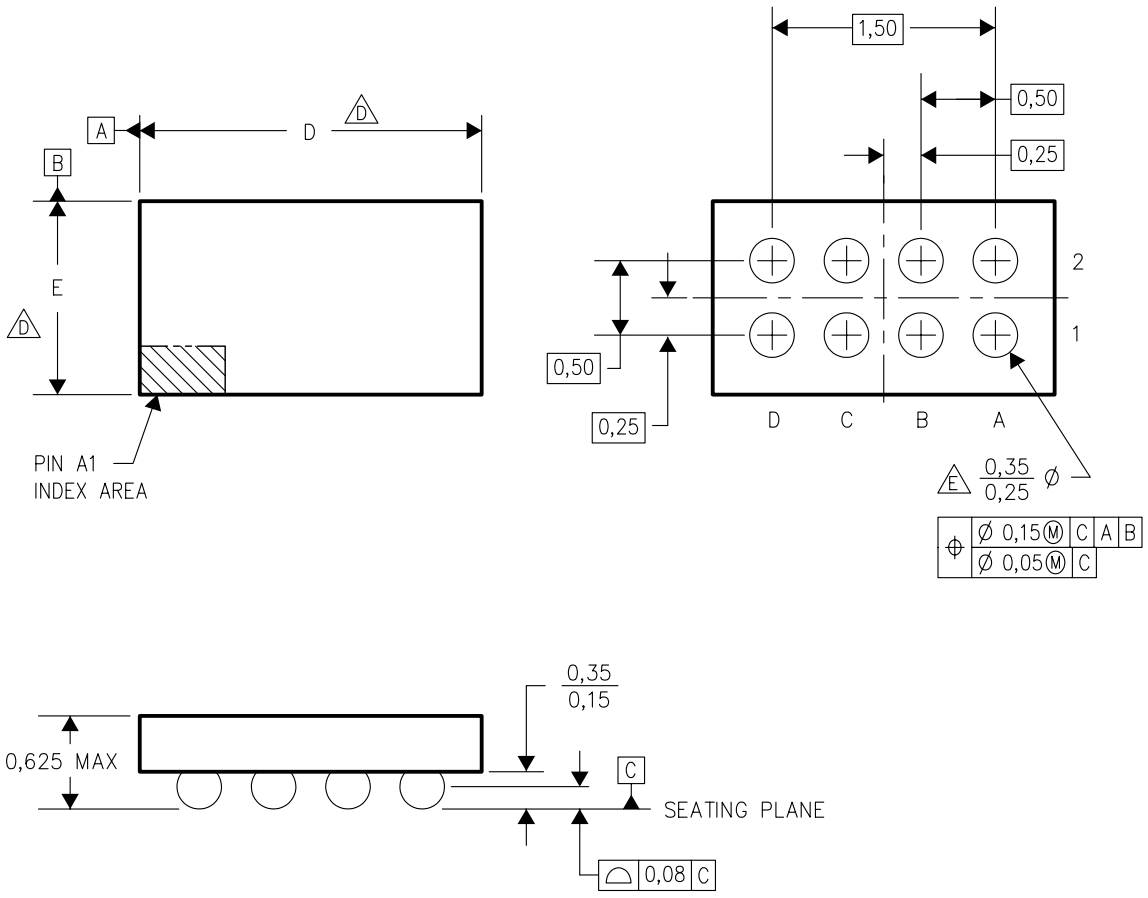
Exposed Thermal Pad Dimensions

DRC (S–PDSO–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YED (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY

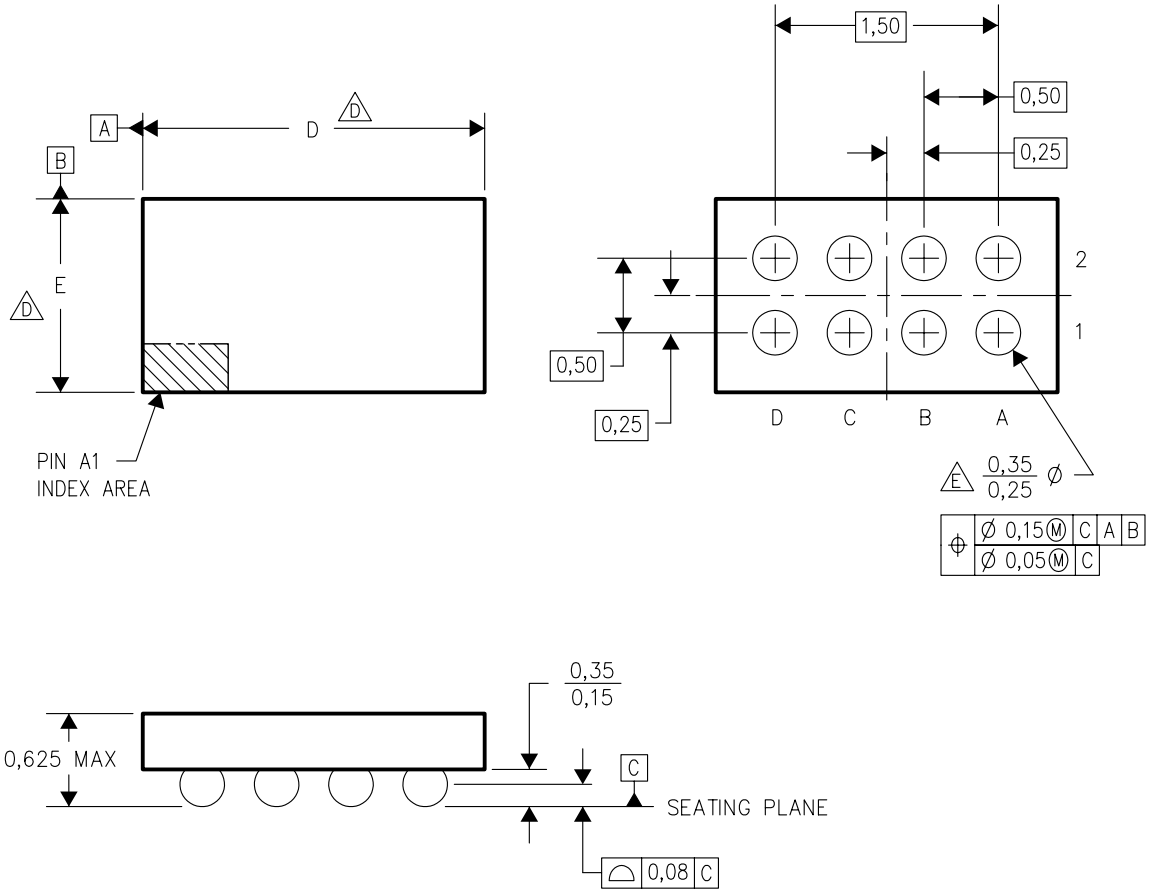


4204180/E 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Devices in YED package can have dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 0.85 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 2 matrix pattern is shown for illustration only.
F. This package contains tin–lead (SnPb) balls. Refer to YZD (Drawing #4205057) for lead–free balls.

NanoStar is a trademark of Texas Instruments.

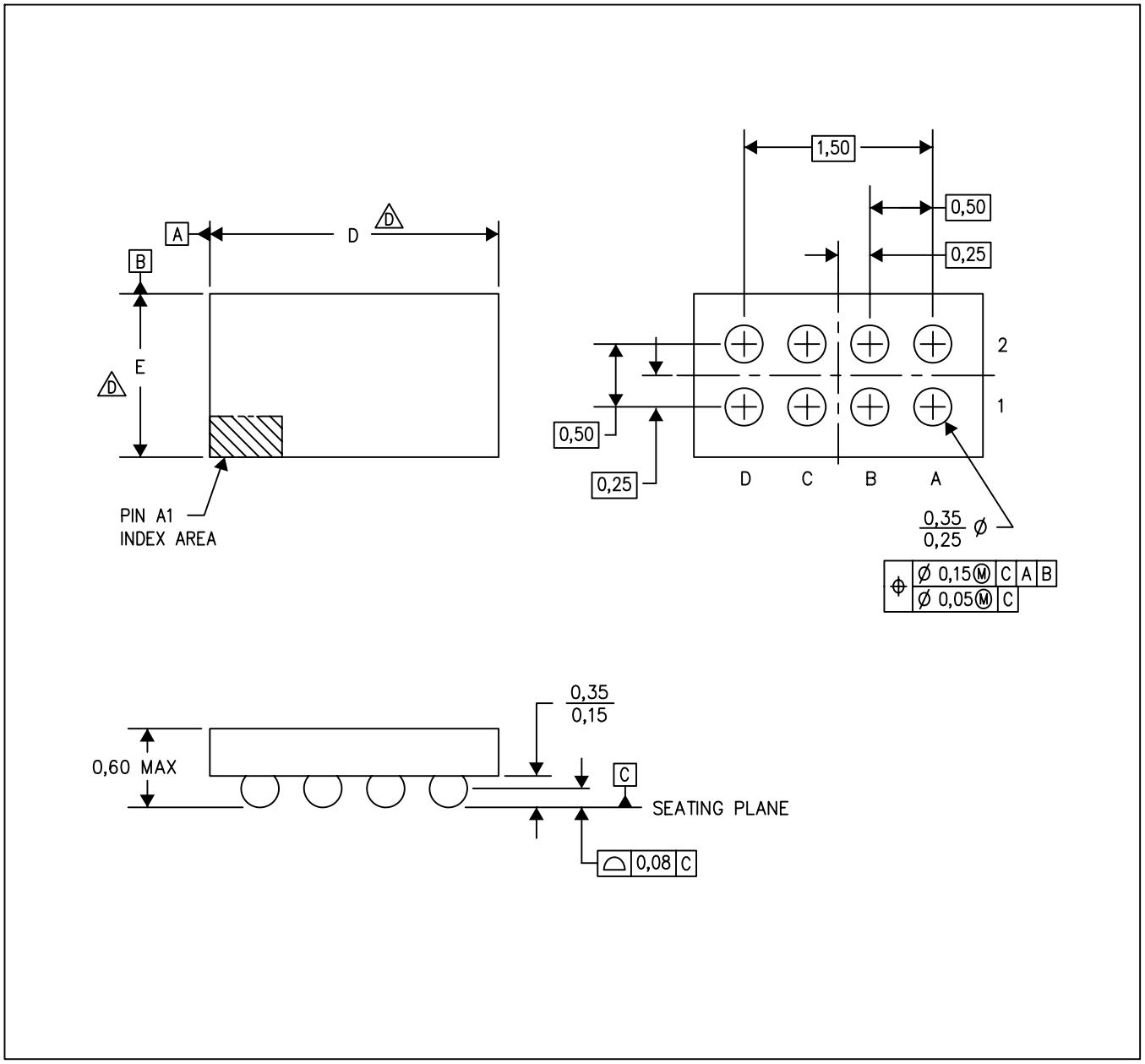
YZD (R–XBGA–N8) DIE–SIZE BALL GRID ARRAY



4205057/C 04/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YZD package can have dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 0.85 to 1.65 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 4 x 2 matrix pattern is shown for illustration only.
F. This package contains lead–free balls. Refer to YED (Drawing #4204180) for tin–lead (SnPb) balls.

NanoFree is a trademark of Texas Instruments.



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Dimension D ranging from 1.85 to 2.65 mm and dimension E ranging from 0.85 to 1.65 mm.
To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.

YZ Wafer Chip–Scale Package Dimensions

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62300DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMN	Samples
TPS62301DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMO	Samples
TPS62302DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMQ	Samples
TPS62303DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMR	Samples
TPS62304DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMS	Samples
TPS62305DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ANU	Samples
TPS62320DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMX	Samples
TPS62321DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AMY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

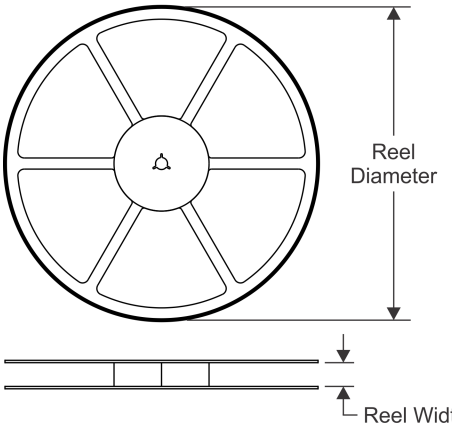
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

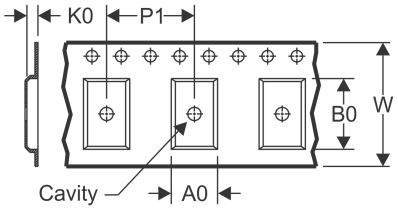
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

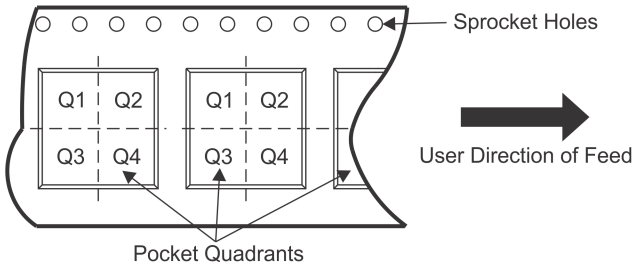


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

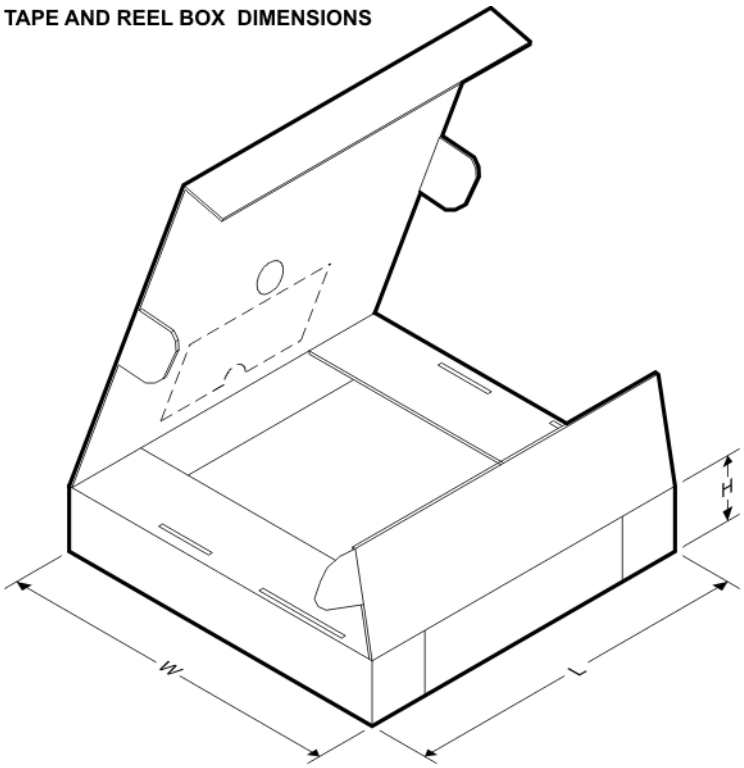
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62300DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62301DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62302DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62303DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62304DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62305DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62320DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62321DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62300DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62301DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62302DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62303DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62304DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62305DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62320DRCR	VSON	DRC	10	3000	350.0	350.0	43.0
TPS62321DRCR	VSON	DRC	10	3000	350.0	350.0	43.0

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