General Description

The MAX14724 is a serial-controlled, 8:4 full-matrix analog multiplexer. The device operates from either a single wide supply or dual ±2.5V supplies. A wide operating range makes the device ideal for battery-powered, portable instruments. All channels guarantee break-before-make switching.

The serial control is selectable between I²C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied. I²C mode provides one address-select pin, allowing for addressing up to two devices on a single bus. The SPI mode includes a DO pin that can be used to daisy-chain multiple devices together with a single select signal.

The MAX14724 features bidirectional operation and can handle rail-to-rail analog signals. All control inputs are 1.6V-logic compatible. This device is available in a small 20-pin, 4mm x 4mm, TQFN and 20-bump, 2mm x 1.7mm, wafer-level package (WLP).

Applications

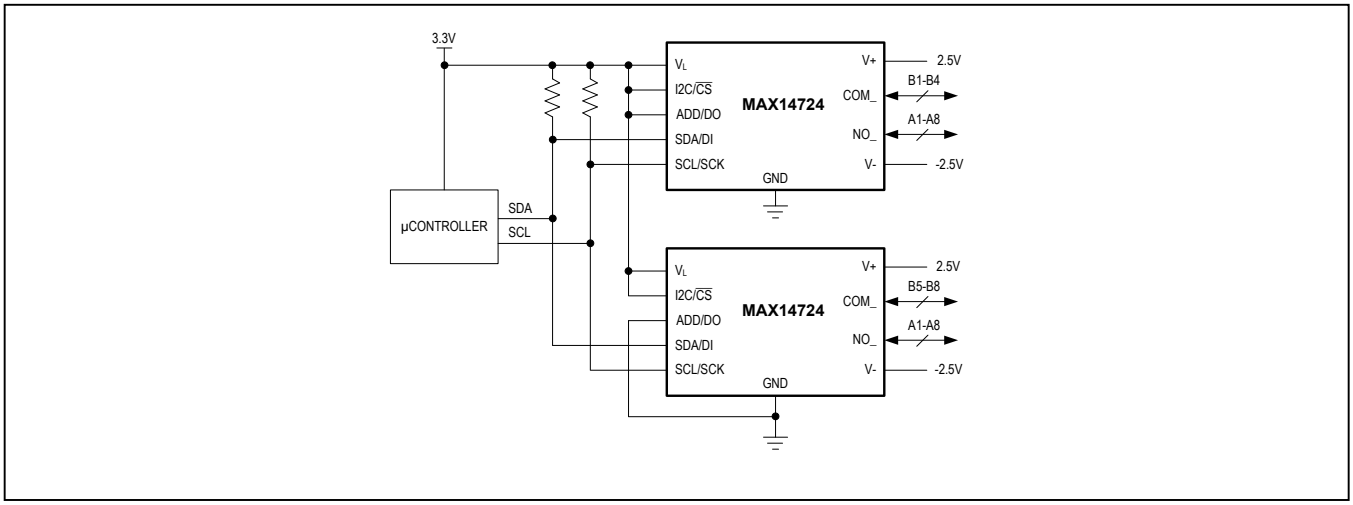
- Medical Equipment
- Data Acquisition
- Signal Switching
- Battery-Powered Equipment

Ordering Information ***appears at end of data sheet.***

Benefits and Features

- Flexible Architecture Enables Ease of Design and Control
  - 8:4 Matrix Switch Multiplexer
  - Fully Programmable with Simultaneous Updates
  - Independent Control of Each Switch
  - Serial Control
    - I²C with Address-Select Pin
    - SPI with DO for Daisy-Chain
    - 1.6V Logic Compatible
- Low Distortion Switching Improves System Performance
  - 1Ω R_{ON} (typ) with +5V or ±2.5V Supply
  - 0.5Ω R_{ON} Match Between Channels (typ)
  - 0.2Ω R_{ON} Flatness Over Signal Range (typ)
  - Low Leakage Current: 5nA at +25°C (typ)
- Integrated Protection for System Reliability
  - ±30kV HBM on NO_ and COM_
  - ±15kV IEC 61000-4-2 Air Gap Discharge on NO_ and COM_
  - ±10kV IEC 61000-4-2 Contact Discharge on NO_ and COM_
- High-Integration Multiplexing Reduces Footprint and System Complexity
  - 20 WLP (2mm x 1.7mm)
  - 20 TQFN (4mm x 4mm)

Typical Application Circuit



maxim integrated™

Absolute Maximum Ratings

V+ .....-0.3V to +6V
V- .....-6V to +0.3V
V_L .....-0.3V to +6V
V+ to V- .....-0.3V to +6V
V_L to V-.....-0.3V to +9V
NO_, COM_ (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
SCL/SCK, SDA/DI, I2C/$\overline{CS}$, ADD/DO .....-0.3V to +6V
ADD/DO to V-.....-0.3V to +9V
Continuous Current into NO_, COM_ .....±50mA
Peak Current into NO_, COM_
(pulsed at 1ms, 10% duty cycle) .....±100mA

Continuous Power Dissipation
20 TQFN (derate 25.6mW/°C above +70°C).....2051mW
20 WLP(derate 21.7mW/°C above +70°C).....1736mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Note 1: Signals on COM_ and NO_ exceeding V+ or V- are clamped by internal diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....39°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....6°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....46°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V+ = 1.6V to 5V, V- = (V+ - 5.5V) to 0V, V_L = 0V to 5.5V (Notes 3, 4), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 2.5V, V- = -2.5V, V_L = 2.5V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V+ Supply	V+		1.6		5.5	V
V- Supply	V-		V+ - 5.5		0	V
V_L Supply	V_L	V- > -2.5V	0		5.5	V
		V- ≤ -2.5V	0		V- + 8	
V+ Supply Current	I+	T_A = +25°C		1	5	µA
V_L Supply Current	I_{VL}	T_A = +25°C		1.5	5	µA
ANALOG SWITCH (Note 6)						
Analog Signal Range	$V_{COM\_}$, $V_{NO\_}$		V-		V+	V
On-Resistance	R_{ON}	$I_{COM\_}$ = 10mA, V+ = 2.5V, V- = -2.5V, $V_{NO\_}$ = V- or V+		1	3	Ω
		$I_{COM\_}$ = 10mA, V+ = 3.0V, V- = 0V, $V_{NO\_}$ = 1.5V			5	
On-Resistance Match Between Channels (Note 7)	ΔR_{ON}	$I_{COM\_}$ = 10mA, V+ = 2.5V, V- = -2.5V, $V_{NO\_}$ = V- or V+		0.5	1.25	Ω
		$I_{COM\_}$ = 10mA, V+ = 3.0V, V- = 0V , $V_{NO\_}$ = 1.5V		1.35		

Electrical Characteristics (continued)

(V+ = 1.6V to 5V, V- = (V+ - 5.5V) to 0V, V_L = 0V to 5.5V (Notes 3, 4), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 2.5V, V- = -2.5V, V_L = 2.5V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
On-Resistance Flatness (Note 8, 9)	R_{ON_FLAT}	V+ = 2.5V, V- = -2.5V, $I_{COM\_}$ = 10mA, $V_{COM\_}$ = -2.5V, -1.25V, 0V, 1.25V, 2.5V		0.2	0.5	Ω
NO_ Off-Leakage Current		T_A = 25°C, Figure 1 (Note 9)	-0.25	+0.005	+0.25	µA
		T_A = 125°C, Figure 1 (Note 9)		+0.5		µA
COM_ Off-Leakage Current		T_A = 25°C, Figure 1 (Note 9)	-0.25	+0.005	+0.25	µA
		T_A = 125°C, Figure 1 (Note 9)		+1.0		µA
COM_ On-Leakage Current		T_A = 25°C, Figure 1 (Note 9)	-0.25	+0.005	+0.25	µA
		T_A = 125°C, Figure 1 (Note 9)		+1.5		µA
DIGITAL I/O						
Input Logic-High	V_{IH}	SCL/SCK, SDA/DI, I²C/$\overline{CS}$, ADD/DO	0.7 x V_L			V
Input Logic-Low	V_{IL}	SCL/SCK, SDA/DI, I²C/$\overline{CS}$, ADD/DO			0.3 x V_L	V
V_L Shutdown Threshold High	V_{LIH}		1.6			V
V_L Shutdown Threshold Low	V_{LIL}				0.4	V
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, V+, or V-	-1	+0.005	+1	µA
Digital Input Capacitance				1		pF
Output Logic-Low (I²C Mode)	V_{OL_I2C}	I_{SINK} = 3mA			0.4	V
Output Logic-Low (SPI Mode)	V_{OL_SPI}	I_{SINK} = 200µA			0.15 x V_L	V
Output Logic-High (SPI Mode)	V_{OH_SPI}	I_{SOURCE} = 200µA	0.85 x V_L			V
DYNAMIC PERFORMANCE						
Turn-Off Time	t_{OFF}	V+ = 2.5V, V- = -2.5V, R_L = 100Ω, C_L = 35pF, $V_{NO\_}$ = 1V, Figure 2		0.6		µs
Break-Before-Make Time	t_{BBM}	V+ = 2.5V, V- = -2.5V, R_L = 100Ω, C_L = 35pF, $V_{NO\_}$ = 1V, Figure 2	0	500		ns
Turn-On Time	t_{ON}	V+ = 2.5V, V- = -2.5V, R_L = 100Ω, C_L = 35pF, $V_{NO\_}$ = 1V, Figure 2		1	2	µs
Bandwidth -3dB	BW	R_S = R_L = 50Ω, $V_{NO\_}$ = 0.5V_{P-P}, C_L = 5pF, Figure 3		50		MHz
Charge Injection	$Q_{COM\_}$, $Q_{NO\_}$	Initial condition: V_{IN} = V_{OUT} = GND. C_{IN} = 1nF, C_{OUT} = 1nF, Figure 4, (Note 10)		-15		pC
NO_ Off-Capacitance	C_{NO_OFF}	$V_{NO\_}$ = 0V, f = 1MHz, Figure 5		50		pF
COM_ Off-Capacitance	C_{COM_OFF}	$V_{COM\_}$ = 0V, f = 1MHz, Figure 5		85		pF
Switch On-Capacitance	C_{ON}	$V_{COM\_}$ = $V_{NO\_}$ = 0V, f = 1MHz, V+ - V- = 5V, Figure 5		125		pF
Off-Isolation		C_L = 5pF, R_L = 50Ω, f = 1MHz, $V_{NO\_}$ = 1V_{RMS}, V+ - V- = 5V, Figure 3		-60		dB

Electrical Characteristics (continued)

(V+ = 1.6V to 5V, V- = (V+ - 5.5V) to 0V, V_L = 0V to 5.5V (Notes 3, 4), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 2.5V, V- = -2.5V, V_L = 2.5V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Crosstalk		C_L = 5pF, R_L = 50Ω, f = 1MHz, $V_{NO\_}$ = $1V_{RMS}$, V+ - V- = 5V, Figure 3			-65		dB
Total Harmonic Distortion Plus Noise	THD+N	R_L = 600Ω, f = 20Hz to 20kHz, $V_{NO\_}$ = $0.5V_{P-P}$, DC bias = (V+ + V-)/2	V+ - V- ≥ 3V		0.1		%
SPI TIMING CHARACTERISTICS (Figure 14, Note 4)							
SCLK Clock Period	t_{CH} + t_{CL}			95			ns
SCLK Pulse-Width High	t_{CH}			35			ns
SCLK Pulse-Width Low	t_{CL}			45			ns
$\overline{CS}$ Fall to SCLK Rise Time	t_{CSS}			15			ns
DI Hold Time	t_{DH}			15			ns
DI Setup Time	t_{DS}			15			ns
Output Data Propagation Delay	t_{DO}	C_L = 15pF, (V+ - V-) ≥ 2.7V and V_L ≥ 2.7V				50	ns
		C_L = 15pF, V_L ≤ 2.7V				125	
DO Rise and Fall Times	t_{FT}	C_L = 15pF			10		ns
$\overline{CS}$ Hold Time	t_{CSH}			60			ns
I^2C TIMING (Figure 6, Note 4)							
I^2C Serial-Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}			1.3			µs
START Condition Setup Time	$t_{SU:STA}$			0.6			µs
START Condition Hold Time	$t_{HD:STA}$			0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$			0.6			µs
Clock Low Period	t_{LOW}			1.3			µs
Clock High Period	t_{HIGH}			0.6			µs
Data Valid to SCL Rise Time	$t_{SU:DAT}$	Write setup time, V_L = (V+ - V-) ≥ 1.8V		100			ns
		Write setup time, V_L = (V+ - V-) = 1.6V		130			
Data Hold Time to SCL Fall	$t_{HD:DAT}$	Write hold time		0			ns

Electrical Characteristics (continued)

(V+ = 1.6V to 5V, V- = (V+ - 5.5V) to 0V, V_L = 0V to 5.5V (Notes 3, 4), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V+ = 2.5V, V- = -2.5V, V_L = 2.5V, T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD PROTECTION						
All COM_ and NO_ pins		Human Body Model (HBM)		±30		kV
All COM_ and NO_ pins		IEC 61000-4-2 Air Gap Discharge		±15		kV
All COM_ and NO_ pins		IEC 61000-4-2 Contact Discharge		±10		kV
All Other Pins		Human Body Model (HBM)		±2		kV

Note 3: V_L maximum operating voltage is 5.5V if V- is greater than -2.5V, otherwise the V_L maximum operating voltage is (V- + 8V)
Note 4: V_L has to be greater than 1.6V for proper I^2C and SPI communication and timing.
Note 5: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 6: (V+ - V-) has to be greater than 2.5V for good analog performance since on-resistance varies greatly when (V+ - V-) < 2.5V (see On-Resistance in *Typical Operating Characteristics*).
Note 7: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 8: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
Note 9: Guaranteed by design.
Note 10: See the *Typical Operating Characteristics* for performance across operating range.

Test Circuits/Timing Diagrams

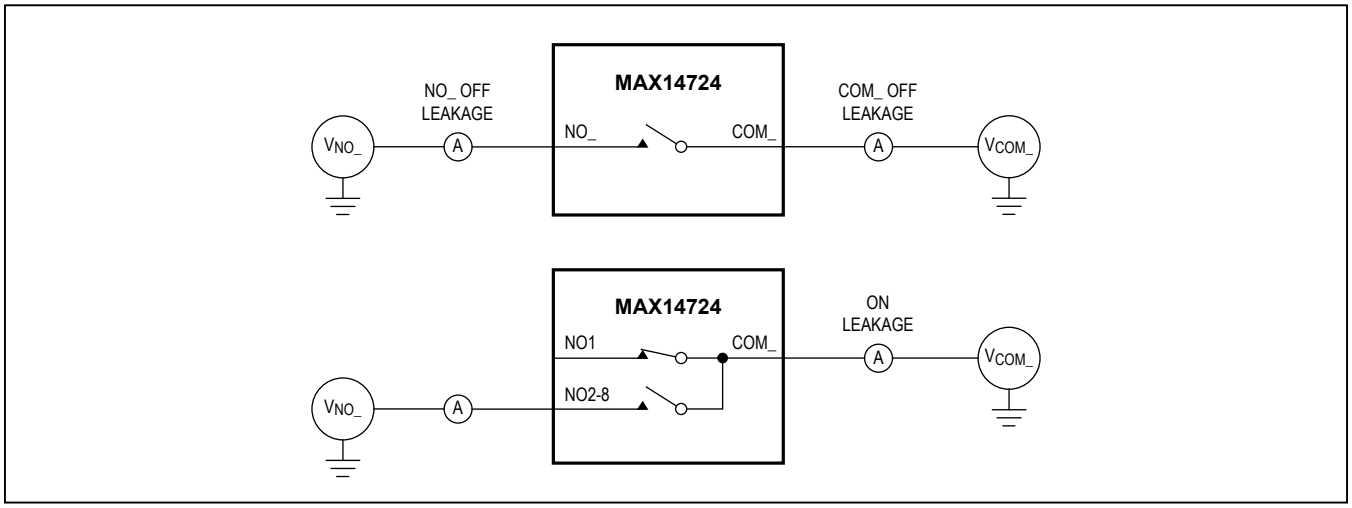


Figure 1. On/Off-Leakage Current

Test Circuits/Timing Diagrams (continued)

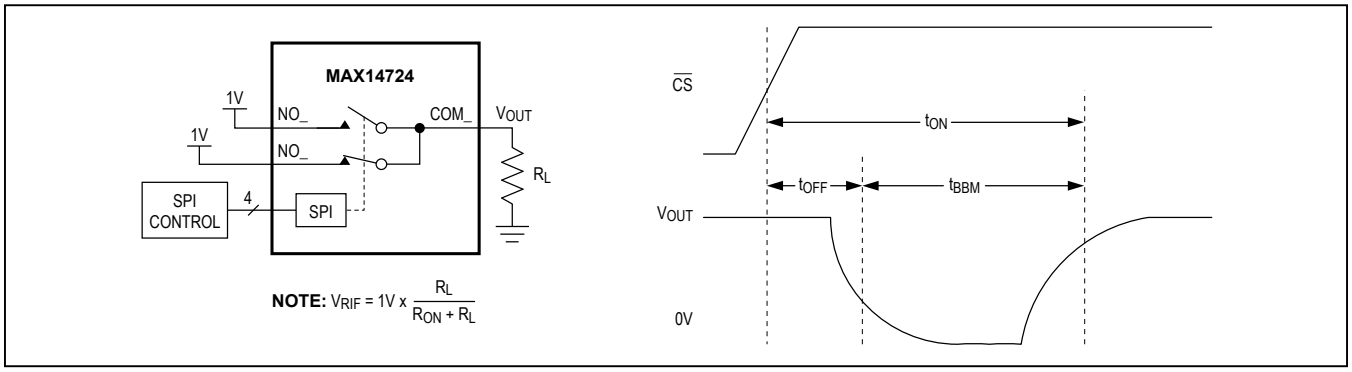


Figure 2. Turn-On/Turn-Off/Break-Before-Make

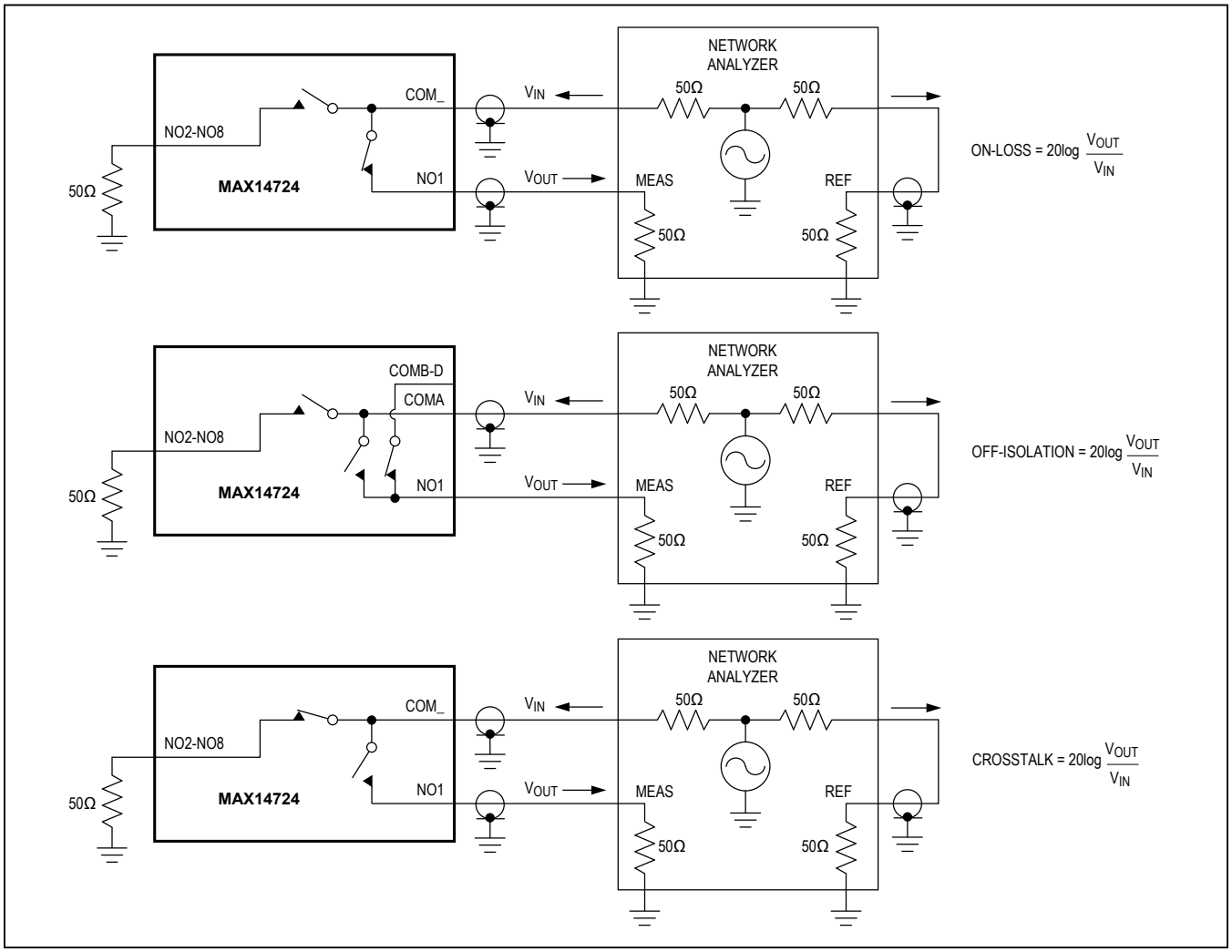


Figure 3. Insertion Loss, Off-Isolation, and Crosstalk

Test Circuits/Timing Diagrams (continued)

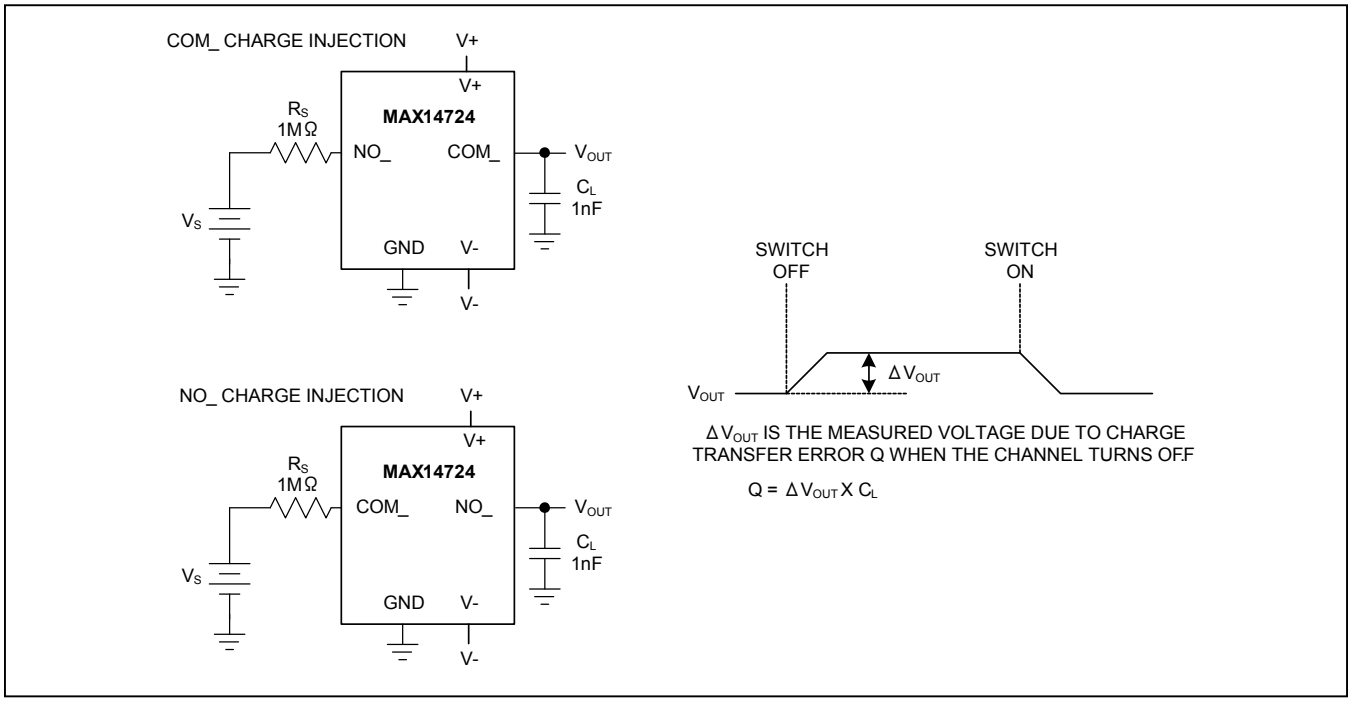


Figure 4. Charge Injection

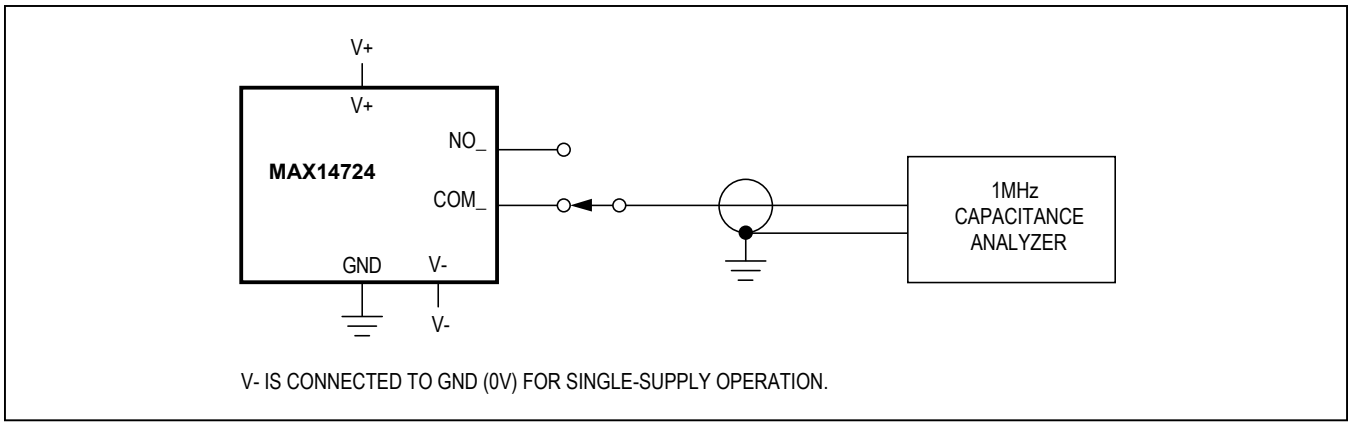
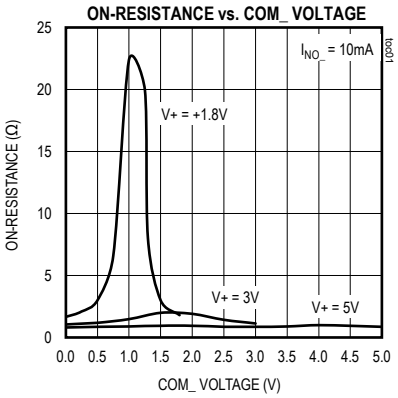
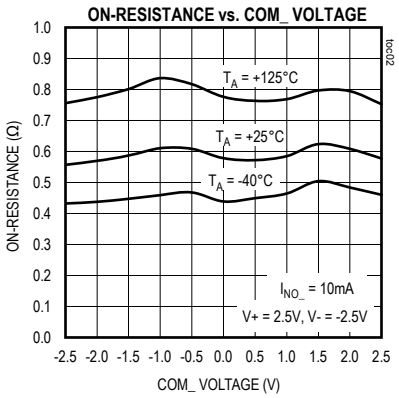


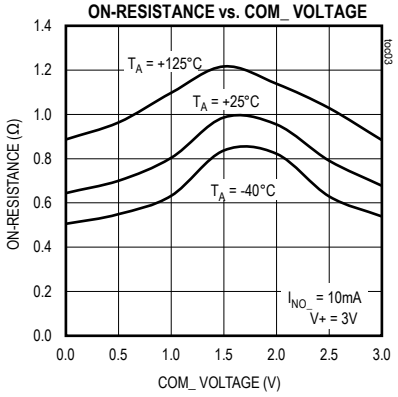
Figure 5. COM_, NO_ Capacitance

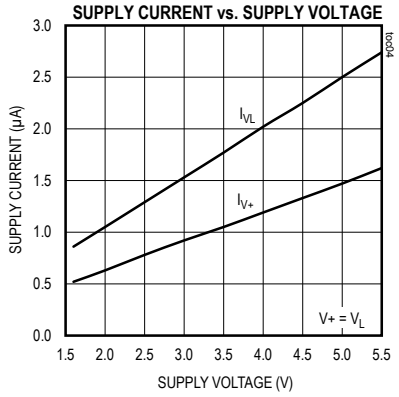
Typical Operating Characteristics

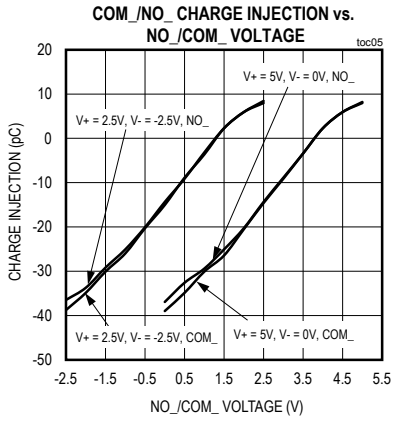
(V+ = 5V, V- = 0V, V_L = V+, T_A = +25°C, unless otherwise noted.)

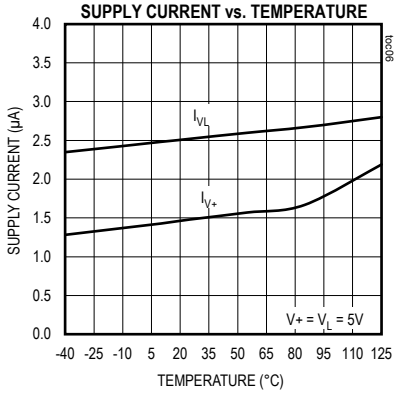








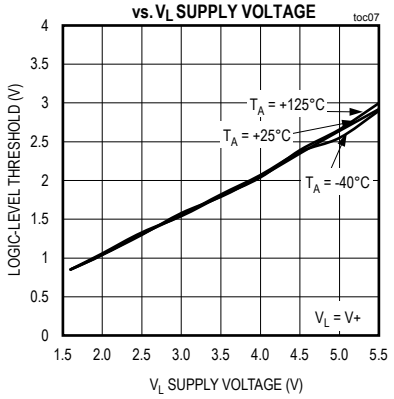




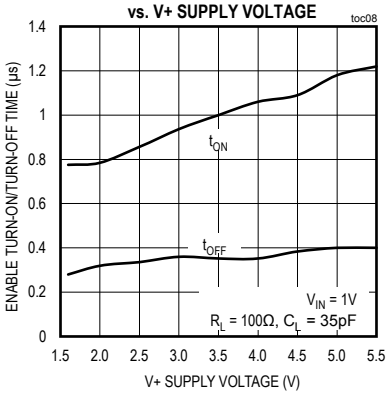
Typical Operating Characteristics (continued)

(V+ = 5V, V- = 0V, V_L = V+, T_A = +25°C, unless otherwise noted.)

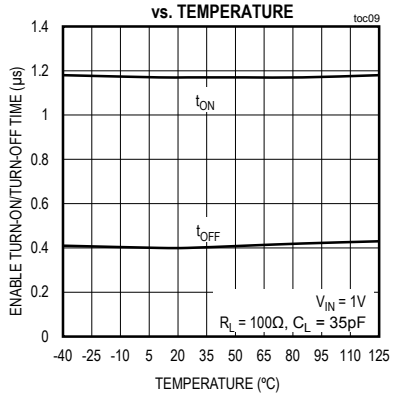
LOGIC-LEVEL THRESHOLD vs. V_L SUPPLY VOLTAGE



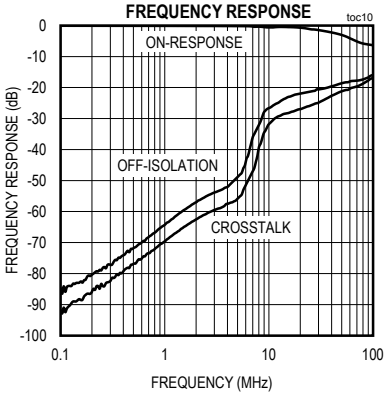
ENABLE TURN-ON/TURN-OFF TIME vs. V+ SUPPLY VOLTAGE



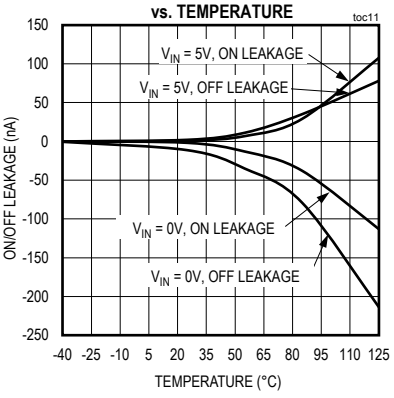
ENABLE TURN-ON/TURN-OFF TIME vs. TEMPERATURE



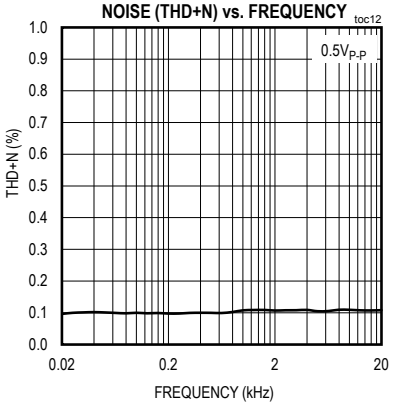
FREQUENCY RESPONSE



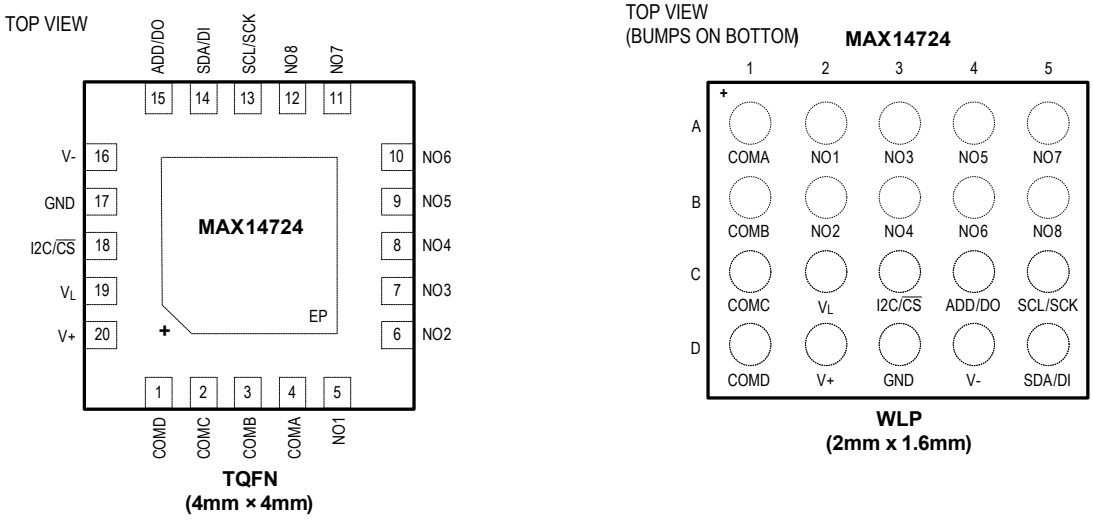
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



TOTAL HARMONIC DISTORTION PLUS NOISE (THD+N) vs. FREQUENCY



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
TQFN	WLP		
1	D1	COMD	Common Terminal D
2	C1	COMC	Common Terminal C
3	B1	COMB	Common Terminal B
4	A1	COMA	Common Terminal A
5	A2	NO1	Normally Open Terminal 1
6	B2	NO2	Normally Open Terminal 2
7	A3	NO3	Normally Open Terminal 3
8	B3	NO4	Normally Open Terminal 4
9	A4	NO5	Normally Open Terminal 5
10	B4	NO6	Normally Open Terminal 6
11	A5	NO7	Normally Open Terminal 7
12	B5	NO8	Normally Open Terminal 8
13	C5	SCL/SCK	I^2C Serial Clock/SPI Serial Clock
14	D5	SDA/DI	I^2C Serial Data/SPI Data Input
15	C4	ADD/DO	I^2C Address Bit/SPI Data Output
16	D4	V-	Negative Supply Voltage Input
17	D3	GND	Ground
18	C3	I2C/$\overline{CS}$	I^2C Select (High)/SPI $\overline{CS}$ (Low). (See the *I^2C and SPI* section).
19	C2	V_L	Logic Supply Voltage for SCL/SCK, SDA/DI, ADD/DO, and I2C/$\overline{CS}$. Drive V_L low to turn off all switches and reset all registers.
20	D2	V+	Positive Supply Voltage Input
—	—	EP	Exposed Pad (TQFN Only). Internally connected to V-. Can be connected to a large plane to maximize thermal performance. Not intended as an electrical connection point.

Functional Diagram

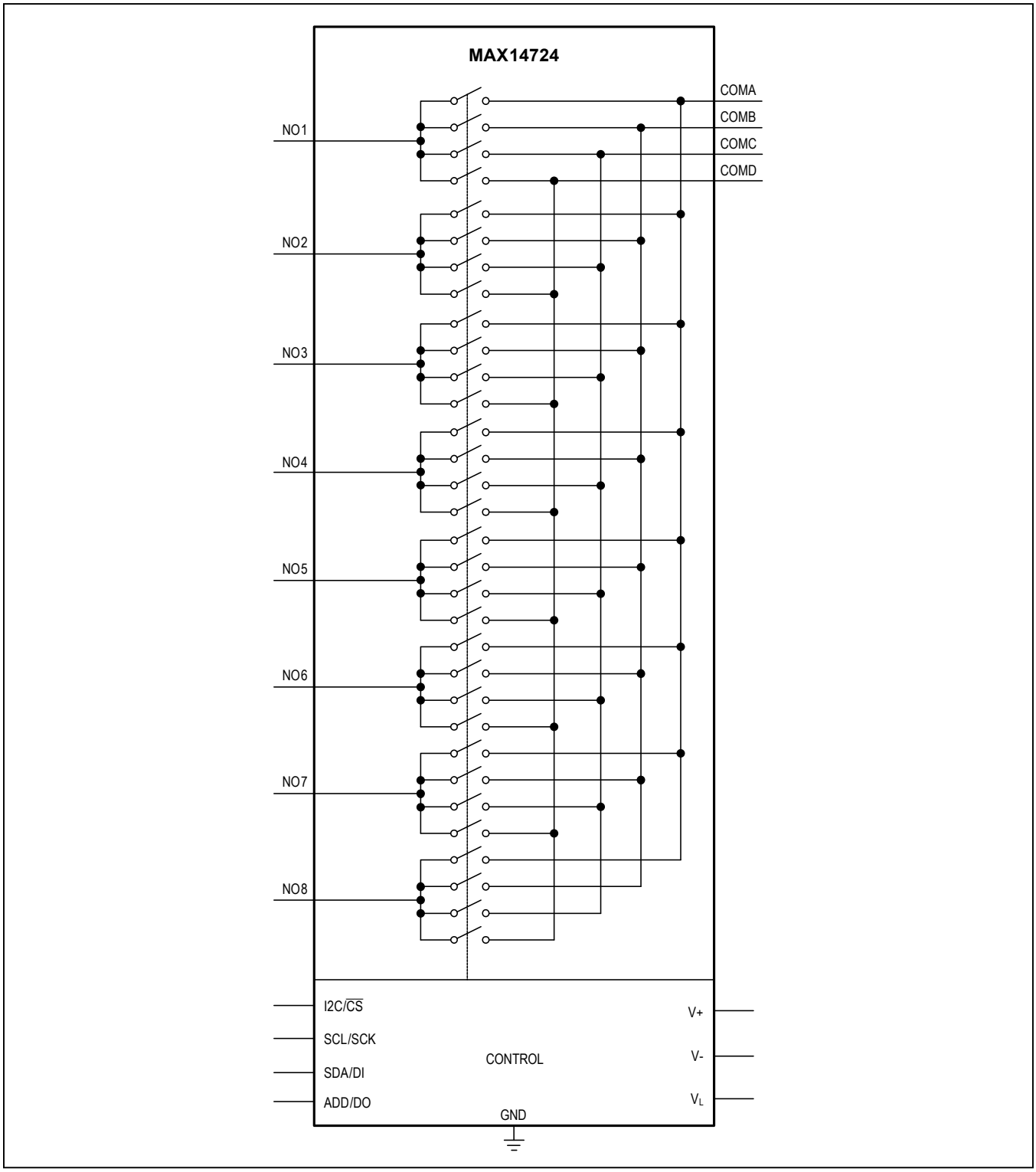


Table 1. Register Map

ADDRESS	NAME	TYPE	DEFAULT	DESCRIPTION
0x00	DIR0	RW	0x00	Switches 8A-1A direct read/write access
0x01	DIR1	RW	0x00	Switches 8B-1B direct read/write access
0x02	DIR2	RW	0x00	Switches 8C-1C direct read/write access
0x03	DIR3	RW	0x00	Switches 8D-1D direct read/write access
0x10	SHDW0	RW	0x00	Switches 8A-1A shadow read/write access
0x11	SHDW1	RW	0x00	Switches 8B-1B shadow read/write access
0x12	SHDW2	RW	0x00	Switches 8C-1C shadow read/write access
0x13	SHDW3	RW	0x00	Switches 8D-1D shadow read/write access
0x14	CMD0	RW	0x00	Set mux A and B command (reads 0x00)
0x15	CMD1	RW	0x00	Set mux C and D command (reads 0x00)

Table 2. Detailed Register Map

DIR0 0x00								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Direct_SW8A-1A							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Direct Register Data for SW8A-1A 0 = Switch open 1 = Switch closed							
DIR1 0X01								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Direct_SW8B-1B							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Direct Register Data for SW8B-1B 0 = Switch open 1 = Switch closed							
DIR2 0X02								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Direct_SW8C-1C							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Direct Register Data for SW8C-1C 0 = Switch open 1 = Switch closed							
DIR3 0X03								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Direct_SW8D-1D							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Direct Register Data for SW8D-1D 0 = Switch open 1 = Switch closed							

Table 2. Detailed Register Map (continued)

SHDW0 0X10								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Shadow_SW8A-1A							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Shadow Register Data for SW8A-1A; temporarily holding register for simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW1 0X11								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Shadow_SW8B-1B							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Shadow Register Data for SW8B-1B; temporarily holding register for simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW2 0X12								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Shadow_SW8C-1C							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Shadow Register Data for SW8C-1C; temporarily holding register for simultaneous updates. 0 = Switch open 1 = Switch closed							
SHDW3 0X13								
BIT	7	6	5	4	3	2	1	0
BIT NAME	Shadow_SW8D-1D							
RESET VALUE	0	0	0	0	0	0	0	0
DESCRIPTION	Shadow Register Data for SW8D-1D; temporarily holding register for simultaneous updates. 0 = Switch open 1 = Switch closed							

Table 2. Detailed Register Map (continued)

CMD0 0X14								
BIT	7	6	5	4	3	2	1	0
BIT NAME	SelB				SelA			
RESET VALUE	0	0	0	0	0	0	0	0
SelB	0000 = Enable only SW1B (Set DIR1 = 0x01) 0001 = Enable only SW2B (Set DIR1 = 0x02) 0010 = Enable only SW3B (Set DIR1 = 0x04) 0011 = Enable only SW4B (Set DIR1 = 0x08) 0100 = Enable only SW5B (Set DIR1 = 0x10) 0101 = Enable only SW6B (Set DIR1 = 0x20) 0110 = Enable only SW7B (Set DIR1 = 0x40) 0111 = Enable only SW8B (Set DIR1 = 0x80) 1000 = Disable all bank B switches (Set DIR1 = 0x00) 1001 = Copy B shadow registers (Set DIR1 = SHDW1) to switches 1010 .. 1111 = No change on bank B							
SelA	0000 = Enable only SW1A (Set DIR0 = 0x01) 0001 = Enable only SW2A (Set DIR0 = 0x02) 0010 = Enable only SW3A (Set DIR0 = 0x04) 0011 = Enable only SW4A (Set DIR0 = 0x08) 0100 = Enable only SW5A (Set DIR0 = 0x10) 0101 = Enable only SW6A (Set DIR0 = 0x20) 0110 = Enable only SW7A (Set DIR0 = 0x40) 0111 = Enable only SW8A (Set DIR0 = 0x80) 1000 = Disable all bank A switches (Set DIR0 = 0x00) 1001 = Copy A shadow registers (Set DIR0 = SHDW0) to switches 1010 .. 1111 = No change on bank A							

Table 2. Detailed Register Map (continued)

CMD1 0X15								
BIT	7	6	5	4	3	2	1	0
BIT NAME	SelD				SelC			
RESET VALUE	0	0	0	0	0	0	0	0
SelD	0000 = Enable only SW1D (Set DIR3 = 0x01) 0001 = Enable only SW2D (Set DIR3 = 0x02) 0010 = Enable only SW3D (Set DIR3 = 0x04) 0011 = Enable only SW4D (Set DIR3 = 0x08) 0100 = Enable only SW5D (Set DIR3 = 0x10) 0101 = Enable only SW6D (Set DIR3 = 0x20) 0110 = Enable only SW7D (Set DIR3 = 0x40) 0111 = Enable only SW8D (Set DIR3 = 0x80) 1000 = Disable all bank D switches (Set DIR3 = 0x00) 1001 = Copy D shadow registers (Set DIR3 = SHDW3) to switches 1010 .. 1111 = No change on bank D							
SelC	0000 = Enable only SW1C (Set DIR2 = 0x01) 0001 = Enable only SW2C (Set DIR2 = 0x02) 0010 = Enable only SW3C (Set DIR2 = 0x04) 0011 = Enable only SW4C (Set DIR2 = 0x08) 0100 = Enable only SW5C (Set DIR2 = 0x10) 0101 = Enable only SW6C (Set DIR2 = 0x20) 0110 = Enable only SW7C (Set DIR2 = 0x40) 0111 = Enable only SW8C (Set DIR2 = 0x80) 1000 = Disable all bank C switches (Set DIR2 = 0x00) 1001 = Copy C shadow registers (Set DIR2 = SHDW2) to switches 1010 .. 1111 = No change on bank C							

Detailed Description

The MAX14724 is a serial-controlled 8:4 full-matrix analog multiplexer. The serial control is selectable between I^2C and SPI. Both modes provide individual control of each independent switch so that any combination of switches can be applied.

The device does not require balanced positive (V+) and negative (V-) supply voltage. However, the voltage difference between the two supplies (V+ - V-) should not exceed 5.5V.

Shutdown

The V_L supply pin can be used as an active-low shutdown/reset signal. When the voltage at V_L is below the V_L Shutdown Threshold Low, all switches are opened and all registers reset, including the SPI-select latch. None of the switches can be activated until the voltage at V_L rises above the V_L Shutdown Threshold High. The device also resets when power is removed from V+, but it is better to use V_L to signal reset or shutdown since the voltages at the analog switch pins (NO_/COM_) must remain between V- and V+, but are independent of V_L.

I^2C and SPI

The I2C/$\overline{CS}$ pin is used simultaneously to select between the I^2C and SPI interfaces and as a chip-select pin for the SPI interface. When logic-high is applied on I2C/$\overline{CS}$, the device enables I^2C communication. To enable SPI communication, I2C/$\overline{CS}$ needs to be driven low and a serial clock should be applied on SCL/SCK. After 21 periods of clock on SCL/SCK, the device latches into SPI mode and I2C/$\overline{CS}$ operates as a purely chip-select pin. The device does not resume I^2C operation if I2C/$\overline{CS}$ is driven high. To return from the latched SPI state and to the I^2C state, V_L or V+ must be driven low. Once V_L or V+ returns high, a logic-high on I2C/$\overline{CS}$ puts the device in the I^2C state again.

I²C Serial Interface

Direct Access Registers

Direct-access registers (DIR0–DIR3) allow the user to read/write the switches eight at a time. These register addresses support autoincrementing so they can be read or written sequentially. The switches are updated once the last bit of the byte is clocked in.

Shadow Registers

Shadow registers (SHDW0–SHDW3) provide storage for switch values to allow for simultaneous updates of the switches. Unlike direct-access registers, these registers have no immediate effect until the copy command is issued. The copy command has to be written in the CMD0 and CMD1 registers. Write to the four registers with the desired state of each switch and then write the appropriate command to registers CMD0 and CMD1 to simultaneously apply the values to the switches.

Set Mux Command Registers

Set mux command registers (CMD0, CMD1) allow the user to easily select any single switch in a bank. The CMD0[7:4] bits allow the user to turn on one single switch in bank B, to open all bank B switches, to copy SHDW1 to DIR1 register, or to leave bank B as is (no change). The CMD0[3:0] bits allow the user to turn on a single switch in bank A, to open all bank A switches, to copy SHDW0 to DIR0 register, or to leave bank A as is (no change). Similarly, the CMD1[7:4] bits allow the user to turn on a single switch in bank D, to open all bank D switches, to copy SHDW3 to DIR3 register, or to leave bank D as is (no change). The CMD1[3:0] bits allow the user to turn on a single switch in bank C, to open all bank C switches, to copy SHDW2 to DIR2 register, or to leave bank C as is (no change). The values apply to the switches once both registers (CMD0 and CMD1) have been written. CMD0 and CMD1 are single 16-bit registers. Therefore, CMD0 must be programmed before CMD1.

Serial Addressing

When in I²C mode, the device operates as a slave device that sends/receives data through an I²C-compatible 2-wire interface. The interface uses a serial-data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the device and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open-drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open-drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX14724 7-bit slave address plus R/$\overline{W}$ bit, a register address byte, one or more data bytes, and, finally, a STOP condition (Figure 6).

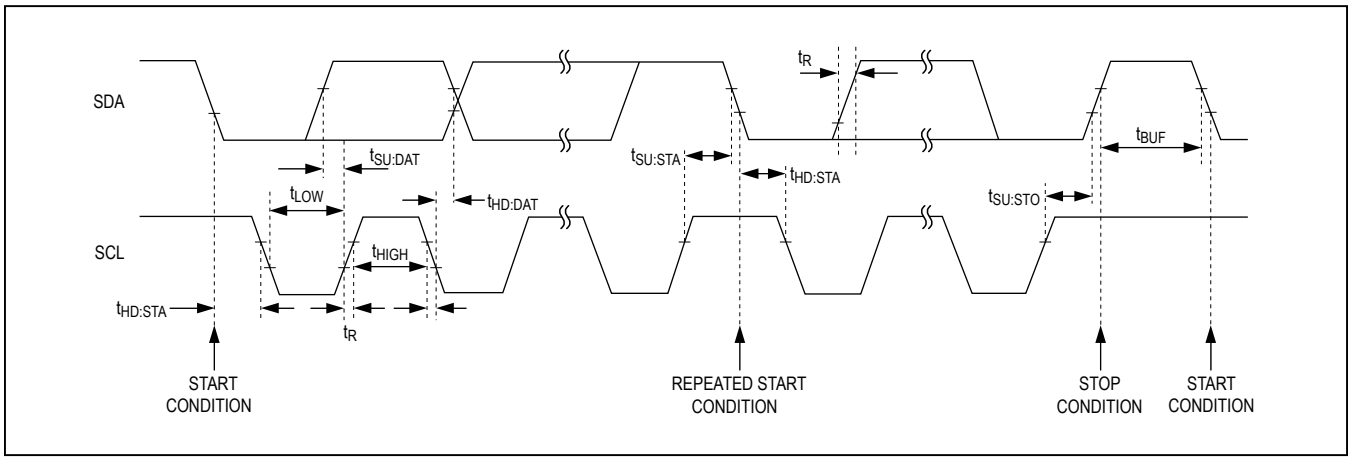


Figure 6. I²C Interface Timing Details

START and STOP Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 7). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

Bit Transfer

One data bit is transferred during each clock pulse (Figure 8). The data on SDA must remain stable while SCL is high.

Acknowledge

An acknowledge bit (ACK) is a clocked 9th bit (Figure 9), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX14724, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device did not pull SDA low, a not acknowledge (NACK) is indicated.

Slave Address

The device features a 7-bit slave address, configured by the ADD/DO input. To select the slave address, connect ADD/DO to GND or V_L, as indicated in Table 3. The device has two possible addresses, allowing up to two MAX14724 devices to share the same interface bus. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command.

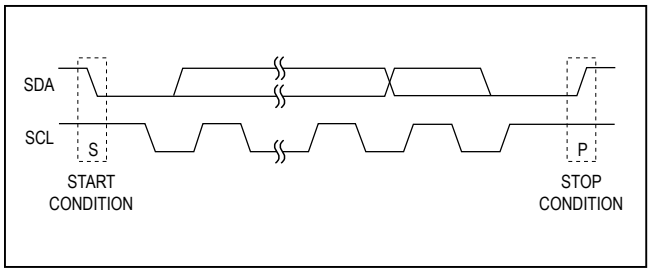


Figure 7. START and STOP Conditions

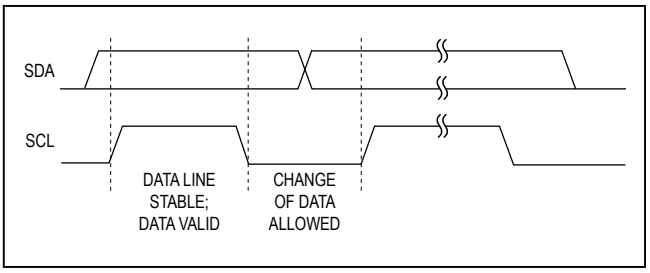


Figure 8. Bit Transfer

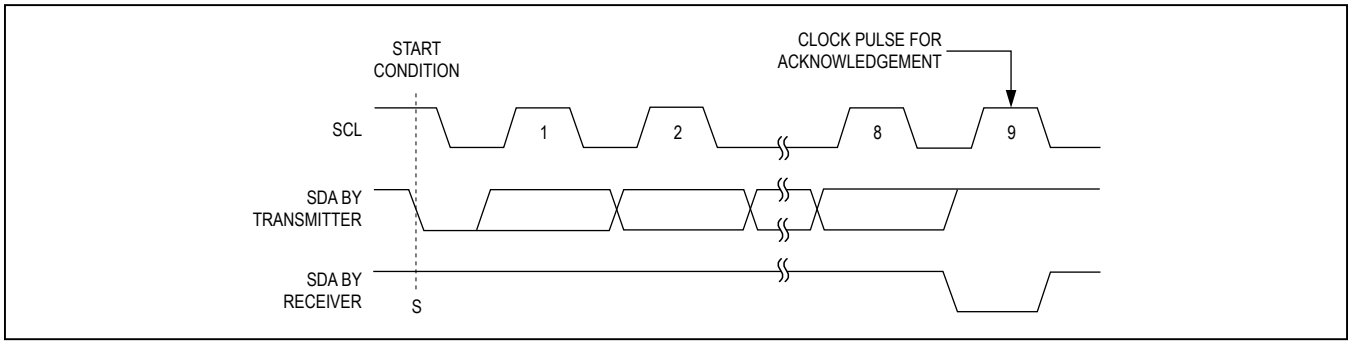


Figure 9. Acknowledge

Table 3. Slave Address Configuration

LOGIC INPUT	I²C SLAVE ADDRESS									
ADD/DO	A6	A5	A4	A3	A2	A1	A0 (ADD)	R/$\overline{W}$	READ	WRITE
0	1	1	1	0	1	0	0	1/0	0xE9	0xE8
1	1	1	1	0	1	0	1	1/0	0xEB	0xEA

Bus Reset

The device resets the bus with the I²C START condition for reads. When the R/$\overline{W}$ bit is set to 1, the device transmits data to the master. Therefore, the master is reading from the device.

Format for Writing

A write to the MAX14724 comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address, with subsequent data bytes going into subsequent registers (Figure 10). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses autoincrement (Figure 11).

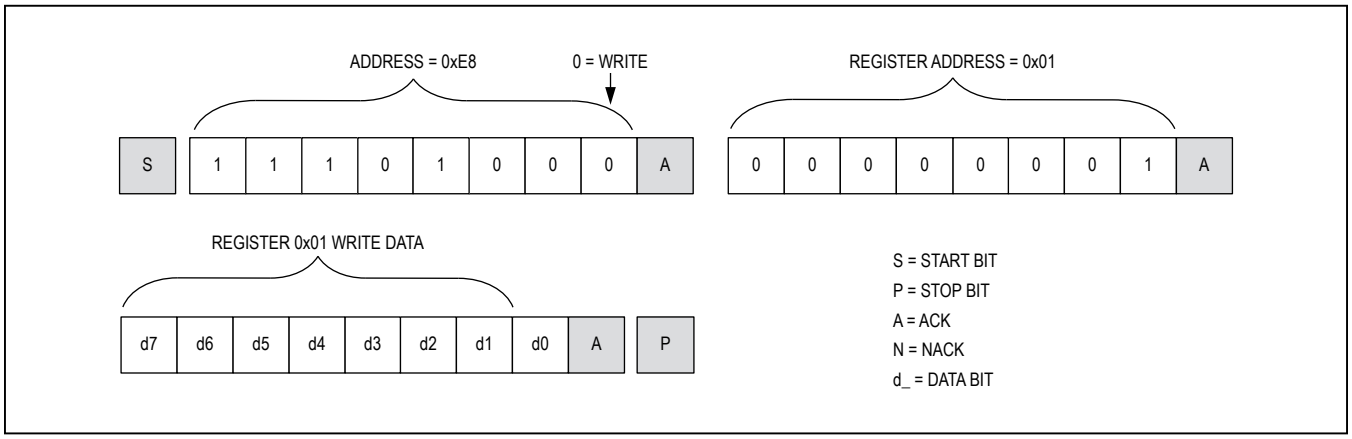


Figure 10. Format for I²C Write

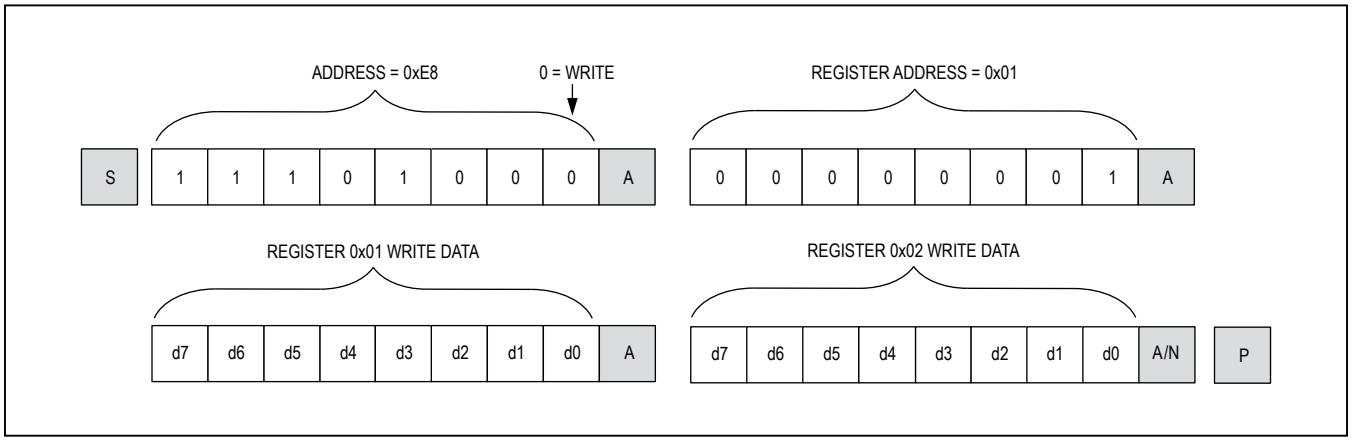


Figure 11. Format for Writing to Multiple Registers

Format for Reading

The device is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer autoincrements after each data byte is read using the same rules for a write. Therefore, a read is initiated by first configuring the register address by performing a write (Figure 11). The master can now read consecutive bytes from the device, with the first data byte being read from the register address pointed to by the previously written register address (Figure 12). Once the master sounds a NACK, the MAX14724 stops sending valid data.

SPI Interface

In SPI mode, the device operates a shift register designed to work with common serial interfaces. The bits are shifted through so that a large serial chain can be made to minimize pins needed for a system with multiple devices (see Figure 21). This shift register is also designed to be compatible with common microcontroller SPI-type interfaces. The switches in the MAX14724 are all transitioned simultaneously. To update the switches in SPI mode, the user must shift in a bit with the desired state of each switch according to the data format listed in Table 4. The switches are updated at the rising edge of $\overline{CS}$, with the last 32 bits of data shifted in only if the number of bits clocked in is greater than or equal to the number of switches (32). The DO pin is the serial output of the shift register.

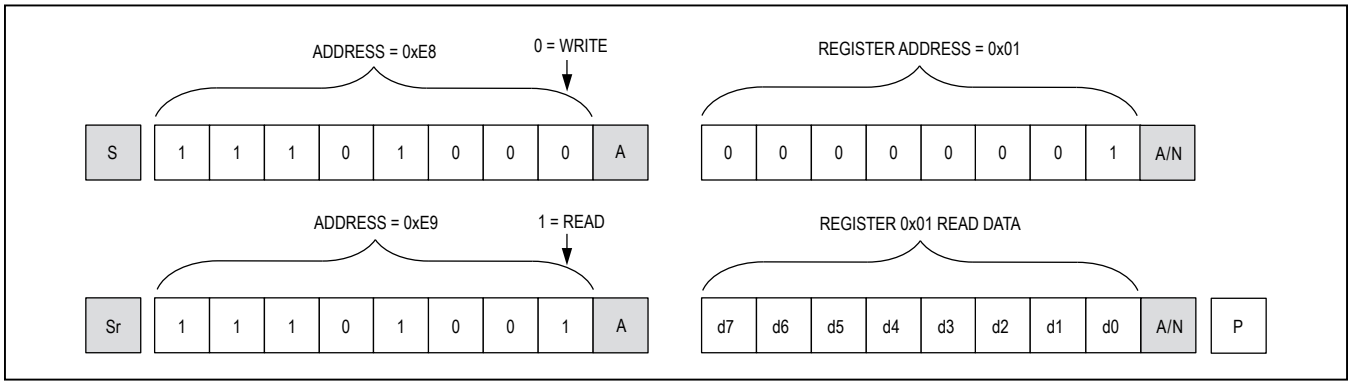


Figure 12. Format for Reads (Repeated START)

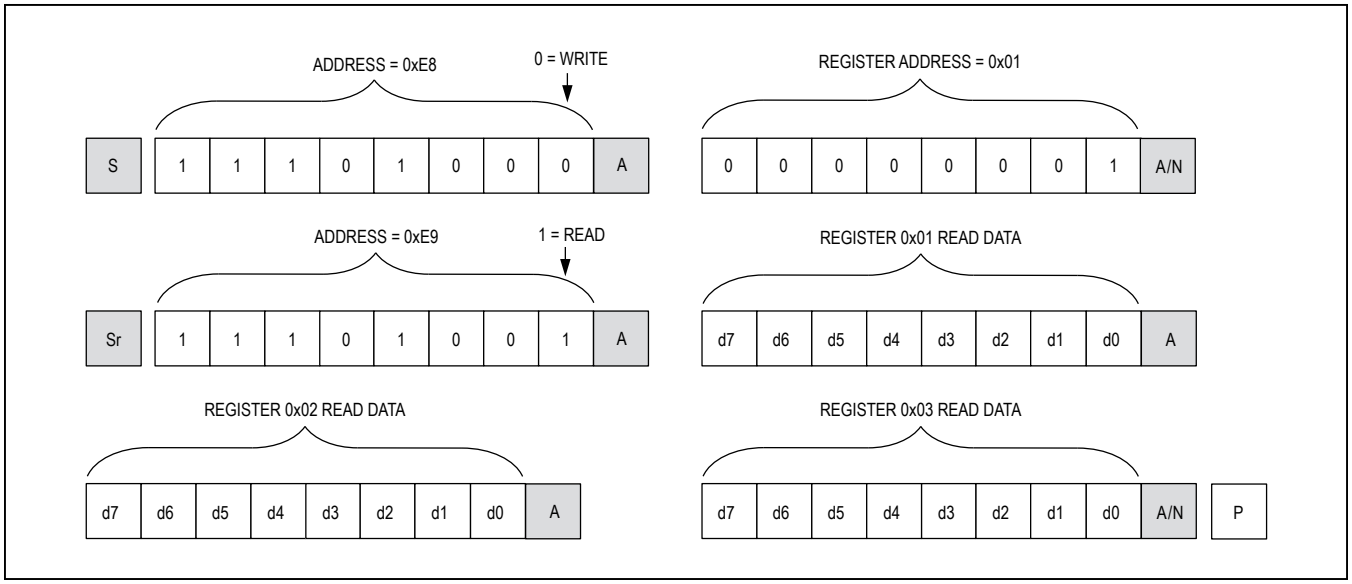


Figure 13. Format for Reading Multiple Registers

This outputs the data loaded into DI, delayed by 32 clocks, and is intended for creating a serial daisy-chain to minimize the number of select lines required by the SPI interface. The first 32 bits out of DO after the falling edge of $\overline{CS}$ are the contents of the shift register prior to $\overline{CS}$ falling, followed by the data being clocked into DI. The bits in the shift register are all zero when power is applied or after shutdown is released.

Note that the data in the shift register may not be the same as the state of the switches. The DO pin is intended for daisy-chain applications and not for switch readback. Note for (V+ - V-) less than 2.7V or V_L less than 2.7V, the DO propagation delay can limit the maximum SPI operating frequency. See Figures 14 and 15 for SPI timing diagrams. The voltage level driven out by the DO buffer is set by the voltage applied to V_L. This allows the voltage to be independent of the supply voltage.

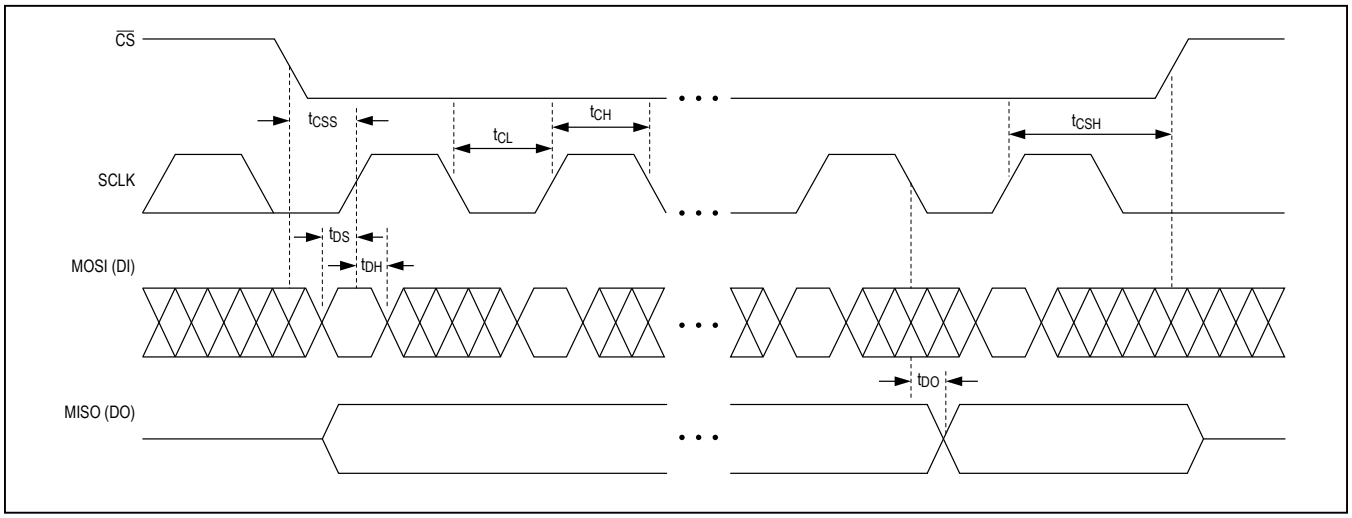


Figure 14. SPI Timing Details

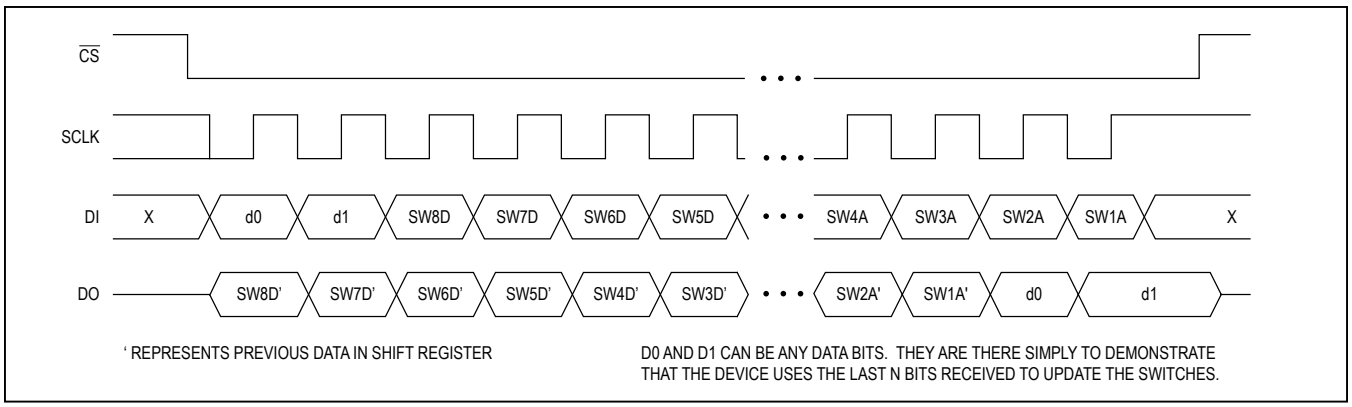


Figure 15. SPI Timing Diagram

Table 4. SPI Data Format

BYTE	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
First	SW8D	SW7D	SW6D	SW5D	SW4D	SW3D	SW2D	SW1D
Second	SW8C	SW7C	SW6C	SW5C	SW4C	SW3C	SW2C	SW1C
Third	SW8B	SW7B	SW6B	SW5B	SW4B	SW3B	SW2B	SW1B
Fourth	SW8A	SW7A	SW6A	SW5A	SW4A	SW3A	SW2A	SW1A

Applications Information

Serial Bus Configurations

The MAX14724 was designed to support a wide variety of multiplexing applications. Multiple devices can be used in a system to expand the number of ports being multiplexed. With the address-select pin provided in I²C mode, two devices can be attached to the same I²C bus simultaneously. There are also several options for addressing multiple devices when using the SPI interface. Using only three pins on the microcontroller, as many devices as desired can be loaded by connecting all $\overline{CS}$ and SCK pins in parallel and chaining the DO pin from one device to the DI pin on the next. It is also acceptable to provide a separate $\overline{CS}$ pin for each device so they can be individually addressed and loaded. Alternatively, a separate data line can be used for each device to reduce the time required to load all the devices. Some of the options and tradeoffs are listed in Table 5, as well as example application diagrams in the typical application circuit.

Extended ESD

ESD-protection structures are incorporated on all pins to protect against electrostatic discharges up to ±2kV (Human Body Model) encountered during handling and assembly. NO_ and COM_ are further protected against ESD up to ±30kV (Human Body Model), ±15kV (Air Gap Discharge method described in IEC 61000-4-2), and ±10kV (Contact Discharge method described in IEC 61000-4-2) without damage.

The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the device continues to function without latchup.

ESD Test Condition

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 16 shows the Human Body Model. Figure 17 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kΩ resistor.

Table 5. Benefits and Limitations of Different Serial-Bus Configurations

SERIAL BUS	PINS	BENEFITS	LIMITATIONS
I²C (Figure 20)	2	Fewest pins	Maximum two devices per bus, slow protocol, no simultaneous updates across all devices
SPI Daisy-Chain (Figure 21)	3	Faster than I²C with only one additional pin, simultaneous updates across all devices in chain	n x 32 clocks required to load all devices
SPI Separate $\overline{CS}$ (Figure 22)	n+2	Common SPI implementation, quick for single device updates	n x 32 clocks required to load all devices, requires an additional pin per device, no simultaneous updates across all devices
SPI Separate Data (Figure 23)	n+2	Fastest loading for multiple devices, simultaneous updates across all devices	Requires an additional pin per device, may not be supported by the SPI controller

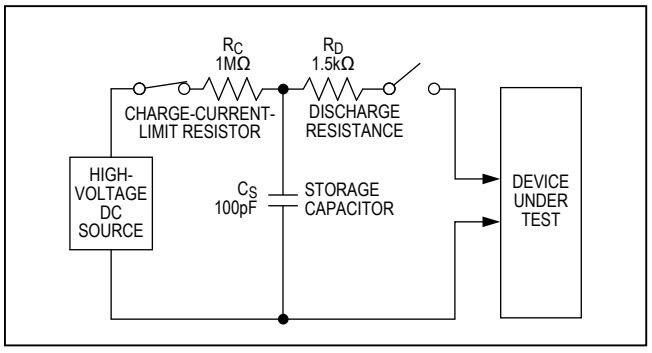


Figure 16. Human Body ESD Test Model

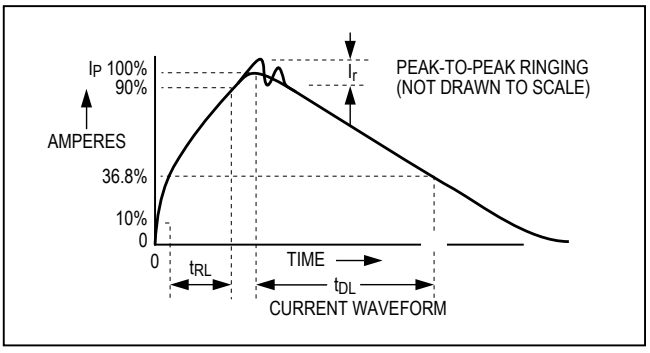


Figure 17. Human Body Current Waveform

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. However, it does not specifically refer to integrated circuits. The major difference between tests done using the Human Body Model and IEC 61000-4-2 is higher peak current in IEC 61000-4-2 because series resistance is lower in the IEC 61000-4-2 model. Hence, the ESD withstand voltage measured to IEC 61000-4-2 is generally lower than that measured using the Human Body Model. Figure 18 shows the IEC 61000-4-2 model, and Figure 19 shows the current waveform for the IEC 61000-4-2 ESD Contact Discharge test.

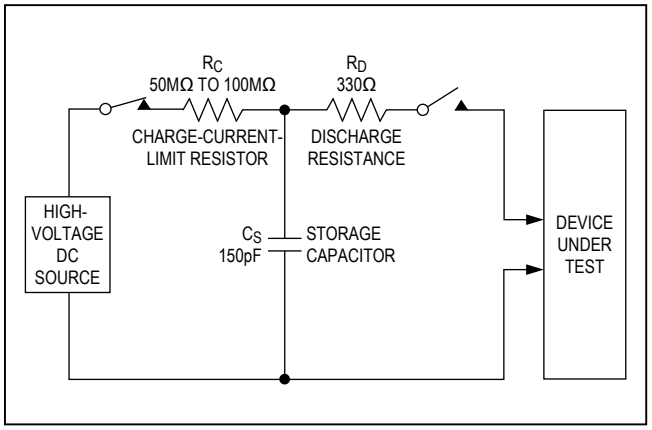


Figure 18. IEC 61000-4-2 ESD Test Model

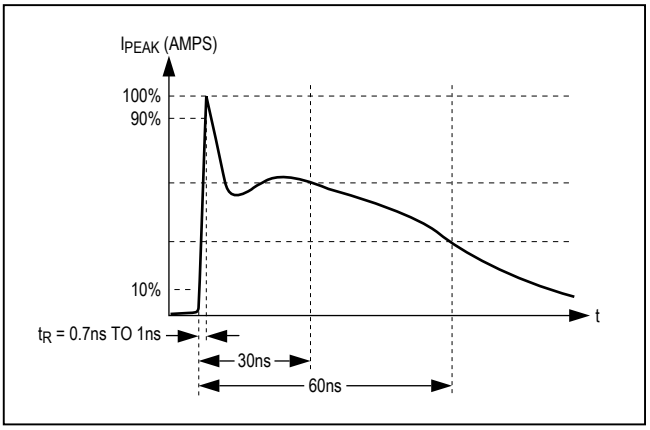


Figure 19. IEC 61000-4-2 ESD Generator Current Waveform

Typical Application Circuit

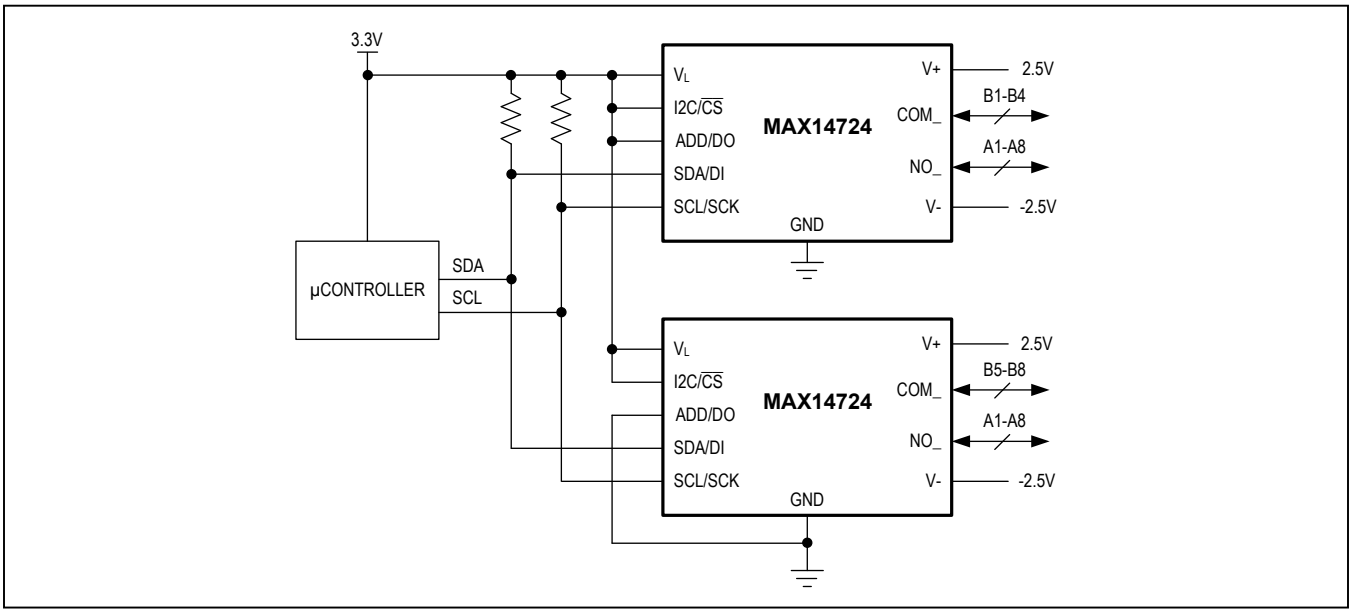


Figure 20. I²C-Controlled 8:8 MUX

Typical Application Circuit (continued)

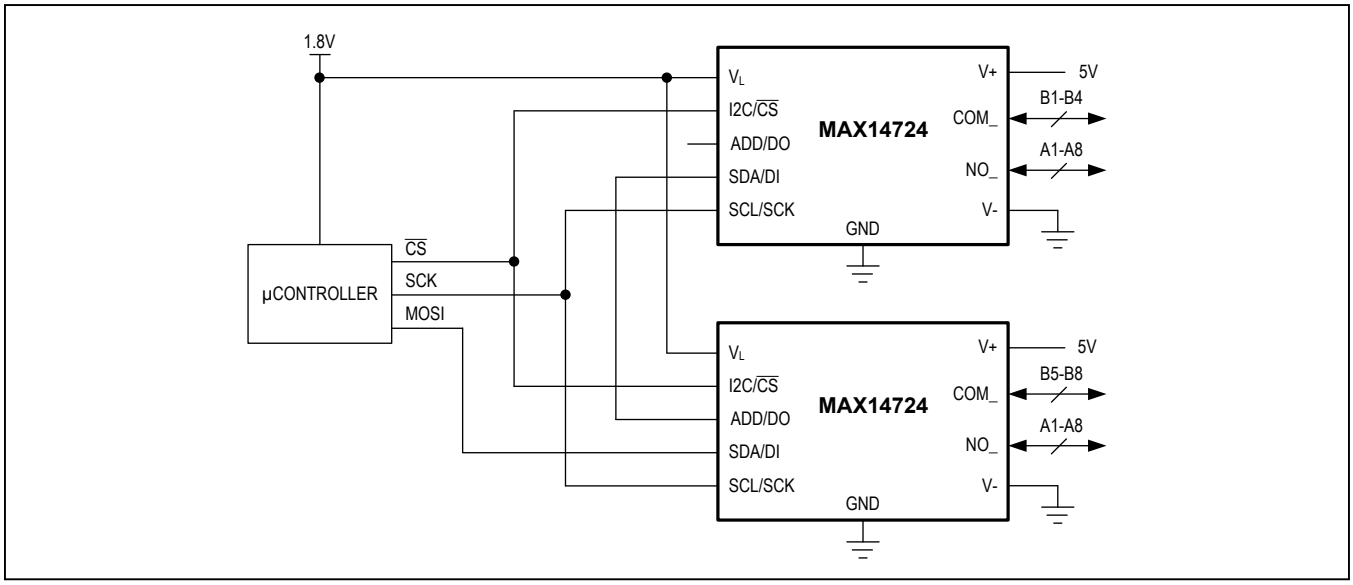


Figure 21. SPI Daisy-Chain 8:8 MUX

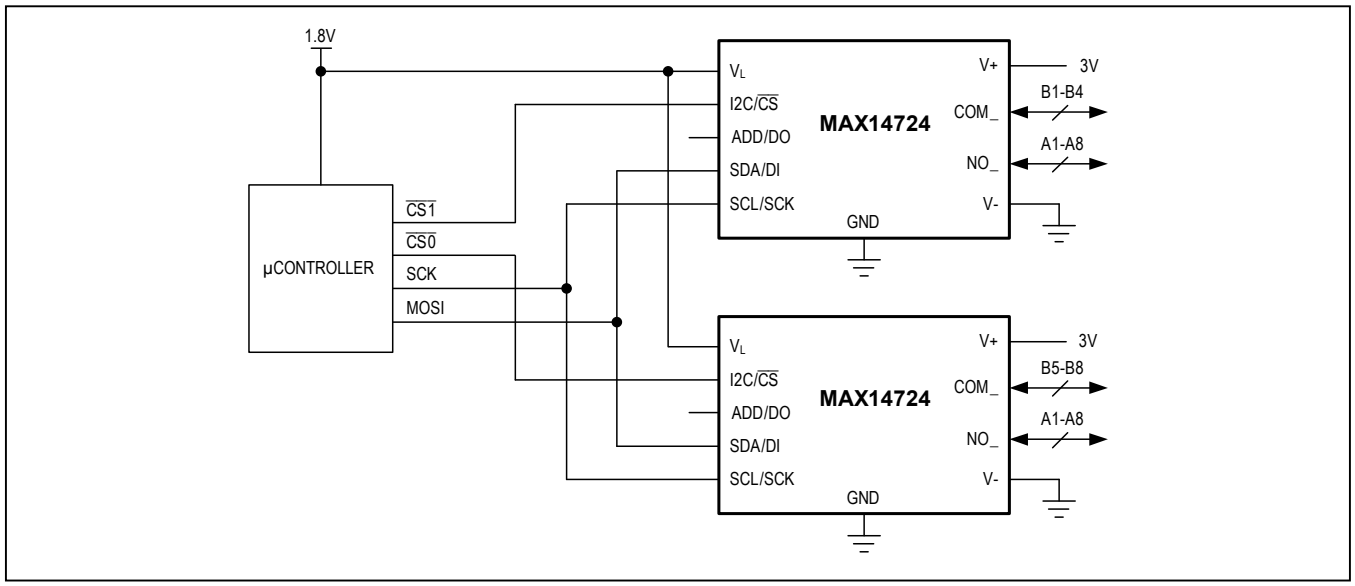


Figure 22. SPI Separate $\overline{CS}$ 8:8 Mux

Typical Application Circuit (continued)

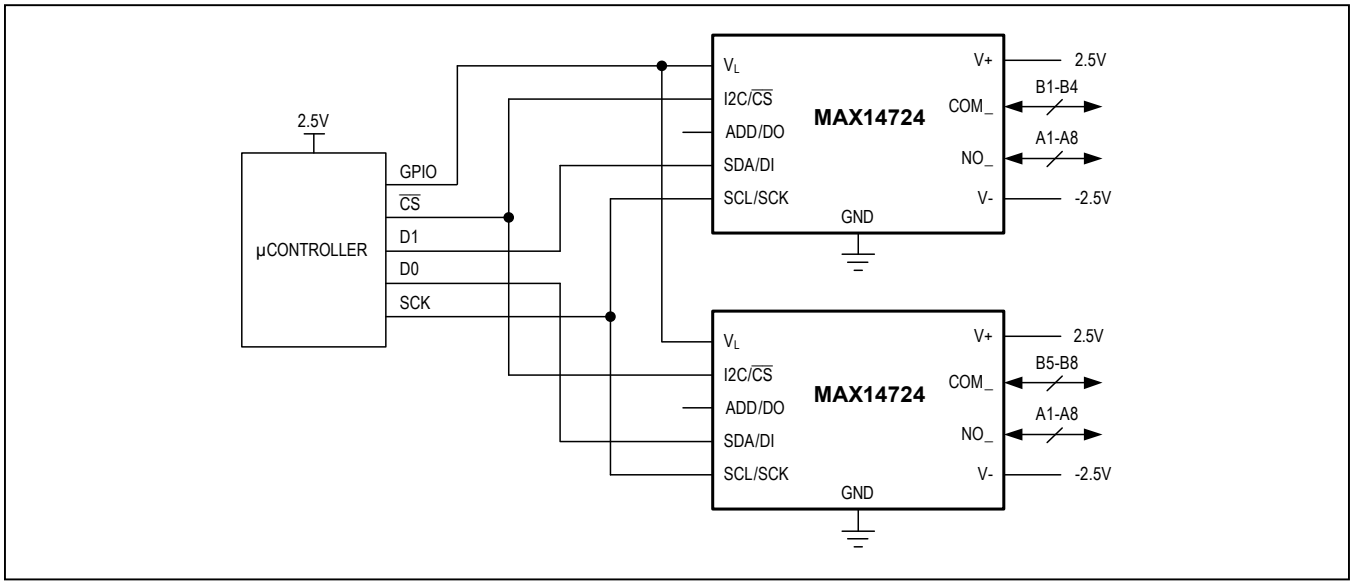


Figure 23. SPI Parallel Data 8:8 Mux

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14724ETP+	-40°C TO +85°C	20 TQFN-EP*
MAX14724ETP+T	-40°C TO +85°C	20 TQFN-EP*
MAX14724EWP+	-40°C TO +85°C	20 WLP
MAX14724EWP+T	-40°C TO +85°C	20 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2044+3C	21-0139	90-0037
20 WLP	W201C2+1	21-0779	Refer to Application Note 1891

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/15	Initial release	—
1	9/15	Removed future product designation from MAX14724ATP+T	24
2	9/15	Updated *Ordering Information*	24

