ON Semiconductor®

Product Bulletin

Document # : PB22572X
Issue Date: 4 January 2019

Title of Change:	AR0330CS Datasheet Update
Effective date:	4 January 2019
Contact information:	Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com>
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	☐ Wafer Fab ☐ Assembly Change ☐ Test Change ☑ Other Documentation

Change Sub-Category(s):

☐ Manufacturing Site Addition
☐ Manufacturing Site Transfer
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☑ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:	ON Semiconductor Sites: None	External Foundry/Subcon Sites: None

Description and Purpose:

AR0330CS Datasheet was converted to ON Semi format and updated with new information. These changes do not affect form, fit, or function of the product.

AR0330CS Datasheet Changes

1. Updated Table 2, "Available Part numbers

Old Table 2:

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0330CSSC00SPBA0-DR	3 MP 1/3" CIS	Dry Pack without Protective Film
AR0330CSSC12SPBA0-DR	3.5 MP 1/3" CIS	Dry Pack without Protective Film
AR0330SR1C00SUKA0-CR	3.5 MP 1/3" CIS	Chip Tray without Protective Film
AR0331SRSC00SHCA0-DRBR	3.1 MP 1/3" CIS	Dry Pack without Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCA0-DPBR	3.1 MP 1/3" CIS	Dry Pack with Protective Film, Double Side BBAR Glass
AR0331SRSC00SUCA0-DRBR	3.1 MP 1/3" CIS	Dry Pack without Protective Film, Double Side BBAR Glass

New Table 2:

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AR0330CS1C12SPKA0-CP	3.5 MP, 1/3-inch, 12 Deg CRA, Parallel, MIPI, CSP	Tray, Protective Film
AR0330CS1C12SPKA0-CR	3.5 MP, 1/3-inch, 12 Deg CRA, Parallel, MIPI, CSP	Tray, No Protective Film
AR0330CSSC12SPBA0-DR	3.5 MP, 1/3-inch, 12 Deg CRA, Parallel, PLCC	Tray, No Protective Film
AR0330SR1C00SUKA0-CP	3.5 MP, 1/3-inch, 0 Deg CRA, Parallel, CSP	Tray, Protective Film
AR0330SR1C00SUKA0-CR	3.5 MP, 1/3-inch, 0 Deg CRA, Parallel, CSP	Tray, No Protective Film
AR0330CS1C12SPKAH3-GEVB	3.5 MP, 1/3- inch, 12 Deg CRA, Parallel, MIPI, CSP	Evaluation board

2. Updated Features section

Old Features Section:

- 3.4 Mp (3:2) and 3.15 Mp (4:3) Still Images

Output clock maximum	98 Mp/s (parallel or 2-lane MIPI)

Supply voltage	I/O/Digital	1.7–1.9 V (1.8 V nominal) or 2.4–3.1 V (2.8 V nominal)
	Digital	1.7–1.9 V (1.8 V nominal)
	Analog	2.7–2.9 V

New Features Section:

- 3.5 Mp Active Array, 2.9 Mp (16:9) Video
  3.4 Mp (3:2) and 3.15 Mp (4:3) Still Images

Output Clock Maximum (CLK_OP)	98 Mp/s (Parallel, MIPI)

Supply Voltage	I/O/Digital	1.7–1.9 V (1.8 V Nominal) or 2.4–3.1 V (2.8 V Nominal)
	Digital	1.7–1.9 V (1.8 V Nominal)
	Analog	2.76–2.9 V

3. Updated Functional Overview Section

Old Section:

Functional Overview

The AR0330CS is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip, phase-locked loop (PLL) that can generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum output pixel rate is 98 Mp/s using a 2-lane MIPI serial interface and 98 Mp/s using the parallel interface. Figure 1 shows a block diagram of the sensor.

User interaction with the sensor is through the two-wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.4Mp active- pixel sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the signal from the column is amplified in a column amplifier and then digitized in an analog-to-digital converter (ADC). The output from the ADC is a 12-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

New Section:

FUNCTIONAL OVERVIEW

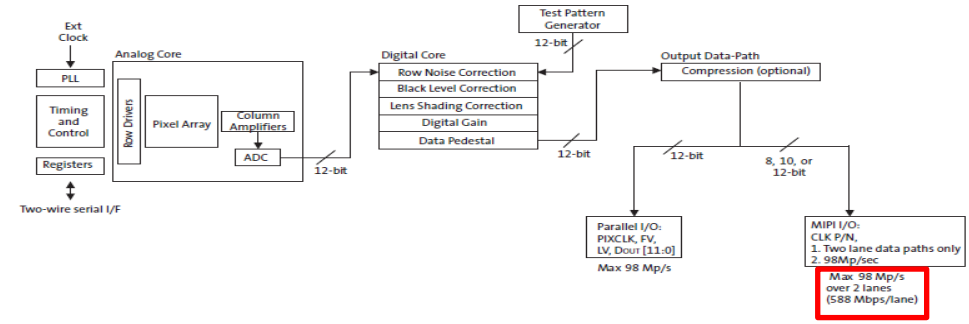
The AR0330CS is a progressive−scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase−locked loop (PLL) that can generate all internal clocks from a single master input clock running between 6 and 27 MHz. The maximum CLK_OP is 98 Mp/s using MIPI serial interface and 98 Mp/s using the parallel interface.

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 3.5 Mp active− pixel sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the signal from the column is amplified in a column amplifier and then digitized in an analog−to−digital converter (ADC). The output from the ADC is a 12−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain).

4. Updated Figure 1, "Block Diagram"

Old Figure 1:

Figure 1: Block Diagram



New Figure 1:

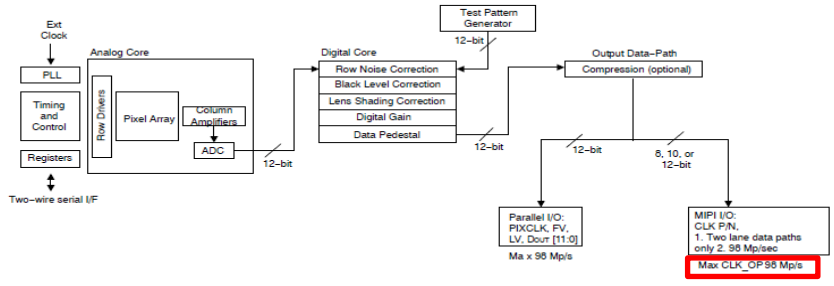


Figure 1. Block Diagram

5. Updated Table 3, "Available Aspect Ratios in the AR0330S Sensor"

Old Table 3:

Table 3: Available Aspect Ratios in the AR0330CS Sensor

Aspect Ratio		Sensor Array Usage
3:2	Still Format #1	2256(H) x 1504(V)
4:3	Still Format #2	2048 (H) x 1536 (V)
16:10	Still Format #3	2256 (H) x 1440 (V)
16:9	HD Format	2304 (H) x 1296 (V)

New Table 3:

Table 3. AVAILABLE ASPECT RATIOS IN THE AR0330CS SENSOR

Aspect Ratio		Sensor Array Usage
3:2	Still Format #1	2256(H) x 1504(V)
4:3	Still Format #2	2048 (H) x 1536 (V)
16:10	Still Format #3	2256 (H) x 1440 (V)
16:9	FHD Format	2304 (H) x 1296 (V)

Updated Table 4, "Available Working Modes in the AR0330S Sensor"

Old Table 4:

Table 4: Available Working Modes in the AR0330CS Sensor

Mode	Aspect Ratio	Active Readout Window	Sensor Output Resolution	FPS (2-Lane MIPI Interface)	FPS (Parallel Interface)	Subsampling	FOV
1080p + EIS	16:9	2304 x 1296	2304 x 1296	30	30	–	100%
3M Still	4:3	2048 x 1536	2048 x 1536	30	25	–	100%
	3:2	2256 x 1504	2256 x 1504	30	25	–	100%
WVGA + EIS	16:9	2304 x 1296	1152 x 648	60	60	2x2	100%
WVGA + EIS Slow-motion	16:9	2304 x 1296	1152 x 648	120	N/A	2x2	100%

New Table 4:

Table 4. AVAILABLE WORKING MODES IN THE AR0330CS SENSOR

Mode	Aspect Ratio	Active Readout Window	Sensor Output Resolution	FPS (2 lane MIPI, 12 bit)	FPS (Parallel Interface)	Subsampling	FOV
1080p + EIS	16:9	2304 x 1296	2304 x 1296	30	30	–	100%
3M Still	4:3	2048 x 1536	2048 x 1536	30	25	–	100%
	3:2	2256 x 1504	2256 x 1504	30	25	–	100%
WVGA + EIS	16:9	2304 x 1296	1152 x 648	60	60	2 x 2	100%

6. Updated Table 11, "DC Electrical Definitions and Characteristics (MIPI Mode)"

Old Table 11:

Table 11: DC Electrical Definitions and Characteristics (MIPI Mode)
f_{EXTCLK} = 24 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; Output load = 68.5pF; T_J = 60°C; Data Rate =588 Mbps; DLL set to 0; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD_IO}	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.7	2.8	2.9	V
Pixel supply voltage	V_{AA_PIX}	2.7	2.8	2.9	V
PLL supply voltage	V_{DD_PLL}	2.7	2.8	2.9	V
MIPI supply voltage	V_{DD_MIPI}	2.7	2.8	2.9	V
Digital operating current		-	114	-	mA
I/O digital operating current		-	0	-	mA
Analog operating current		-	41	-	mA
Pixel supply current		-	9.9	-	mA
PLL supply current		-	15	-	mA
MIPI digital operating current		-	35	-	mA

New Table 11:

Table 11. DC Electrical Definitions and Characteristics (MIPI Mode)
f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 1.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; Output load = 68.5 pF; T_J = 60°C; Data Rate = 588 Mbps; DLL set to 0; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD_IO}	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.76	2.8	2.9	V
Pixel supply voltage	V_{AA_PIX}	2.76	2.8	2.9	V
PLL supply voltage	V_{DD_PLL}	2.7	2.8	2.9	V
MIPI supply voltage	V_{DD_MIPI}	2.7	2.8	2.9	V
Digital operating current		–	114	–	mA
I/O digital operating current		–	0	–	mA
Analog operating current		–	41	–	mA
Pixel supply current		–	9.9	–	mA
PLL supply current		–	15	–	mA
MIPI digital operating current		–	35	–	mA

7. Updated Table 12, "DC Electrical Definitions and Characteristics (Parallel Mode)"

Old Table 12:

Table 12: DC Electrical Definitions and Characteristics (Parallel Mode)
f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 1.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; Output load = 68.5 pF; TJ = 60°C; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD_IO}	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.7	2.8	2.9	V
Pixel supply voltage	V_{AA_PIX}	2.7	2.8	2.9	V
PLL supply voltage	V_{DD_PLL}	2.7	2.8	2.9	V
Digital operating current	I(V_{DD})		66.5	75	mA
I/O digital operating current	I(V_{DD_IO})		24	35	mA
Analog operating current	I(V_{AA})		36	44	mA

New Table 12:

Table 12. DC Electrical Definitions and Characteristics (Parallel Mode)

f_{EXTCLK} = 24 MHz; V_{DD} = 1.8 V; V_{DD_IO} = 1.8 V; V_{AA} = 2.8 V; V_{AA_PIX} = 2.8 V; V_{DD_PLL} = 2.8 V; Output load = 68.5 pF; T_J = 60°C; 2304 x 1296 at 30 fps

Definition	Symbol	Min	Typ	Max	Unit
Core digital voltage	V_{DD}	1.7	1.8	1.9	V
I/O digital voltage	V_{DD_IO}	1.7	1.8	1.9	V
		2.4	2.8	3.1	V
Analog voltage	V_{AA}	2.76	2.8	2.9	V
Pixel supply voltage	V_{AA_PIX}	2.76	2.8	2.9	V
PLL supply voltage	V_{DD_PLL}	2.7	2.8	2.9	V
Digital operating current	I(V_{DD})		66.5	75	mA
I/O digital operating current	I(V_{DD_IO})		24	35	mA
Analog operating current	I(V_{AA})		36	44	mA
Pixel supply current	I(V_{AA_PIX})		10.5	18	mA
PLL supply current	I(V_{DD_PLL})		6	11	mA

8. Updated Parallel PLL Configuration Section

Old Section:

The maximum output of the parallel interface is 98 Mpixel/s (CLK_OP). This will limit the readout clock (CLK_PIX) to 49 Mpixel/s. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK}, or CLK_OP when configured to use the parallel interface.

New Section:

The maximum output of the parallel interface is 98 Mpixel/s (CLK_OP). This will limit the readout clock (CLK_PIX) to 49 MHz. The sensor will not use the F_{SERIAL}, F_{SERIAL_CLK} when configured to use the parallel interface.

9. Updated Table 19, "PLL Parameters for the Parallel Interface"

Old Table 19:

Table 19: PLL Parameters for the Parallel Interface

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	27	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		49	Mpixel/s
Output Clock	CLK_OP		98	Mpixel/s

New Table 19:

Table 19. PLL PARAMETERS FOR THE PARALLEL INTERFACE

Parameter	Symbol	Min	Max	Unit
External Clock	EXTCLK	6	27	MHz
VCO Clock	F_{VCO}	384	768	MHz
Readout Clock	CLK_PIX		49	MHz
Output Clock	CLK_OP		98	Mpixel/s

10. Updated Table 20, "Example PLL Configuration for the Parallel Interface"

Old Table 20:

Table 20: Example PLL Configuration for the Parallel Interface

Parameter	Value	Output
F_{VCO}		588 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		49 Mpixel/s (= 588 MHz / 12)
CLK_OP		98 Mpixel/s (= 588 MHz / 6)
Output pixel rate		98 MPixel/s

New Table 20:

Table 20. EXAMPLE PLL CONFIGURATION FOR THE PARALLEL INTERFACE

Parameter	Value	Output
F_{VCO}		588 MHz (Max)
vt_sys_clk_div	1	
vt_pix_clk_div	6	
CLK_PIX		49 MHz (CLK_OP/2)
CLK_OP		98 Mpixel/s (= 588 MHz / 6)
Output pixel rate		98 MPixel/s

11. Updated Table 22, "Example PLL Configurations for the Serial Interface"

Old Table 22:

Table 22: Example PLL Configurations for the Serial Interface

Parameter	2-lane		1-lane			Notes
	12-bit	10-bit	12-bit	10-bit	8-bit	
F_{VCO}	588	490	768	768	768	MHz
vt_sys_clk_div	2	2	4	4	4	
vt_pix_clk_div	6	5	6	5	4	
op_sys_clk_div	1	1	1	1	1	
op_pix_clk_div	12	10	12	10	8	
F_{SERIAL}	588	490	768	768	768	MHz
F_{SERIAL_CLK}	294	245	384	384	384	MHz
CLK_PIX	49	49	32	38.4	48	Mpixel/s
CLK_OP	49	49	64	76.8	96	Mpixel/s
Pixel Rate	98	98	64	76.8	96	Mpixel/s

New Table 22:

Table 22. EXAMPLE PLL CONFIGURATIONS FOR THE SERIAL INTERFACE

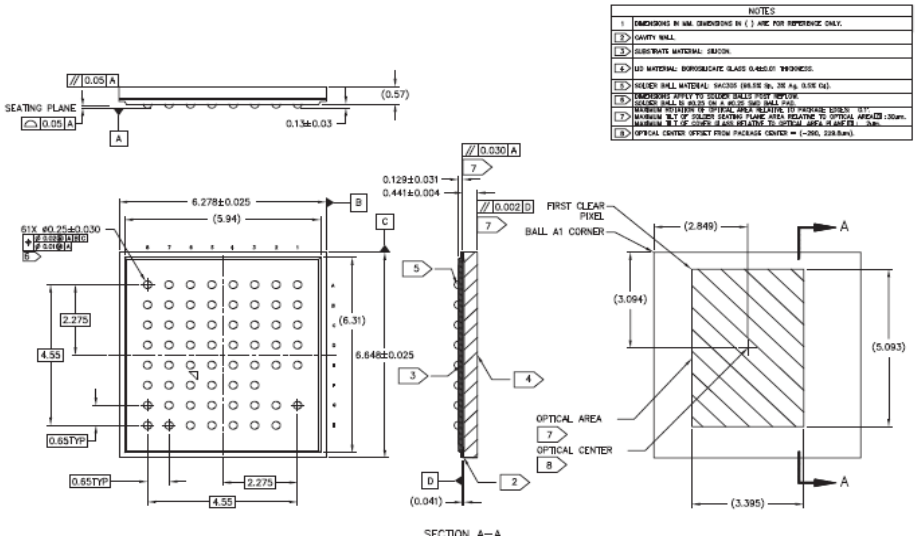
Parameter	2-lane		1-lane			Notes
	12-bit	10-bit	12-bit	10-bit	8-bit	
F_{VCO}	768	760	768	768	768	MHz
vt_sys_clk_div	2	2	4	4	4	
vt_pix_clk_div	6	5	6	5	4	
op_sys_clk_div	1	1	1	1	1	
op_pix_clk_div	12	10	12	10	8	
F_{SERIAL}	768	760	768	768	768	MHz
F_{SERIAL_CLK}	384	380	384	384	384	MHz
CLK_PIX	64	76	32	38.4	48	MHz
CLK_OP	64	76	64	76.8	96	Mpixel/s
Pixel Rate	128	144	64	76.8	96	Mpixel/s

12. Updated "CSP Parallel/MIPI Package Drawing with official ON Semi case outline

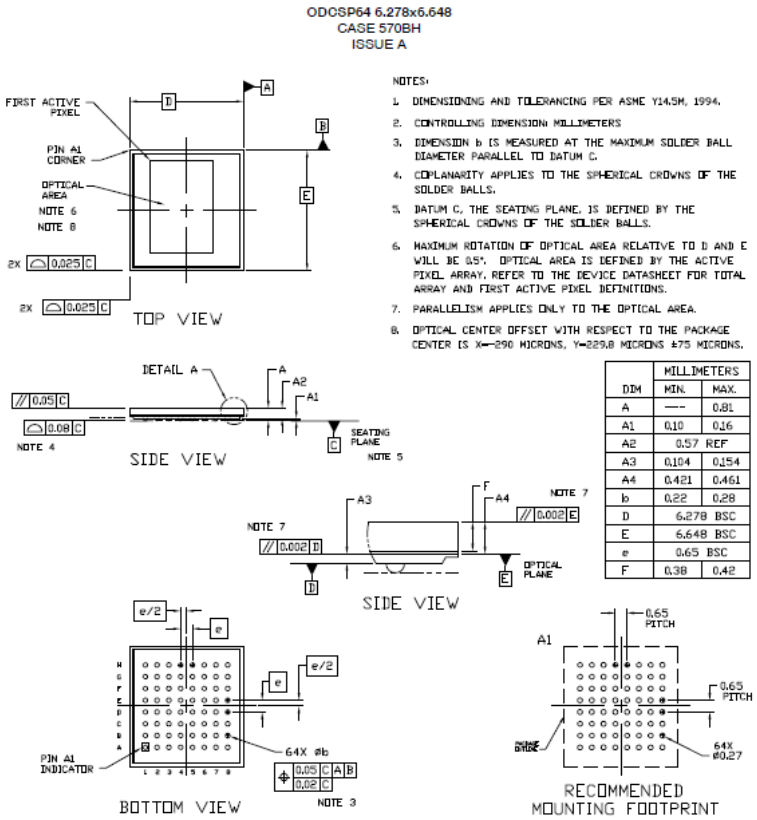
Old Figure 41:

CSP Packages

Figure 41: CSP Parallel/MIPI Package



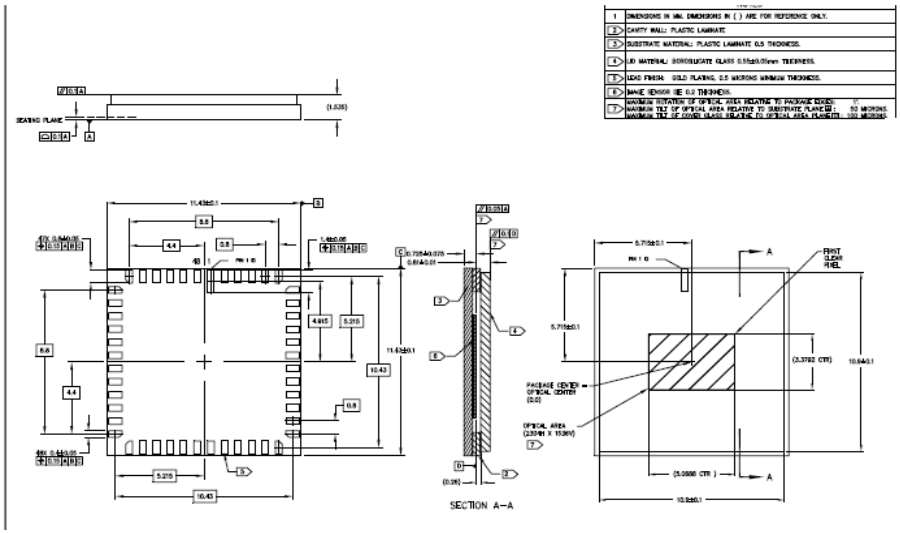
New Case Outline 570BH:



13. Updated PLCC Package Drawing with official ON Semi case outline

Old Figure 42:

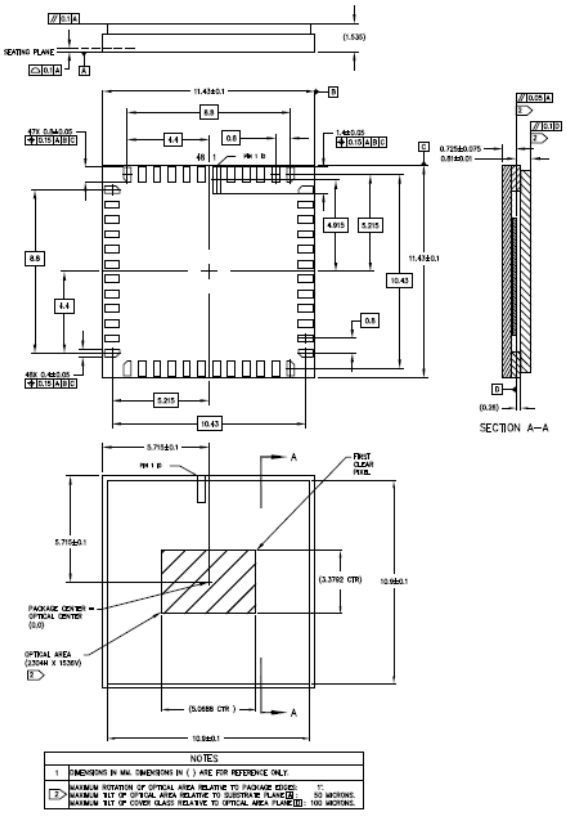
Figure 42: PLCC Package Drawing



New CASE 776AM:

PACKAGE DIMENSIONS

PLCC48 11.43x11.43
CASE 776AM
ISSUE O



List of Affected Parts:

Note: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal.**

AR0330CS1C12SPKA0-CP	AR0330CSSC12SPBA0-DR	AR0330SR1C00SUKA0-CP
AR0330CS1C12SPKA0-CR	AR0330CSSC12SPBA0-DR-E	AR0330SR1C00SUKA0-CR

Appendix A: Changed Products

D

Product	Customer Part Number
AR0330CS1C12SPKA0-CP	
AR0330CS1C12SPKA0-CR	
AR0330CSSC12SPBA0-DR	
AR0330SR1C00SUKA0-CP	
AR0330SR1C00SUKA0-CR	